8 INTERFACE

8.1 MPU Interface Type Selection

ST77916 supports 8 bit parallel data bus for 8080 series CPU, RGB serial interfaces, SPI interface, QSPI interface, MIPI interface. Selection of these interfaces are set by IM[2:0] pins as shown below.

IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	3-line 9bit serial I/F	SDA: in/out
0	0	1	MIPI I/F	DP/DN
0	1	0	2 data lane serial I/F	SDA1: in/out、SDA2: in
0	1	1	QSPI I/F	SDA1: in/out、SDA[3:0]: in
1	0	0	RGB_3-line 9bit serial I/F	SDA: in/out、DB[5:0]: in
1	0	1	RGB_4-line 8bit serial I/F	SDA: in/out、DB[5:0]: in
1	1	0	4-line 8bit serial I/F	SDA: in/out
1	1	1	80-8bit parallel I/F	DB[7:0]: in/out

Table 6 Interface Type Selection

8.2 8080-Ⅰ Series MCU Parallel Interface

The MCU can use 8080-8bits parallel interface: 11-lines with 8-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[7:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[7:0] bits is either display data or command parameter. When D/C='0', D[7:0] bits is command. The interface functions of 8080-8bits parallel interface are given in following table.

IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read back selection
1	1	1	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
				1	↑	1	Read 8-bit display data (D7 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)

Table 7 the function of 8080 - 8 bits parallel interface

8.2.1 Write cycle sequence

The write cycle means that the host writes information (command / data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[7:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

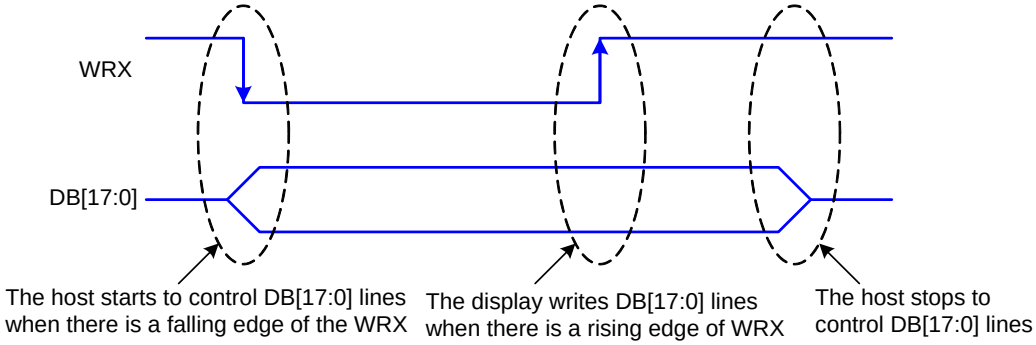


Figure 8 8080 - 8 bits WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

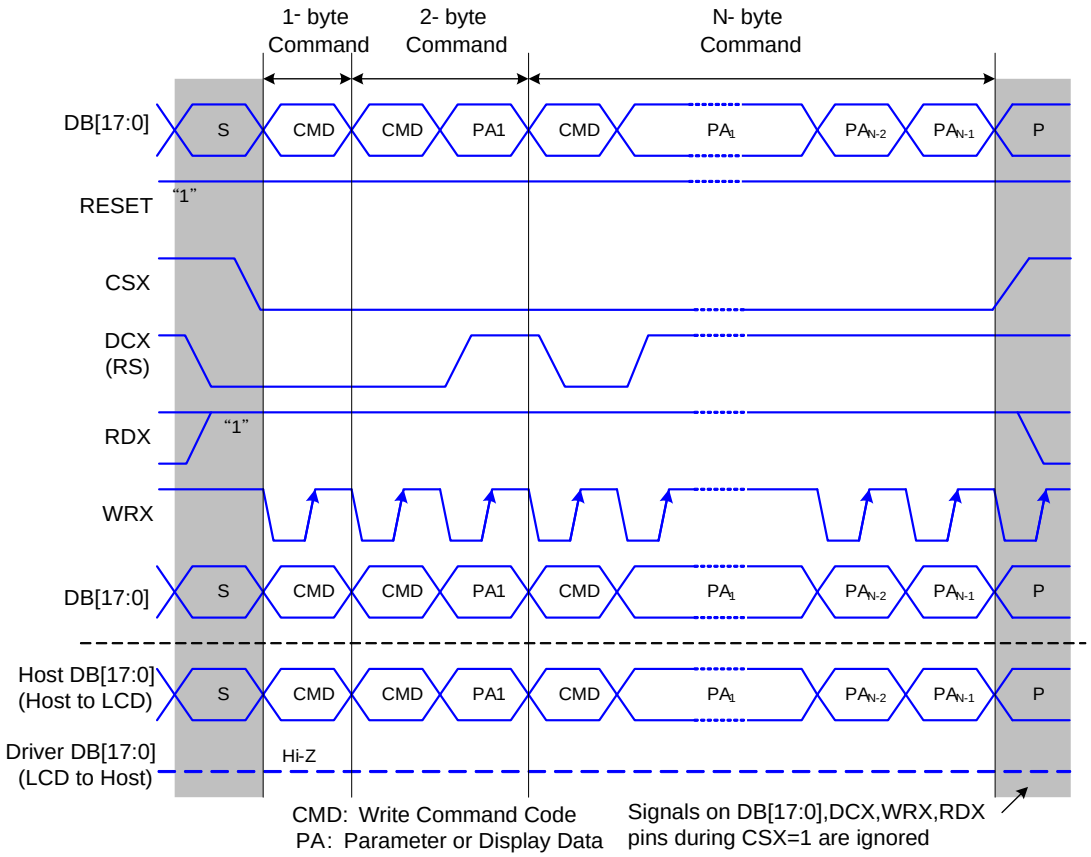


Figure 9 8080 - 8 bits Parallel Bus Protocol, Write to Register or Display RAM

8.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[7:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

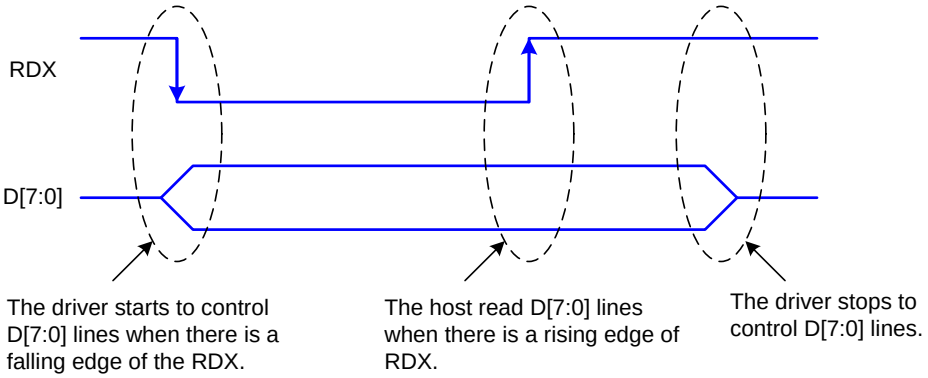


Figure 10 8080 – 8 bits RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

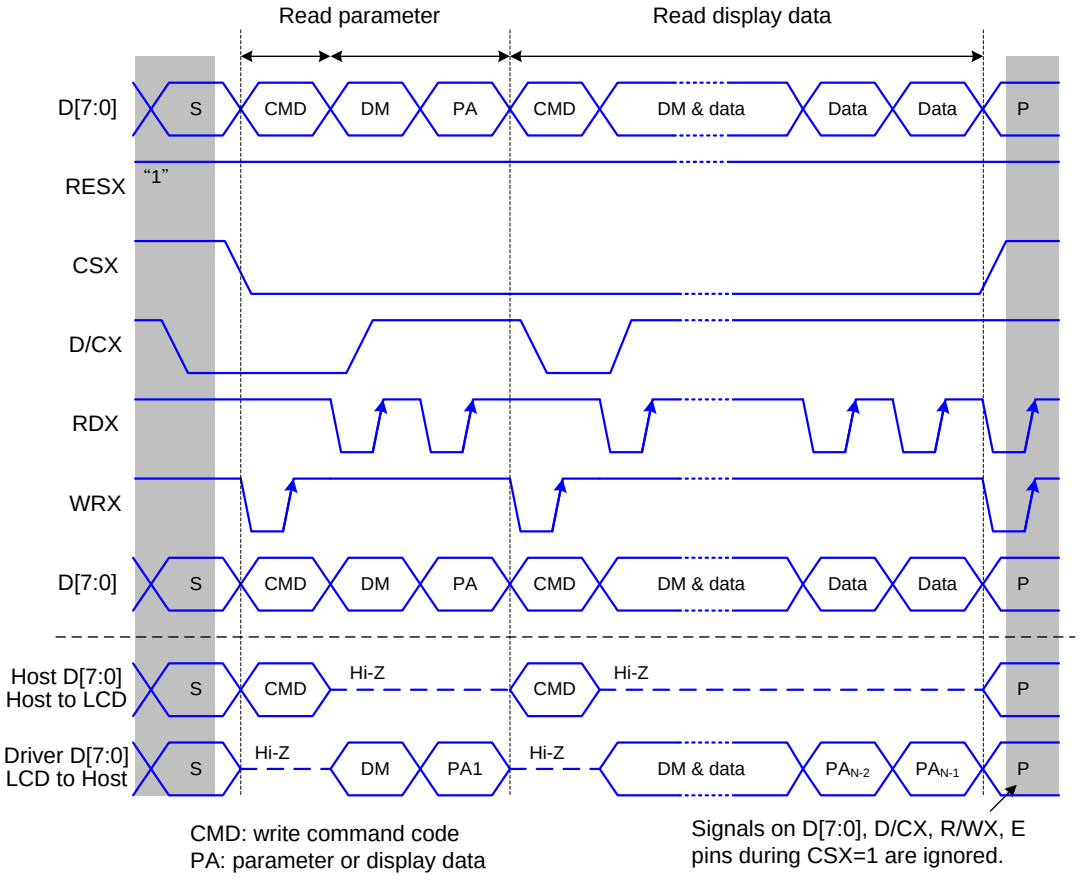


Figure 11 8080 - 8 bits parallel bus protocol, read data from register or display RAM

8.3 Serial Interface

IM2	IM1	IM0	Interface	Read back selection
0	0	0	3-line serial interface Ⅰ	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	0	4-line serial interface Ⅰ	

Table 8 Selection of serial interface

The serial interface is either 3-lines/9-bits or 4-lines/8-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

8.3.1 Pin description

3-line serial interface Ⅰ

Pin Name	Description
CSXP	Chip selection signal
RDXP (SCLP)	Clock signal
D0P (SDAP)	Serial input/output data

4-line serial interface Ⅰ

Pin Name	Description
CSXP	Chip selection signal
DCXP (A0)	Data is regarded as a command when DCXP is low Data is regarded as a parameter or data when DCXP is high
RDXP (SCLP)	Clock signal
D0P (SDA)	Serial input/output data

Table 9 pin description of serial interface

8.3.2 Command write mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

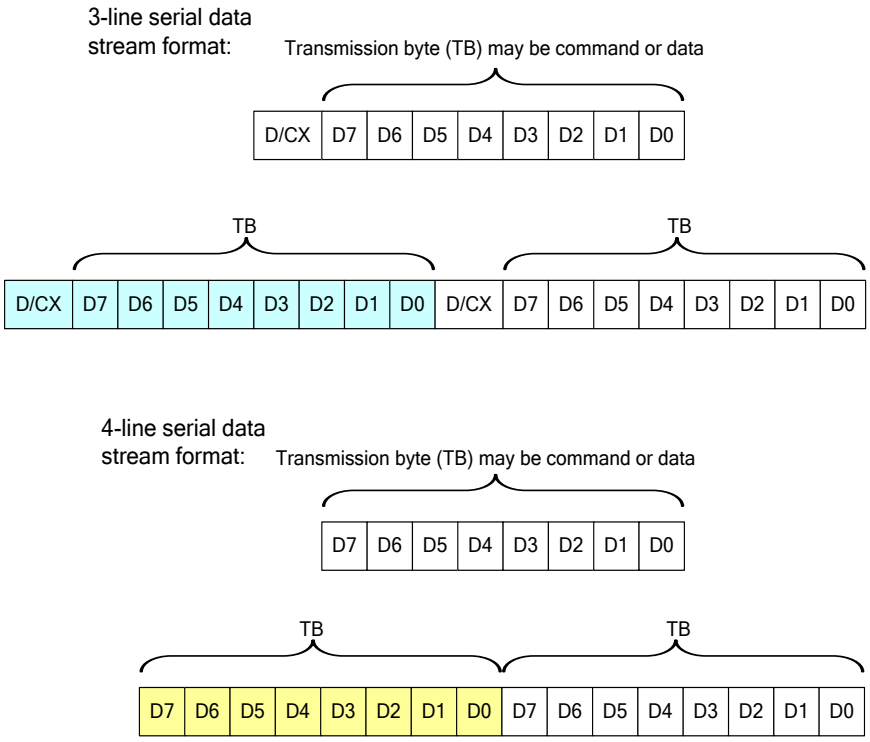


Figure 12 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL..

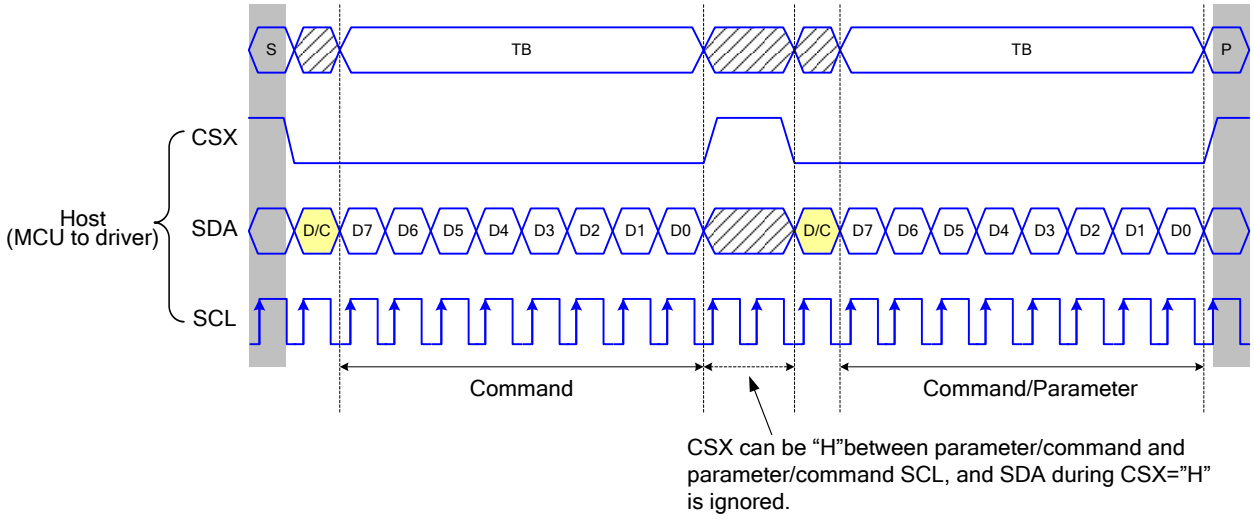


Figure 13 3-line serial interface write protocol (write to register with control bit in transmission)

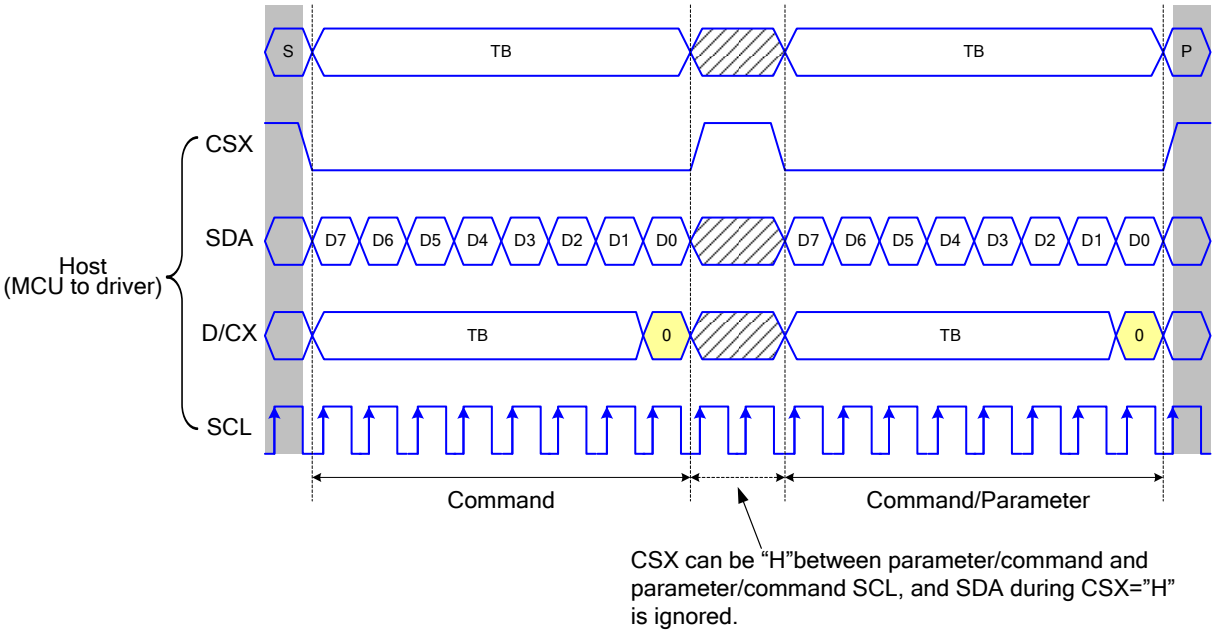


Figure 14 4-line serial interface write protocol (write to register with control bit in transmission)

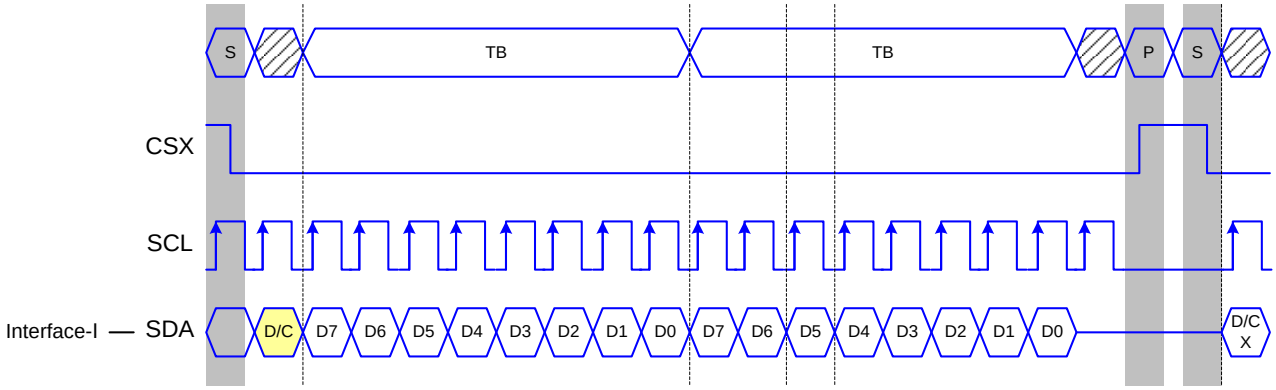
8.3.3 Read function

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

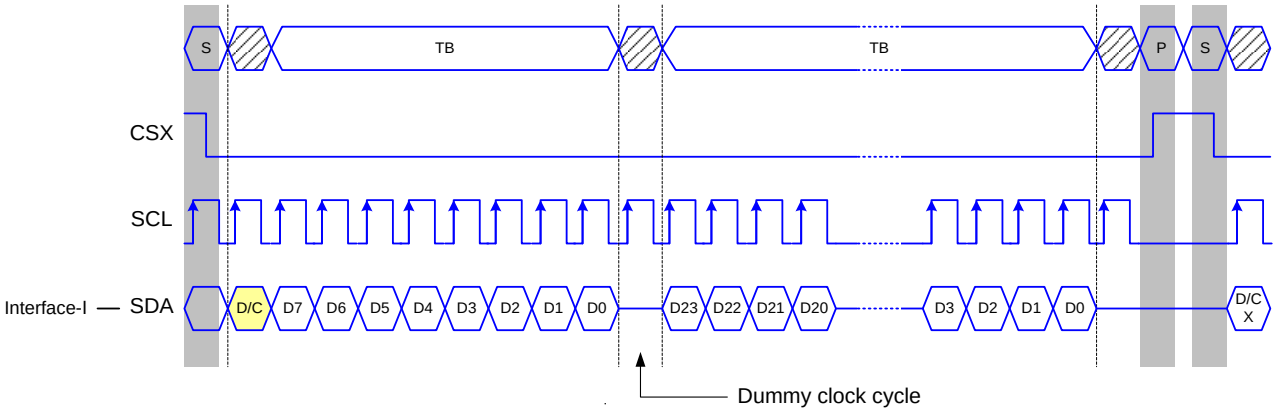
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

8.3.4 3-line serial interface Ⅰ protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read):



3-line Serial Protocol (for RDDST command: 32-bit read):

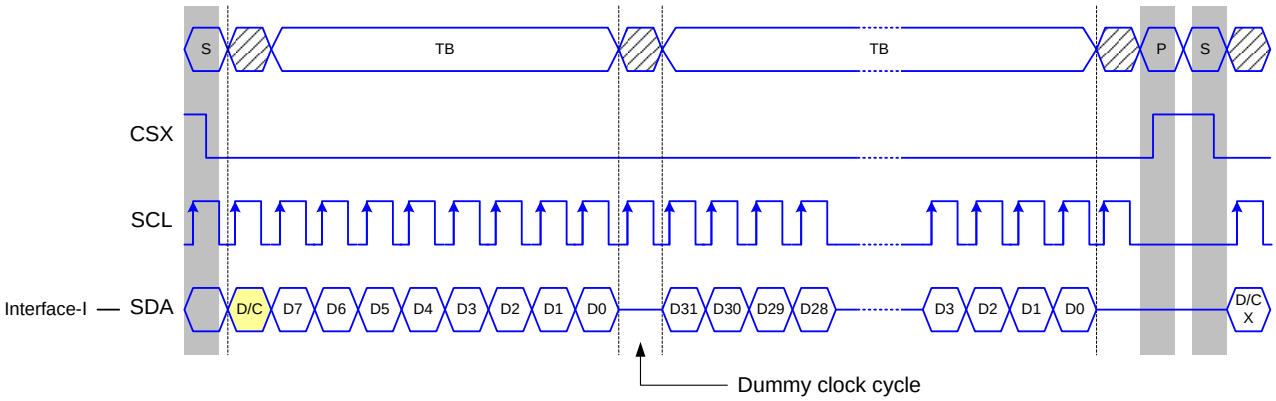
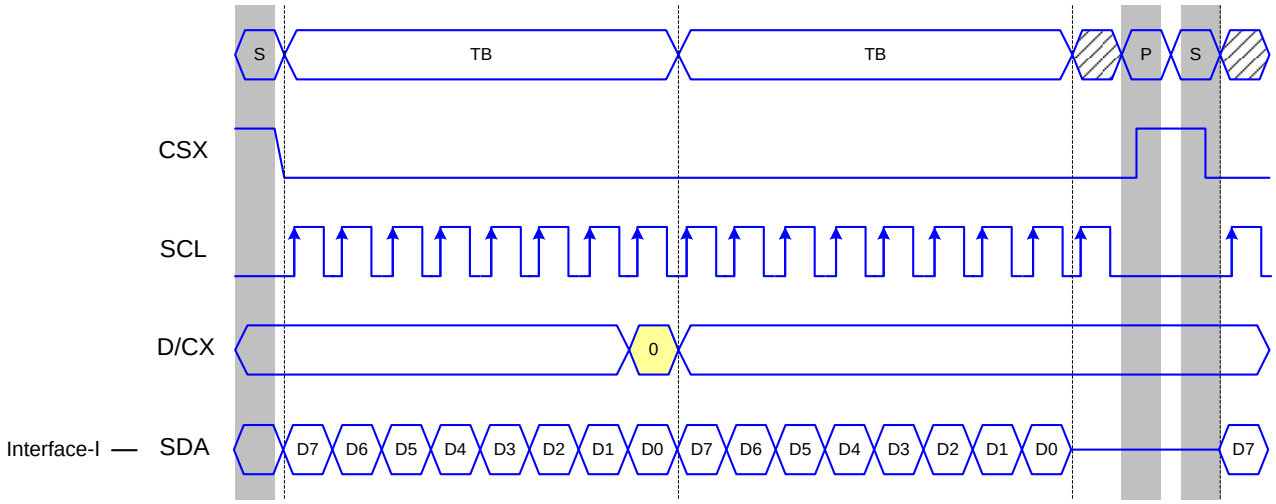


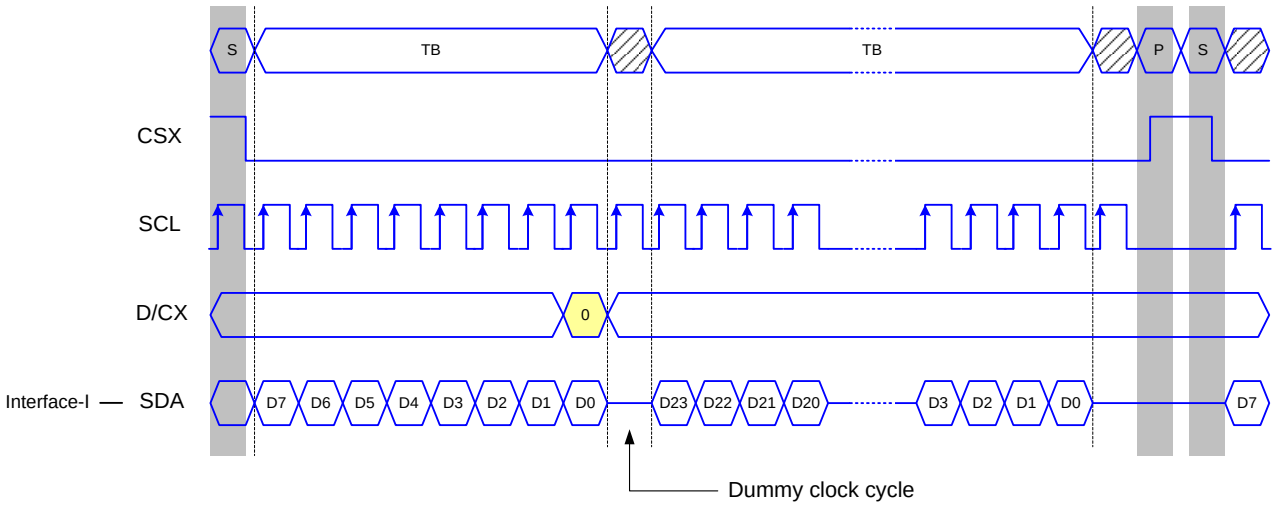
Figure 15 3-line serial interface read protocol

8.3.5 4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

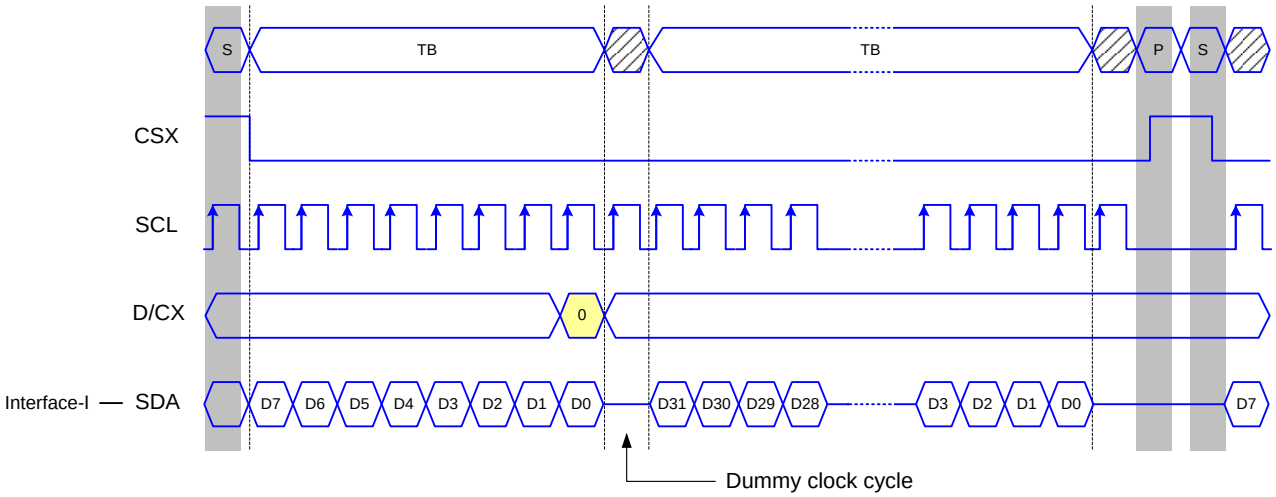


Figure 16 4-line serial interface read protocol

8.4 2 data lane serial Interface

Interface selection:

IM2	IM1	IM0	Interface	Read back selection
0	1	0	2 data lane serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read)

Table 10 IM pin selection

2-wire data lane serial interface use: CSX (chip enable), SCL (serial clock) and SDA1 (serial data input/output 1), and SDA2 (serial data input 2).

2 data lane hardware suggestion and Pin description:

2 data lane serial interface, IM[2:0]=010

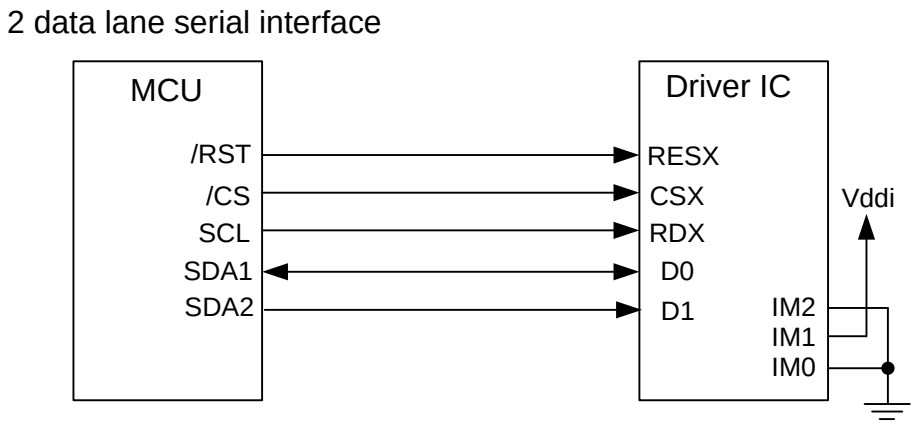


Figure 17 Hardware suggestion of 2 data lane serial interface

Pin Name	Description
CSX	Chip selection signal
RDXP (SCLP)	Clock signal
D0P (SDA1P)	Serial data input/output1
D1P	Serial data input2

Table 11 Pin description of 2 data lane serial interface

Command write mode:

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface, so users can ignore the input data of D1P.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

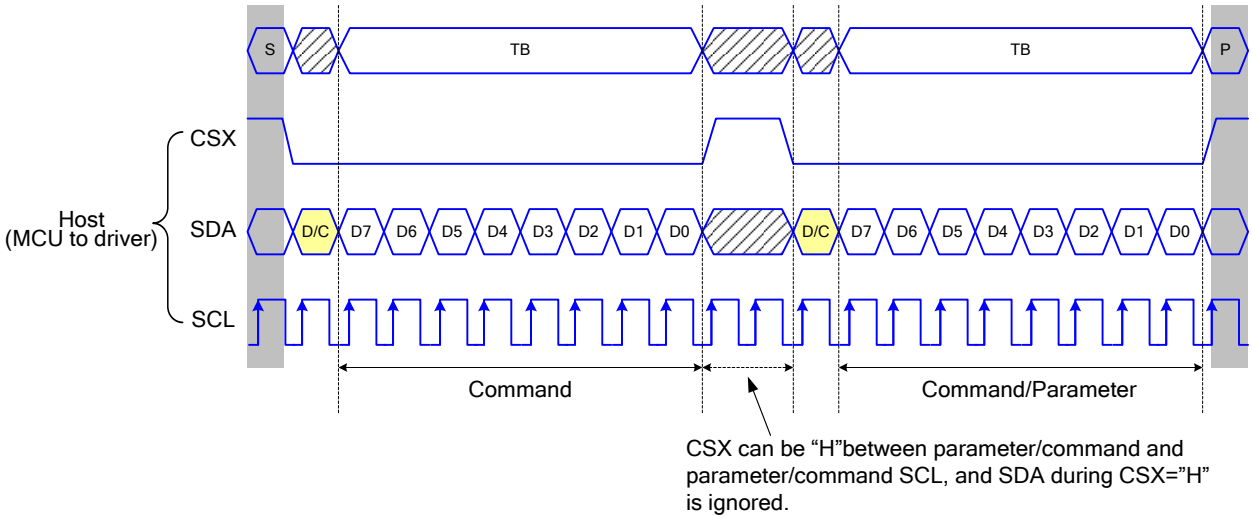


Figure 18 3-line serial interface write protocol (write to register with control bit in transmission)

SRAM write mode:

The SRAM write mode of 2-wire data line serial interface need use SDA pin and D1P pin to be data input pins.

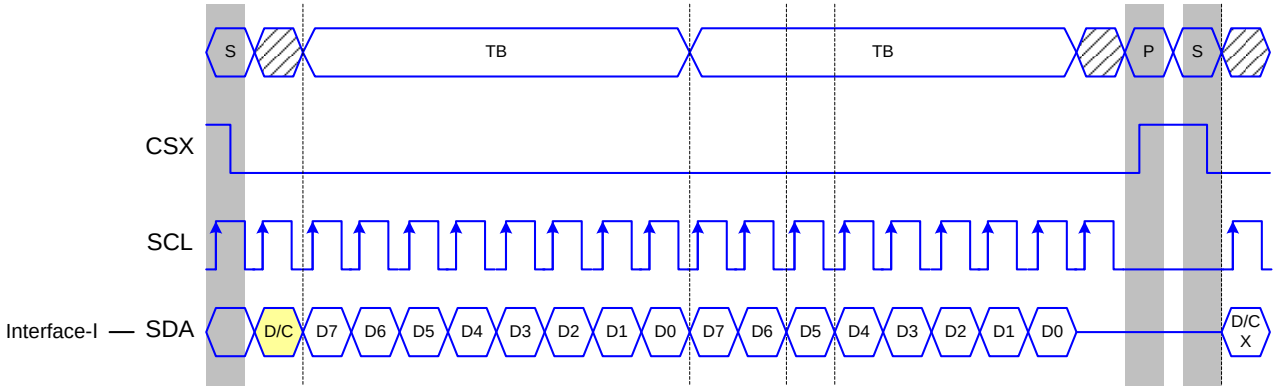
Read function:

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and D1P pin can be ignored. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

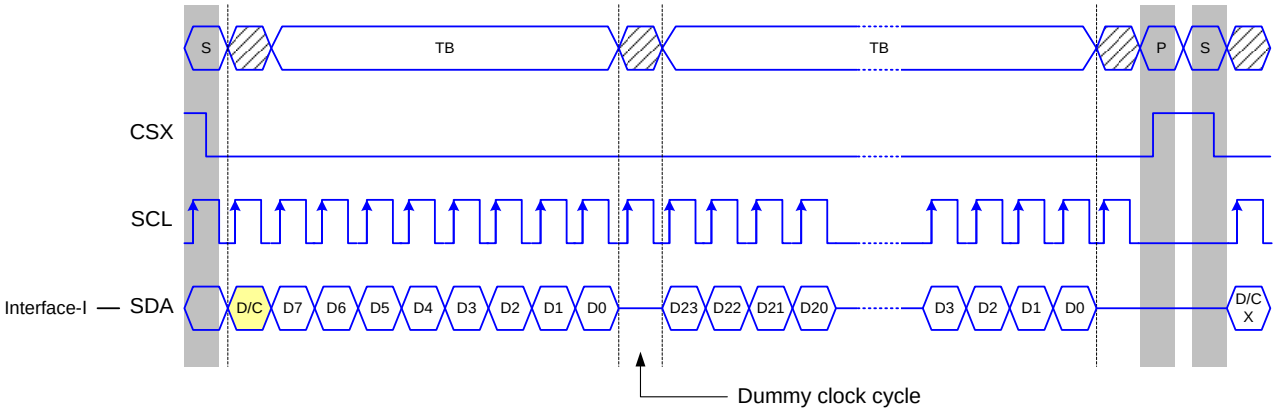
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line serial interface Ⅰ protocol:

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

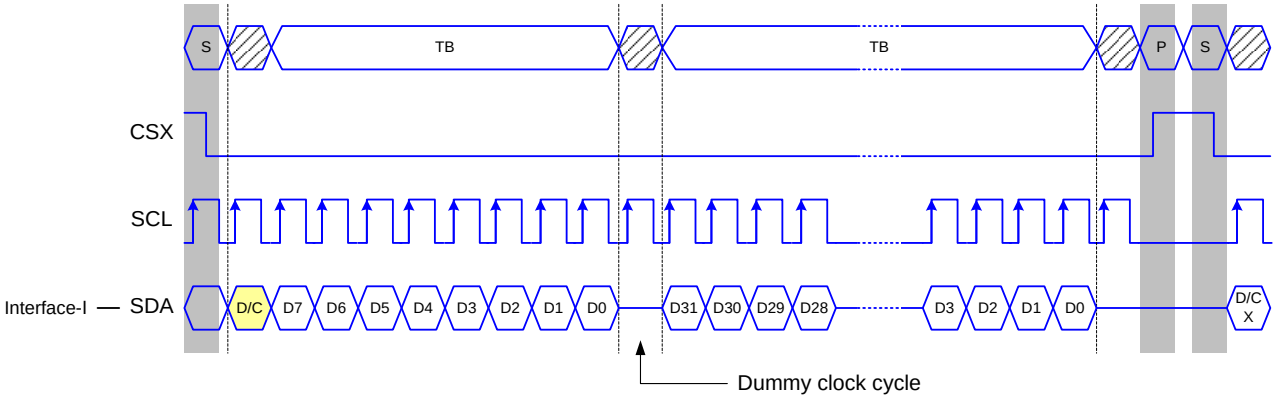


Figure 19 3-line serial interface read protocol

8.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

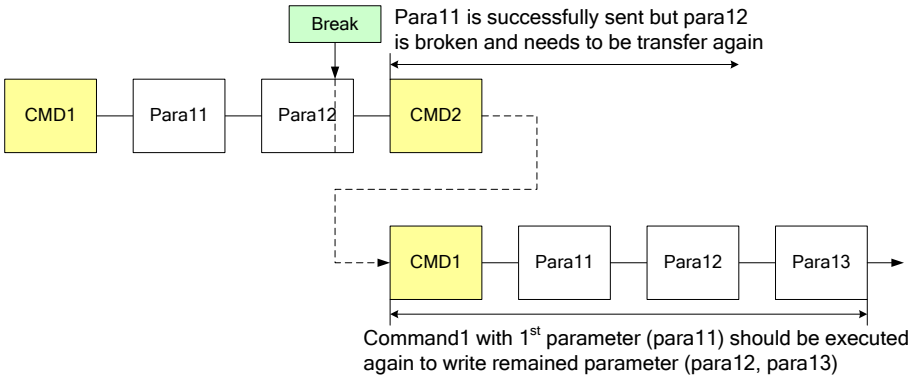


Figure 20 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

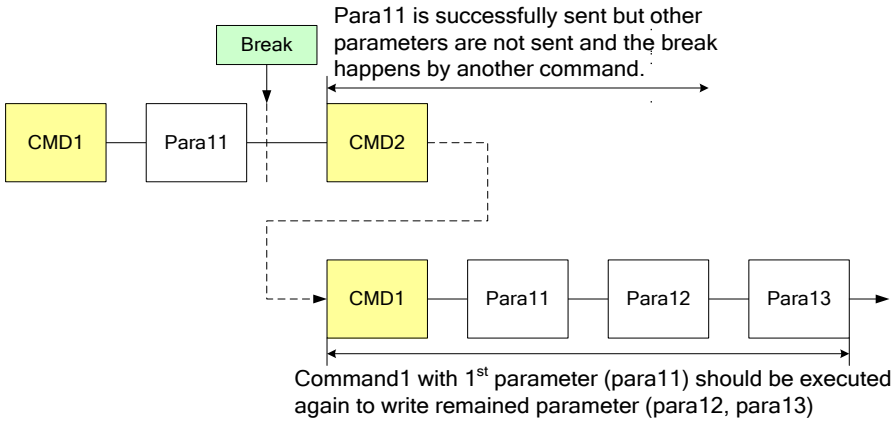


Figure 21 Write interrupts recovery (both serial and parallel Interface)

8.6 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the Chip Select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the Chip Select line is released after a whole byte of a command has been completed, then the display module will receive either the command‘s parameters (if appropriate) or a new command when the Chip Select line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command

2) Command-Pause-Parameter

3) Parameter-Pause-Command

4) Parameter-Pause-Parameter

8.6.1 Parallel interface pause

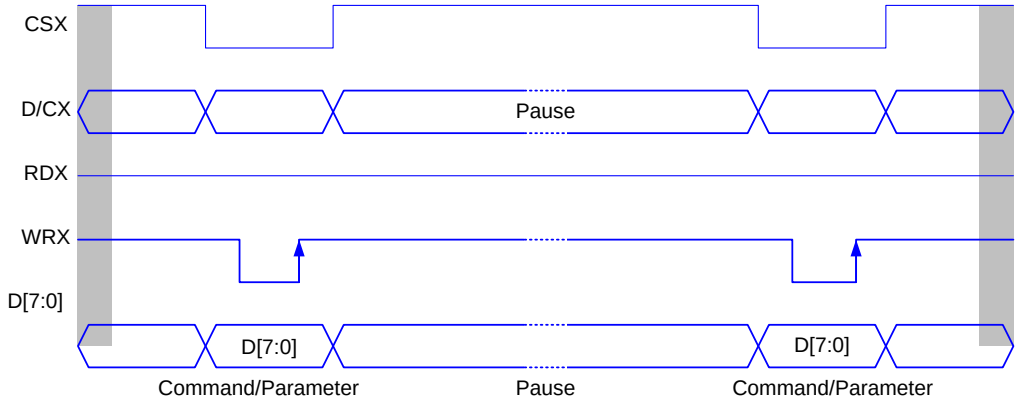


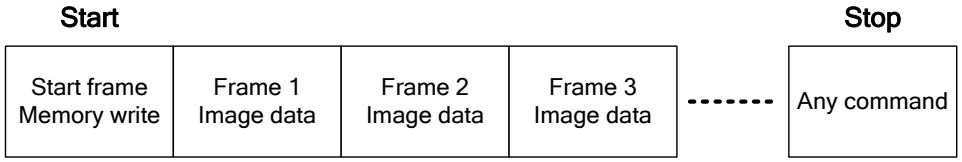
Figure 22 Parallel bus pause protocol (paused by CSX)

8.7 Data Transfer Mode

The module has two kinds color modes for transferring data to the display RAM. These are 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

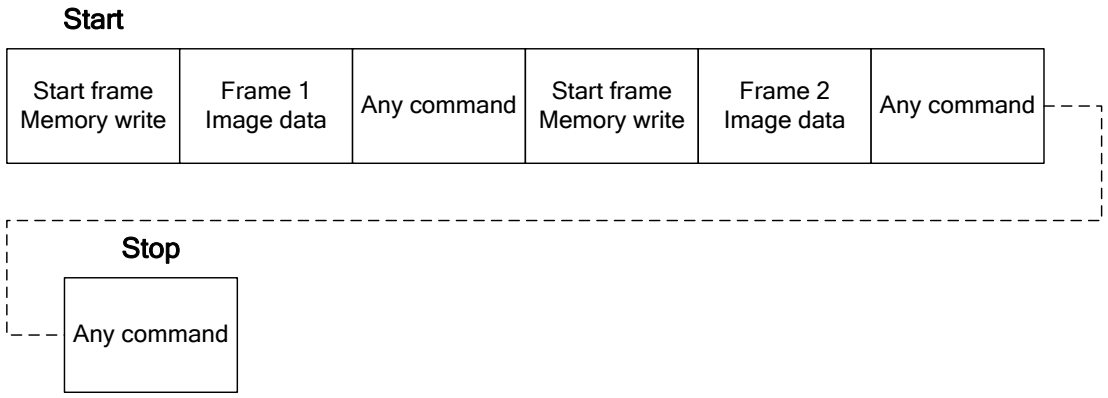
8.7.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



8.7.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

8.8 Data Color Coding

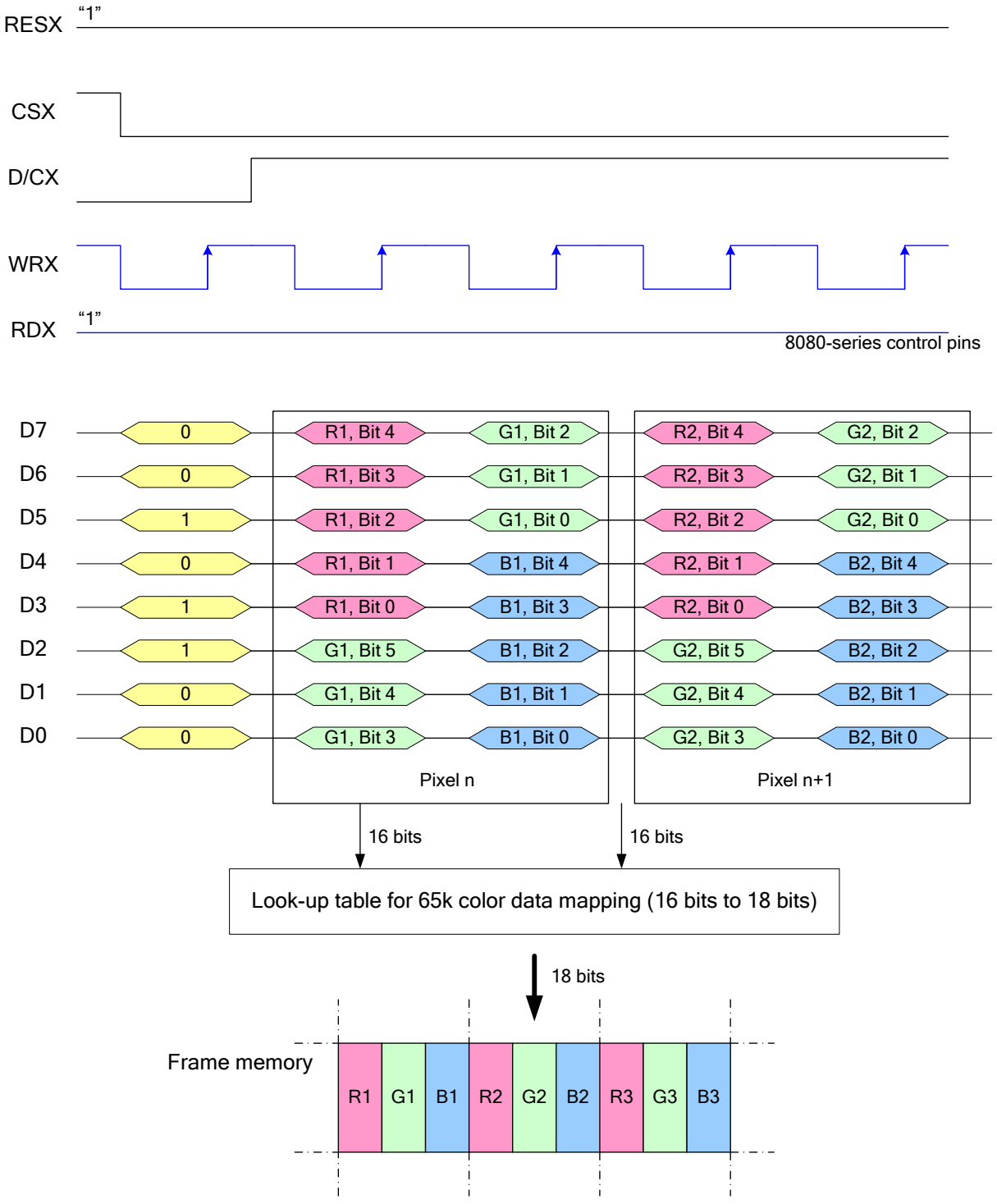
8.8.1 8080-Ⅰ series 8-bit Parallel Interface

The 8080-Ⅰ series 8-bit parallel interface of ST77916 can be used by setting IM[2:0]=”111b”. Different display data formats are available for two Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.8.1.1 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"

There is 1pixel (3 sub-pixels) per 2-byte



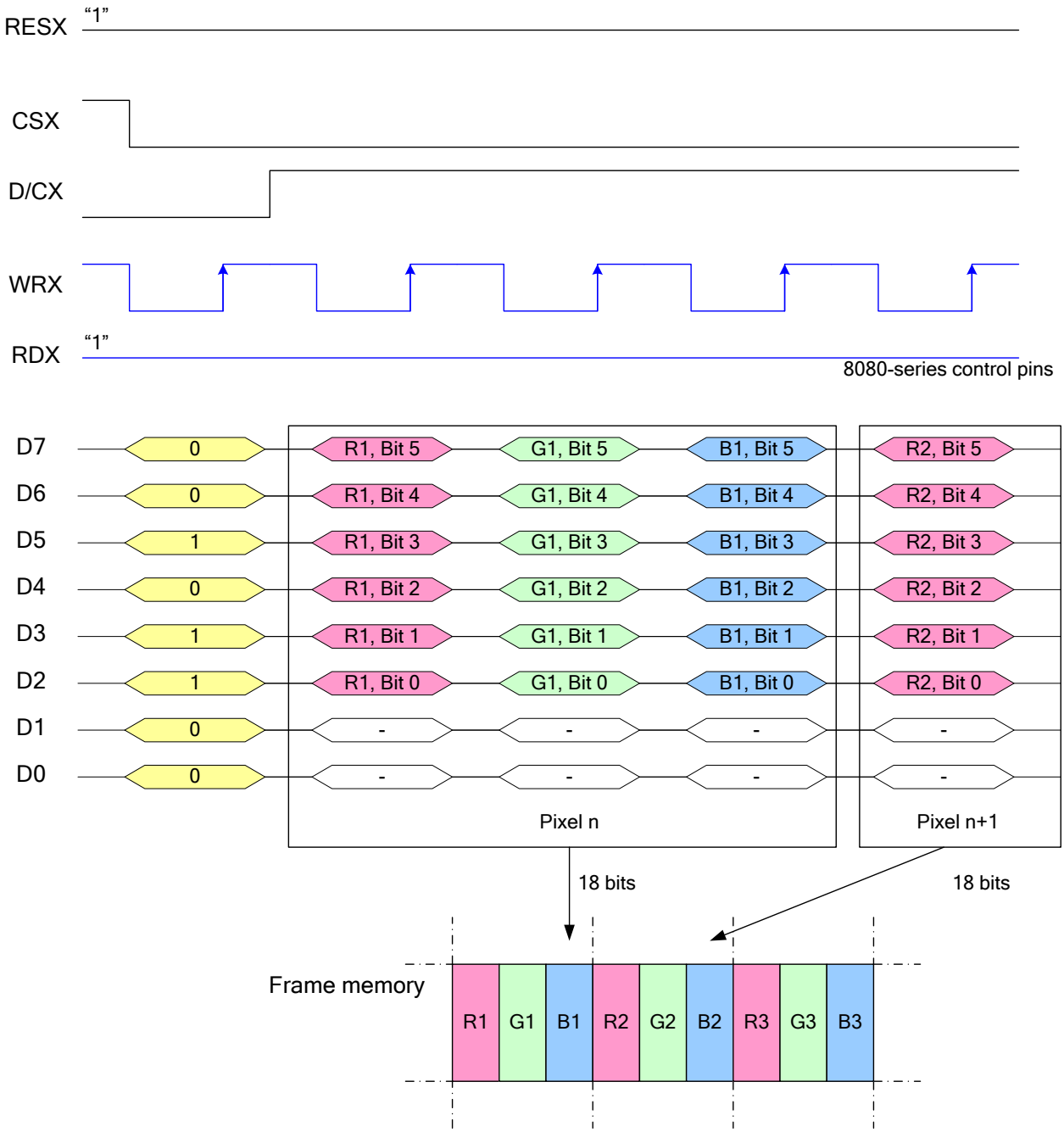
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

8.8.1.2 8-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"

There is 1pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

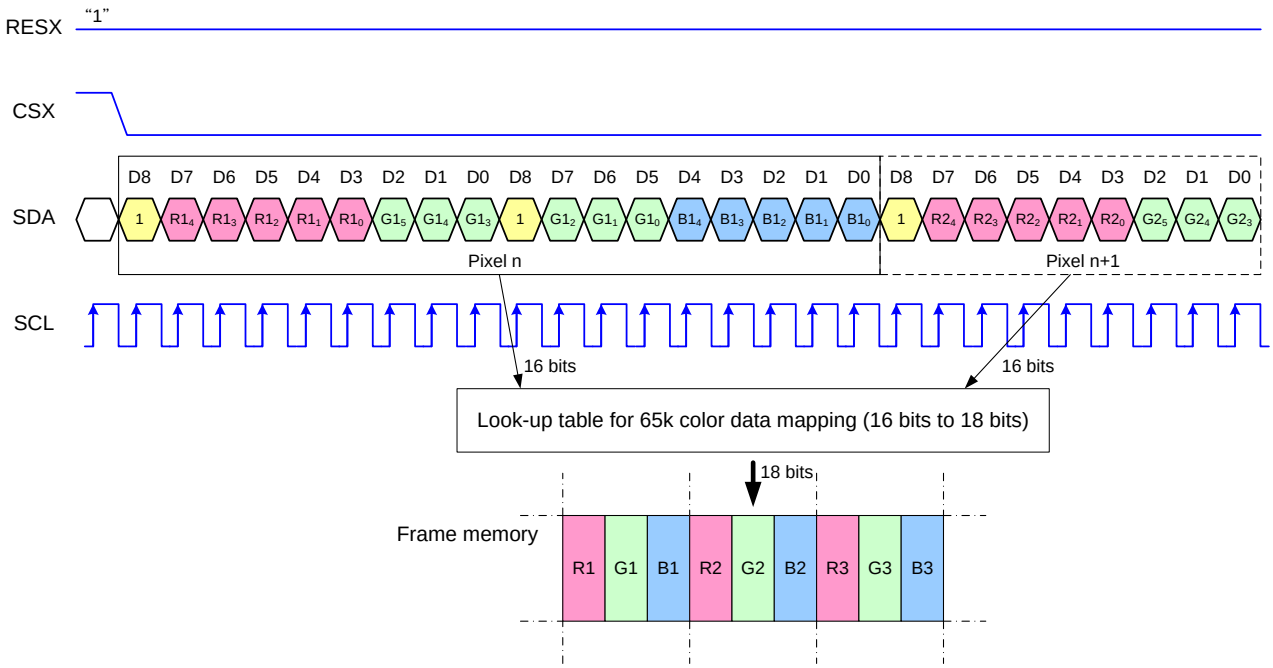
8.8.2 3-Line Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

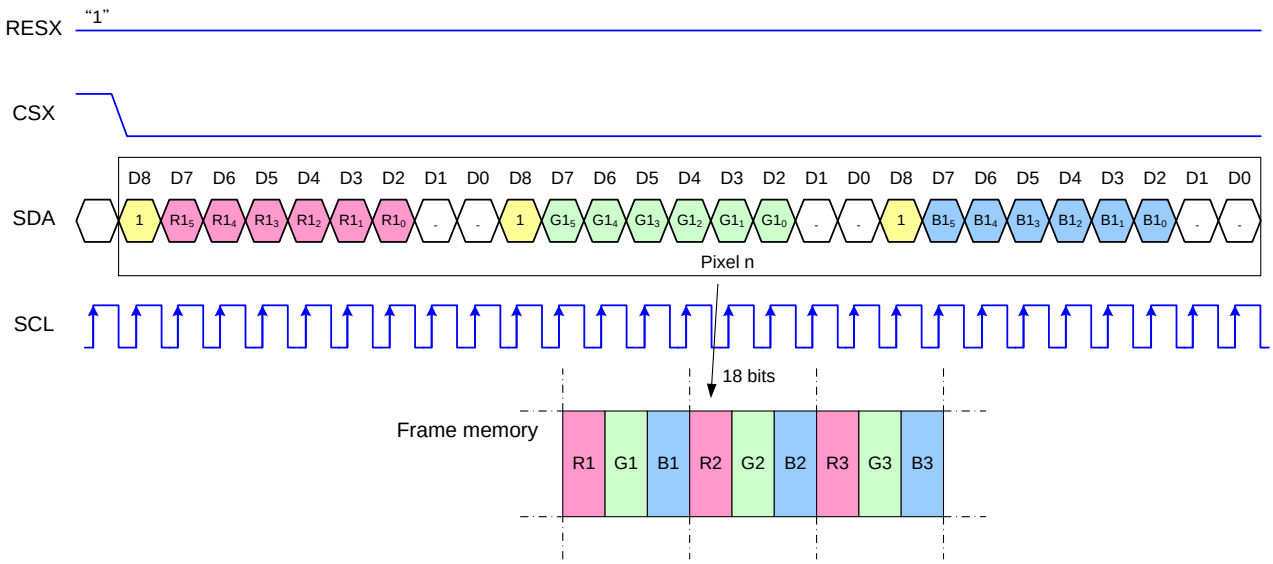
262k colors, RGB 6-6-6-bit input

8.8.2.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah=”05h”



Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.2.2 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah=”06h”



Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

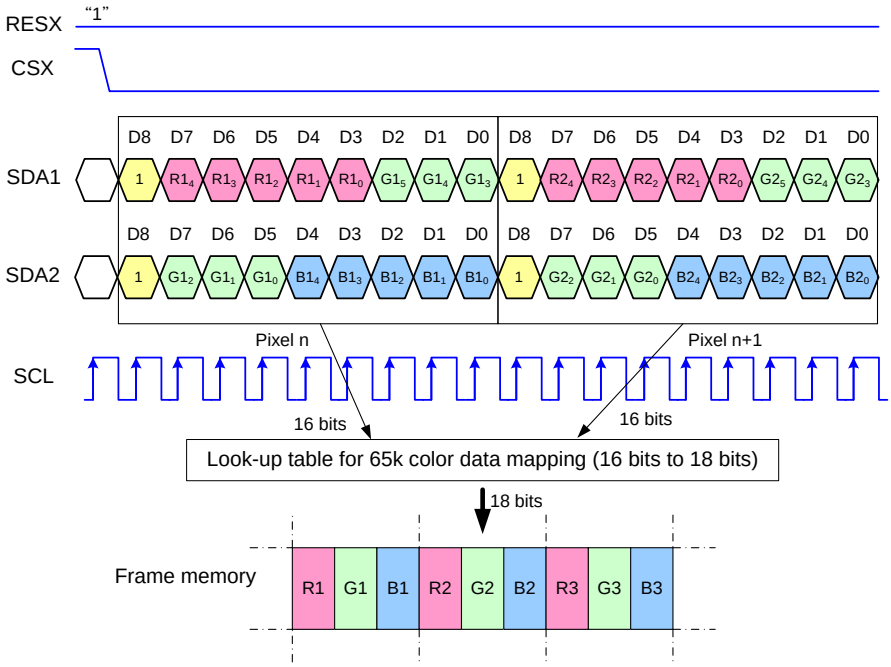
8.8.3 2 Data Lane Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

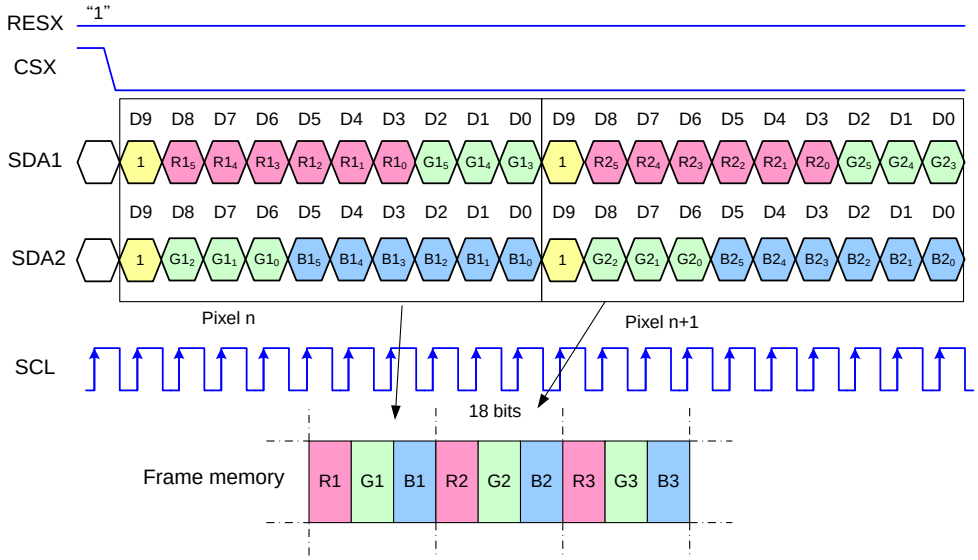
262k colors, RGB 6-6-6-bit input

8.8.3.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"



Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.3.2 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3Ah="06h"



Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

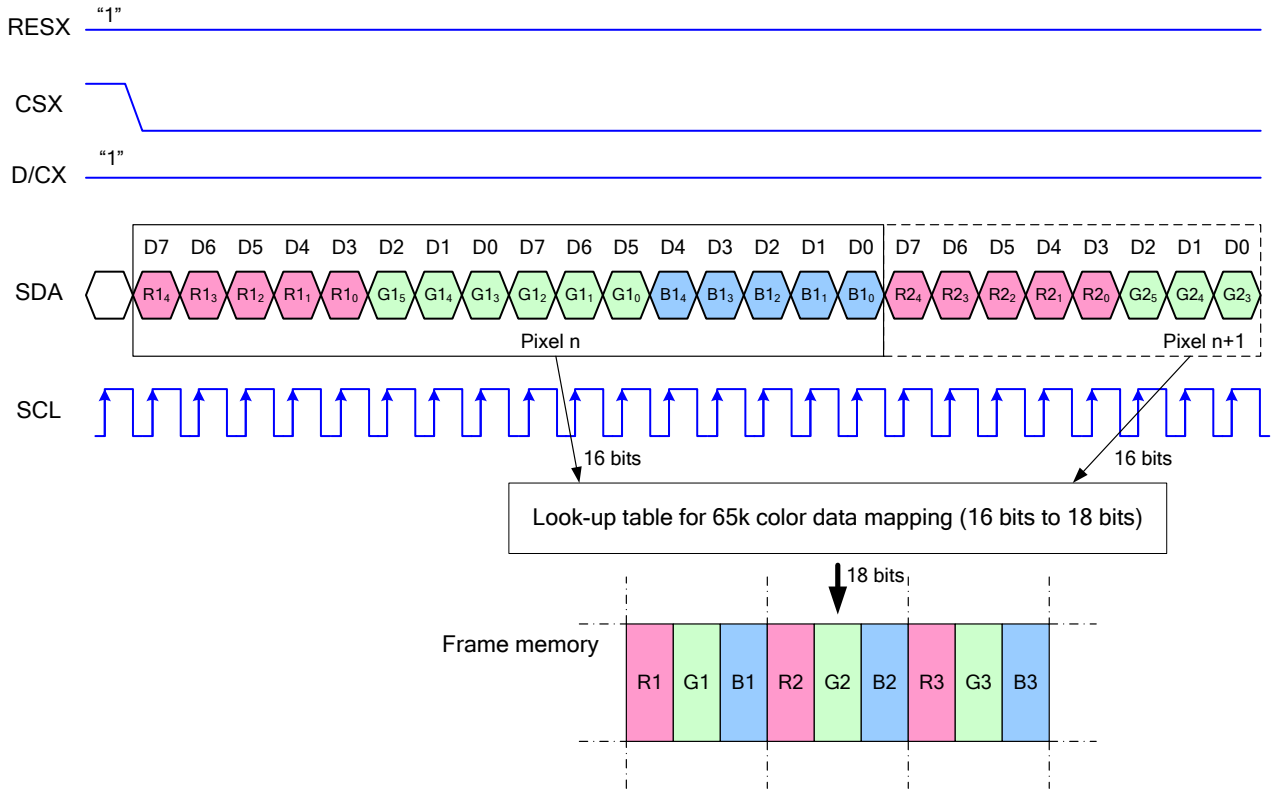
8.8.4 4-Line Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.8.4.1 Write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, 3Ah="05h"

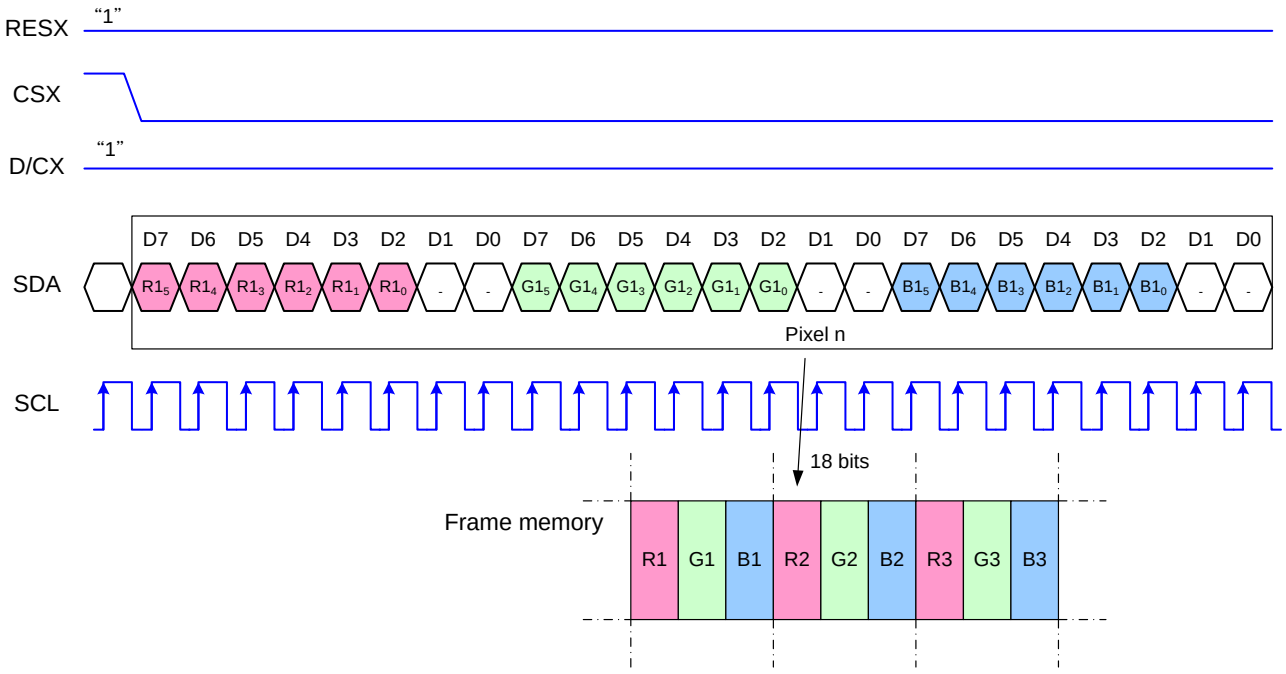


Note 1. Pixel data with the 16-bit color depth information

Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.8.4.2 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"



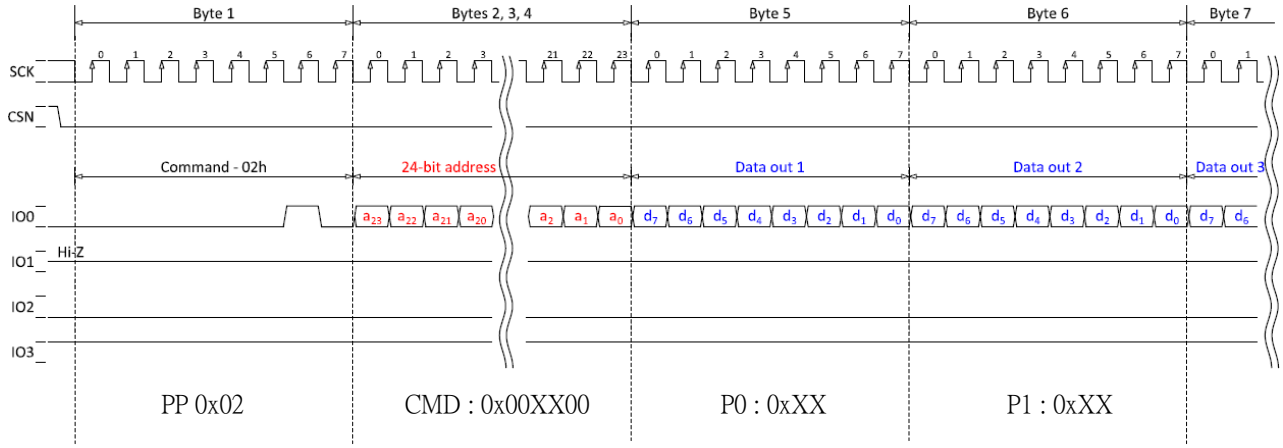
Note 1. Pixel data with the 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

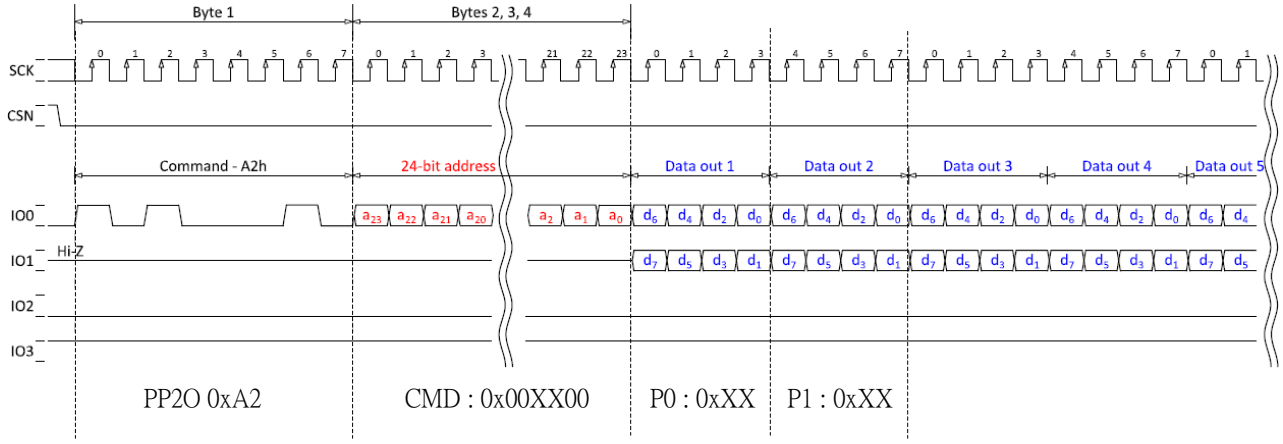
8.8.5 Quad-SPI Interface

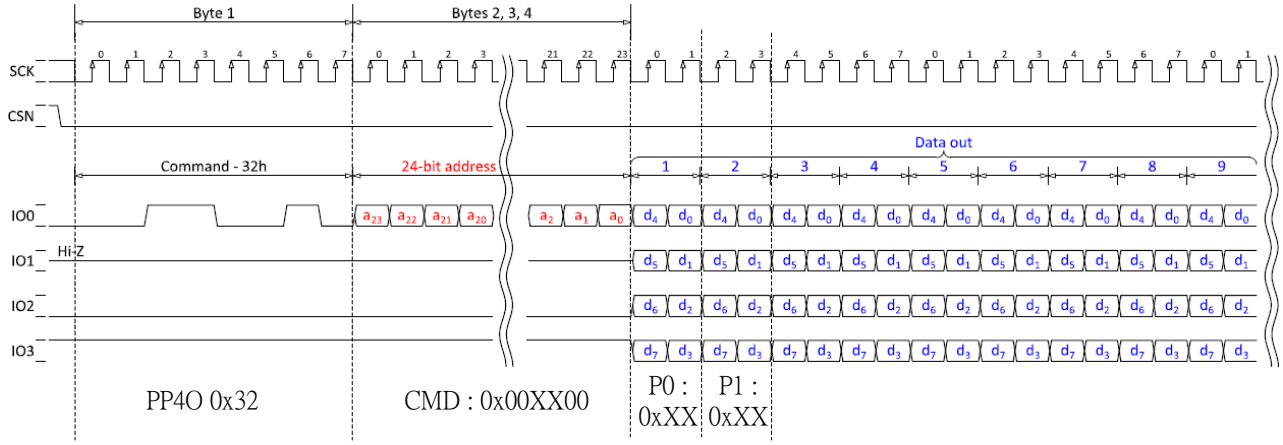
Pin Name	Description
CSXP	Chip selection signal
RDXP (SCLP)	Clock signal (Max=50MHz)
D0P	Serial input data lane 0
D1P	Serial input/output data lane 1
D2P	Serial input data lane 2
D3P	Serial input data lane 3

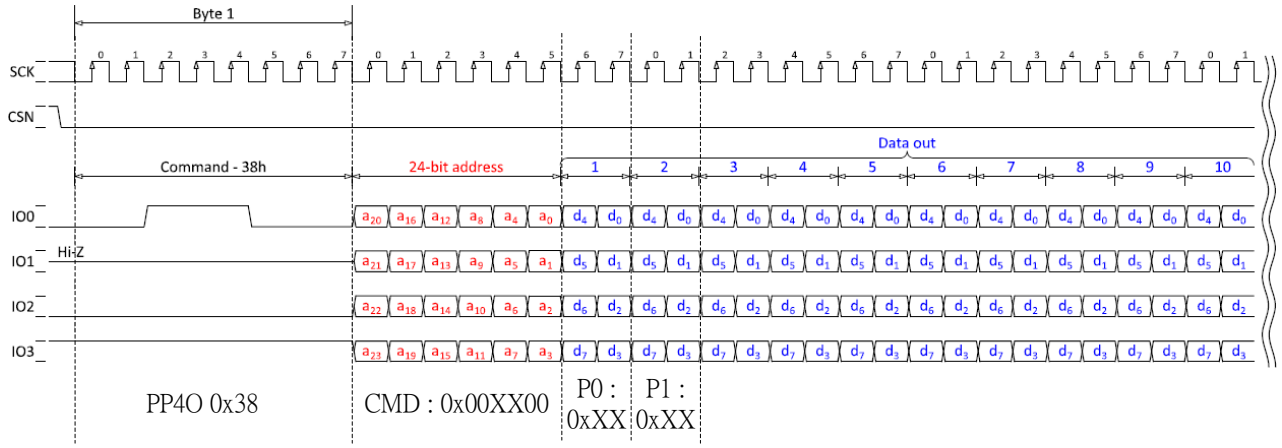
8.8.5.1 Command write mode:

When host writes commands or parameter to ST77916, host needs to send 1 byte of write command instruction (0x02、0xA2、0x32 or 0x38). Then host sends 3 bytes of AD[23:0] which is composed of 1 byte of 0x00, 1 byte of command address and 1 byte of 0x00. After host sending instruction and AD[23:0], the following data is parameter (are parameters). When the last bit of parameter has been sent, CSX pin should be returned “H” level.



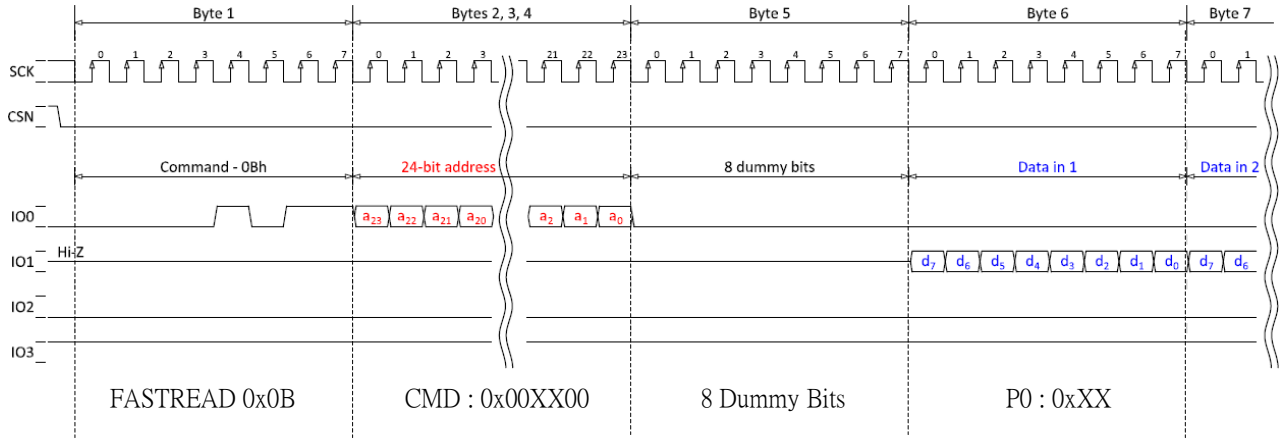






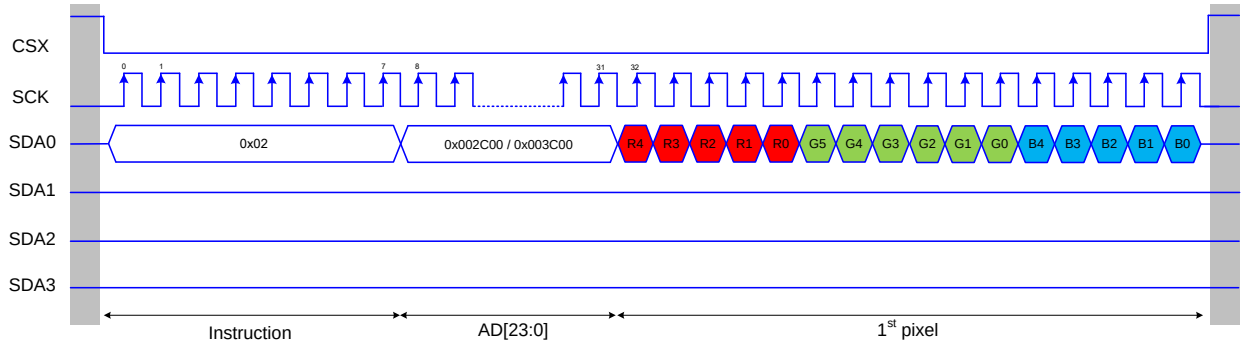
8.8.5.2 Read command mode

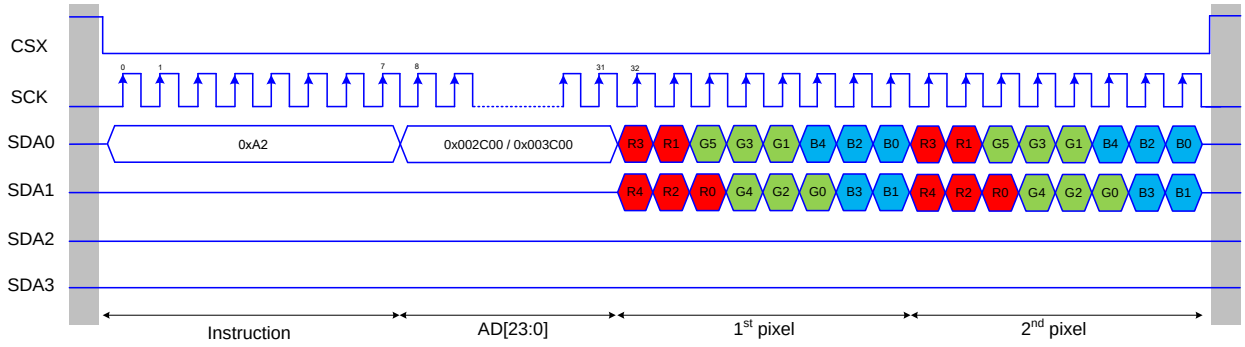
When host reads commands or parameter to ST77916, host needs to send 1 byte of write command instruction (0x0B). Then host sends 3 bytes of AD[23:0] which is composed of 1 byte of 0x00, 1 byte of command address and 1 byte of 0x00. After host sending read command and AD[23:0], the following output data is command address parameter (are parameters). When the last bit of parameter has been output, CSX pin should be returned “H” level.

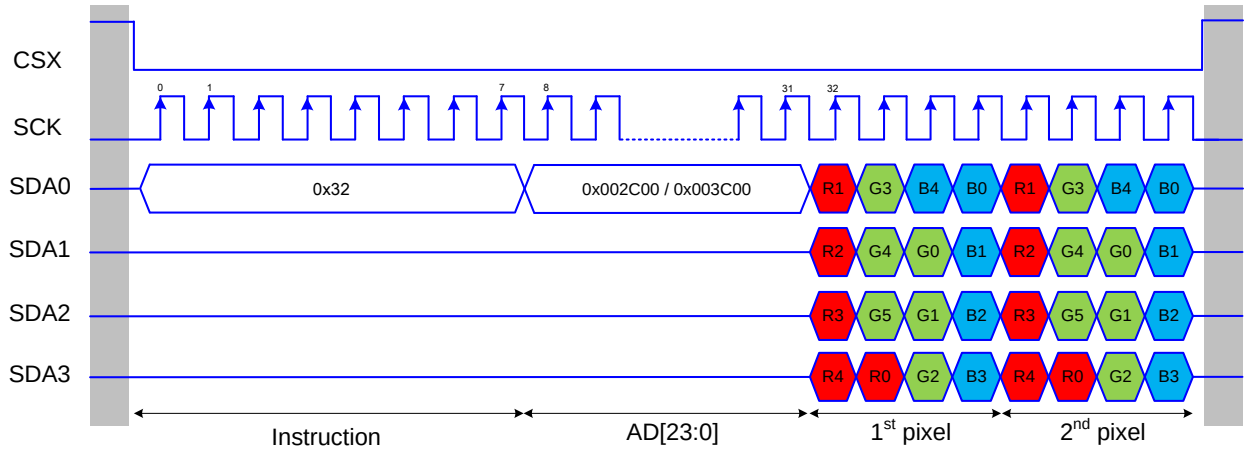


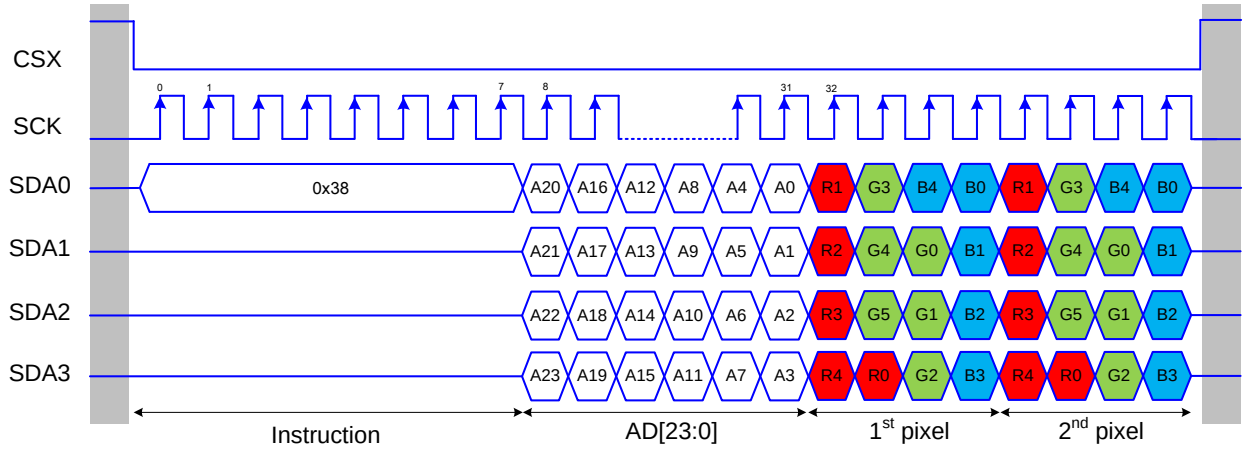
8.8.5.3 Color Format

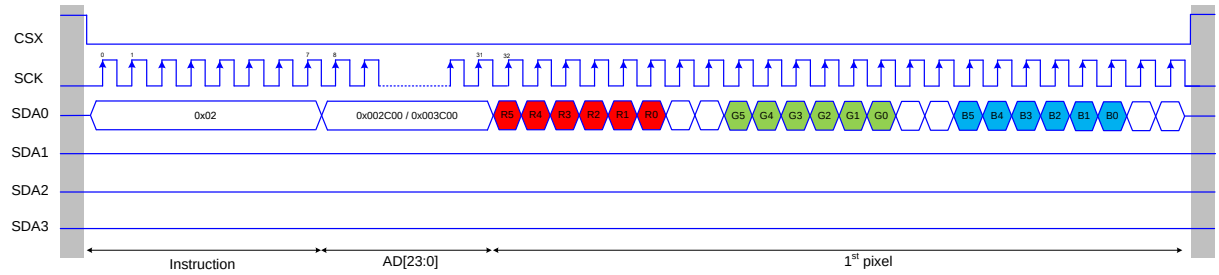
QSPI RGB565

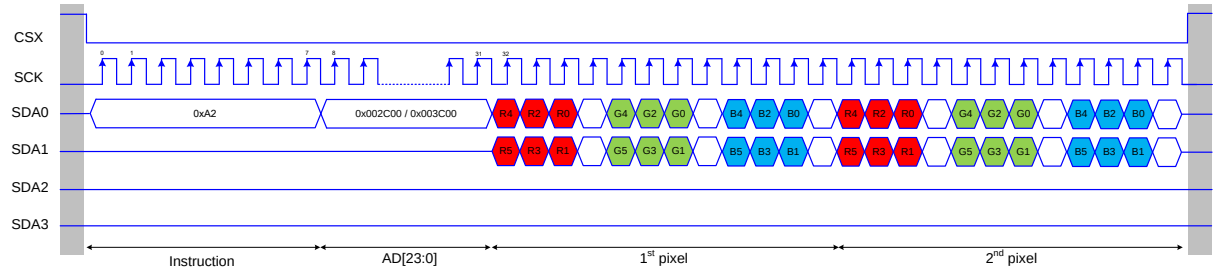


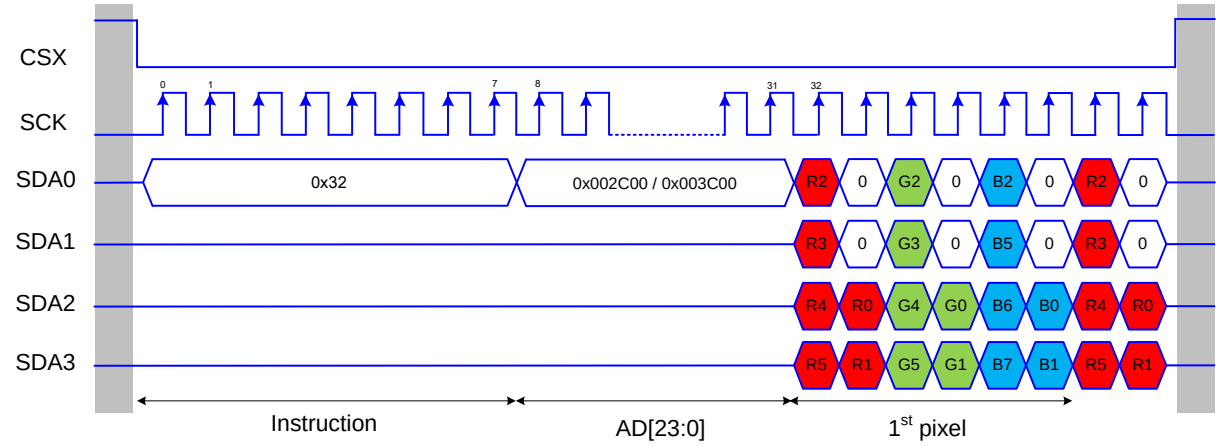


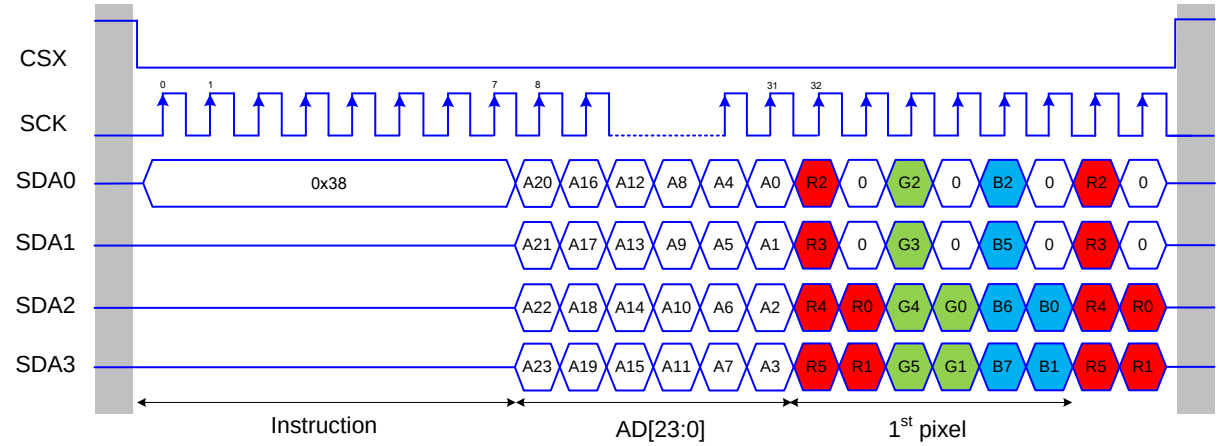












8.9 RGB Interface

8.9.1 RGB interface Selection

The color format selection of RGB Interface for ST77916 is selected by setting the command 3Ah, DB [6:4].

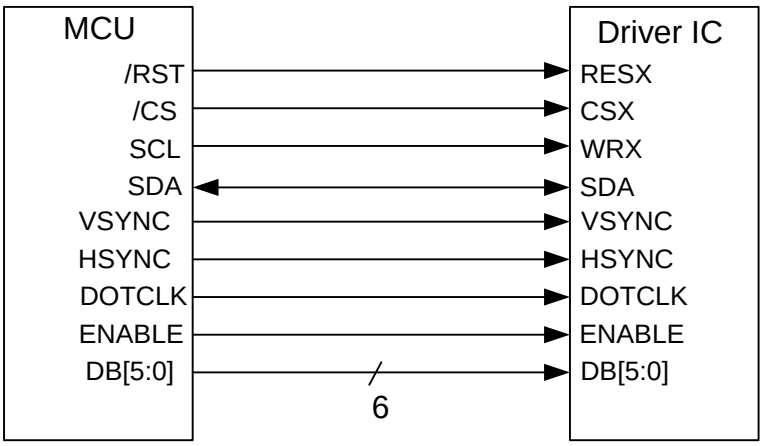
RGB Interface Mode	3Ah, DB[6:4]	Data pins
6-bit 262K RGB Interface	110	DB[5:0]
6-bit 65K RGB Interface	101	DB[5:0]

8.9.2 RGB Color Format

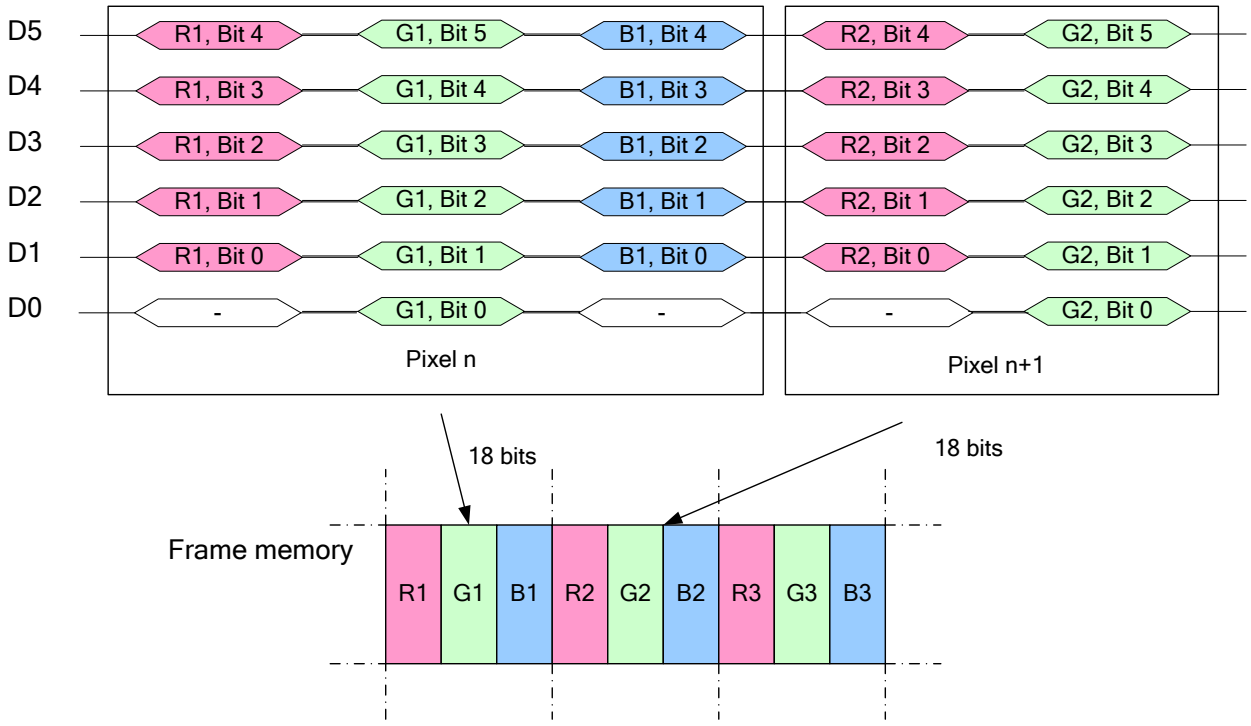
ST77916 supports two kinds of RGB interface, DE mode and HV mode, and 6bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[5:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[5:0] pins can be used. When using RGB interface, only serial interface can be selected.

6-bit RGB interface & 3-line serial interface hardware suggestion, IM[2:0]=100.
6-bit RGB interface & 4-line serial interface hardware suggestion, IM[2:0]=101.

6-bit RGB Interface



Write data for 6-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



Write data for 6-bit/pixel (RGB 6-6-6-bit input), 262K-Colors

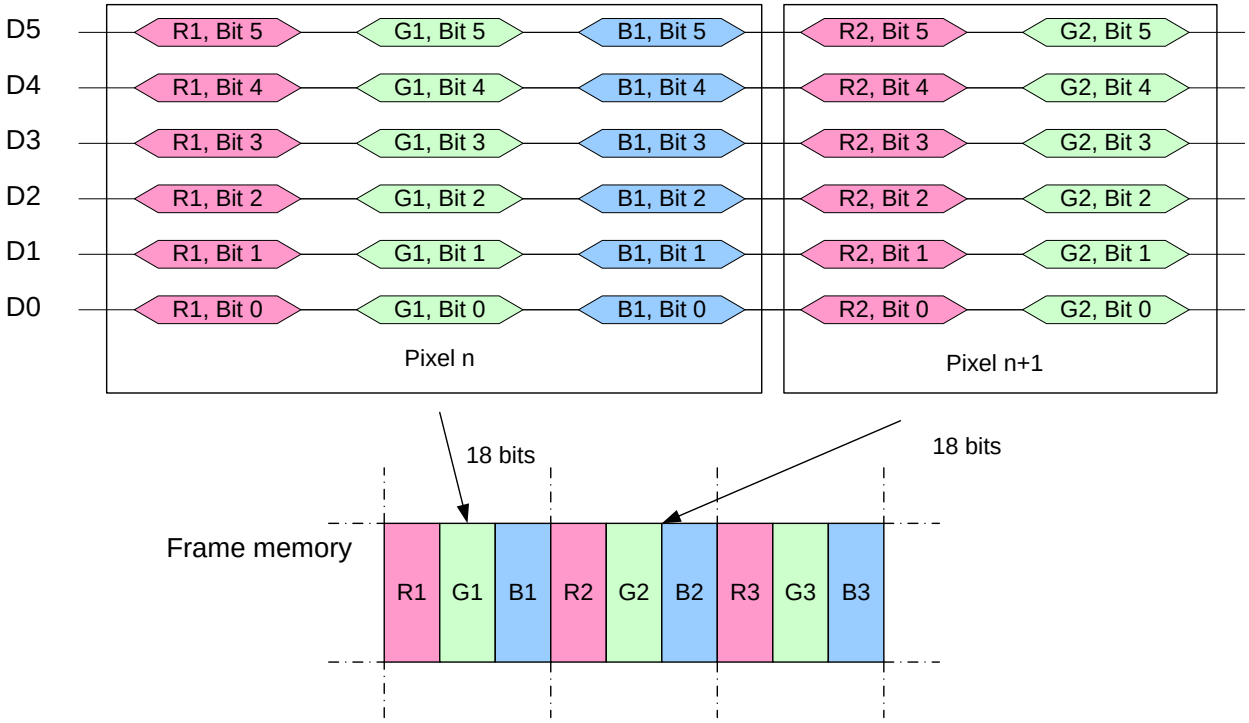


Figure 23 RGB Interface Data Format

8.9.3 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

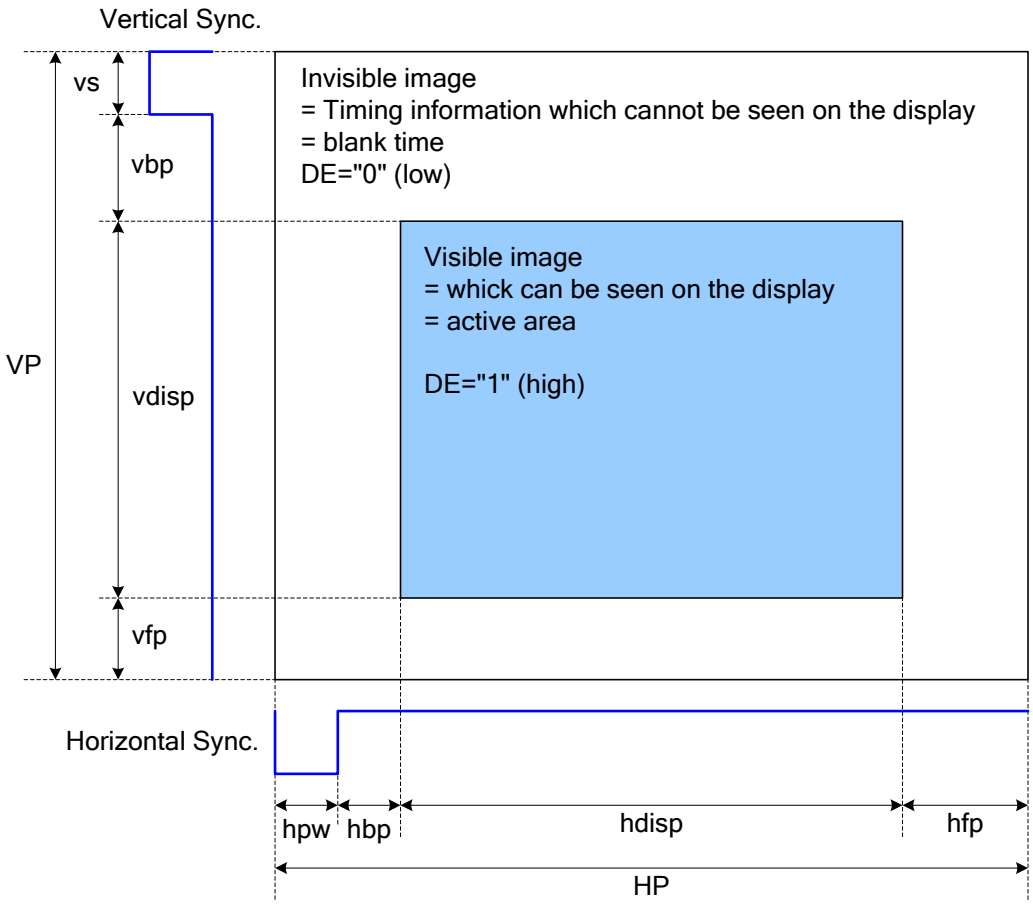


Figure 24 DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

6bit RGB interface:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	6	30	hpw+hbp=93	Clock
Horizontal Sync. Back Porch	hbp	12	30		Clock
Horizontal Sync. Front Porch	hfp	6	60	-	Clock
Vertical Sync. Width	vs	2	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

Note:

Typical value are related to the setting of dot clock is 17MHz and frame rate is 60Hz, VDD=VDDI=2.8V..

In with ram mode, hpw+hbp+hfp≧66

In without ram mode, hpw+hbp≧60

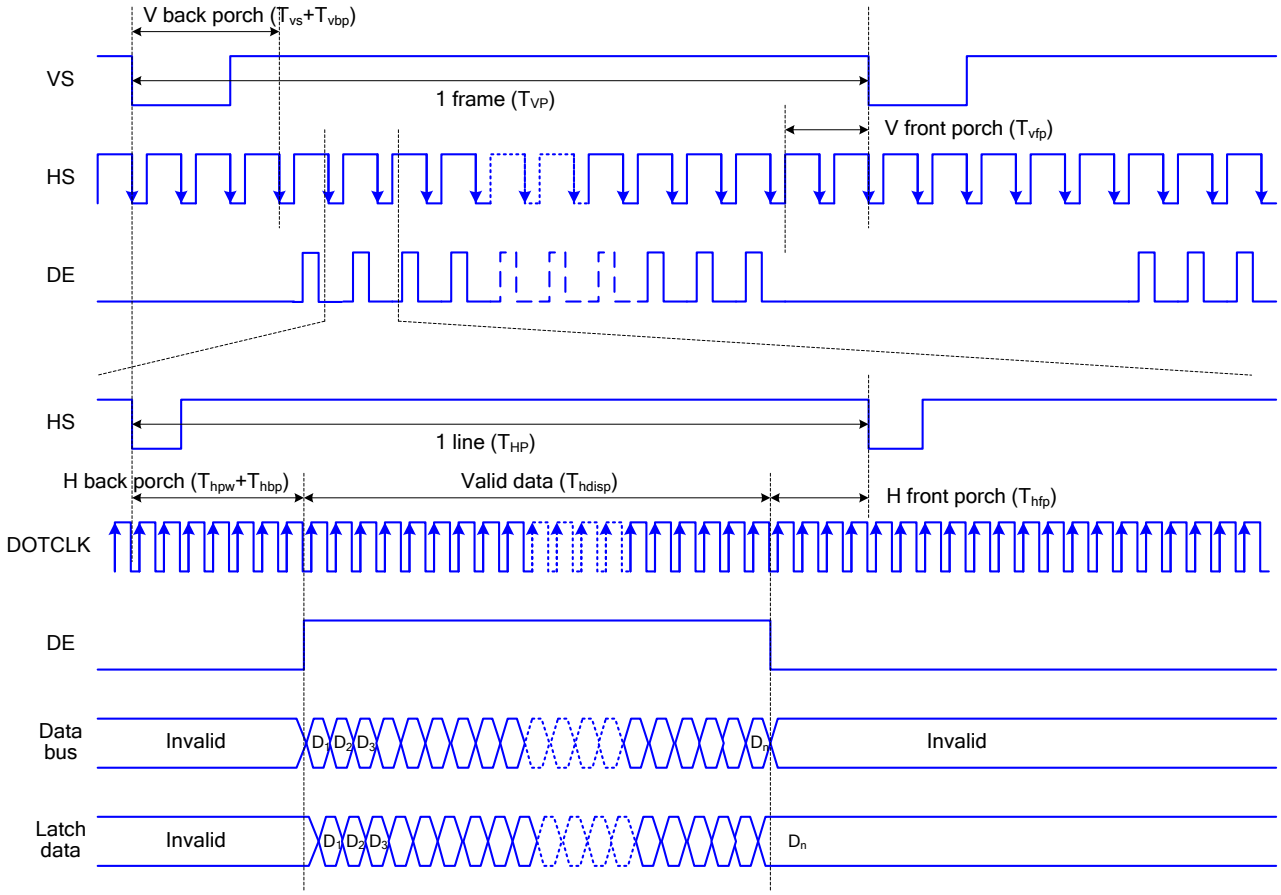
8.9.4 RGB Interface Mode Selection

ST77916 supports two kinds of RGB interface, DE mode and HV mode. Each mode also can select with ram and without ram. The table shown below uses command BDh, DB[7] to select with ram and without ram.

RCM	RGB Mode	WO	Data Path
0	DE mode	0	Ram
		1	Shift register (without Ram)
1	HV mode	0	Ram
		1	Shift register (without Ram)

8.9.5 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 25 Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.

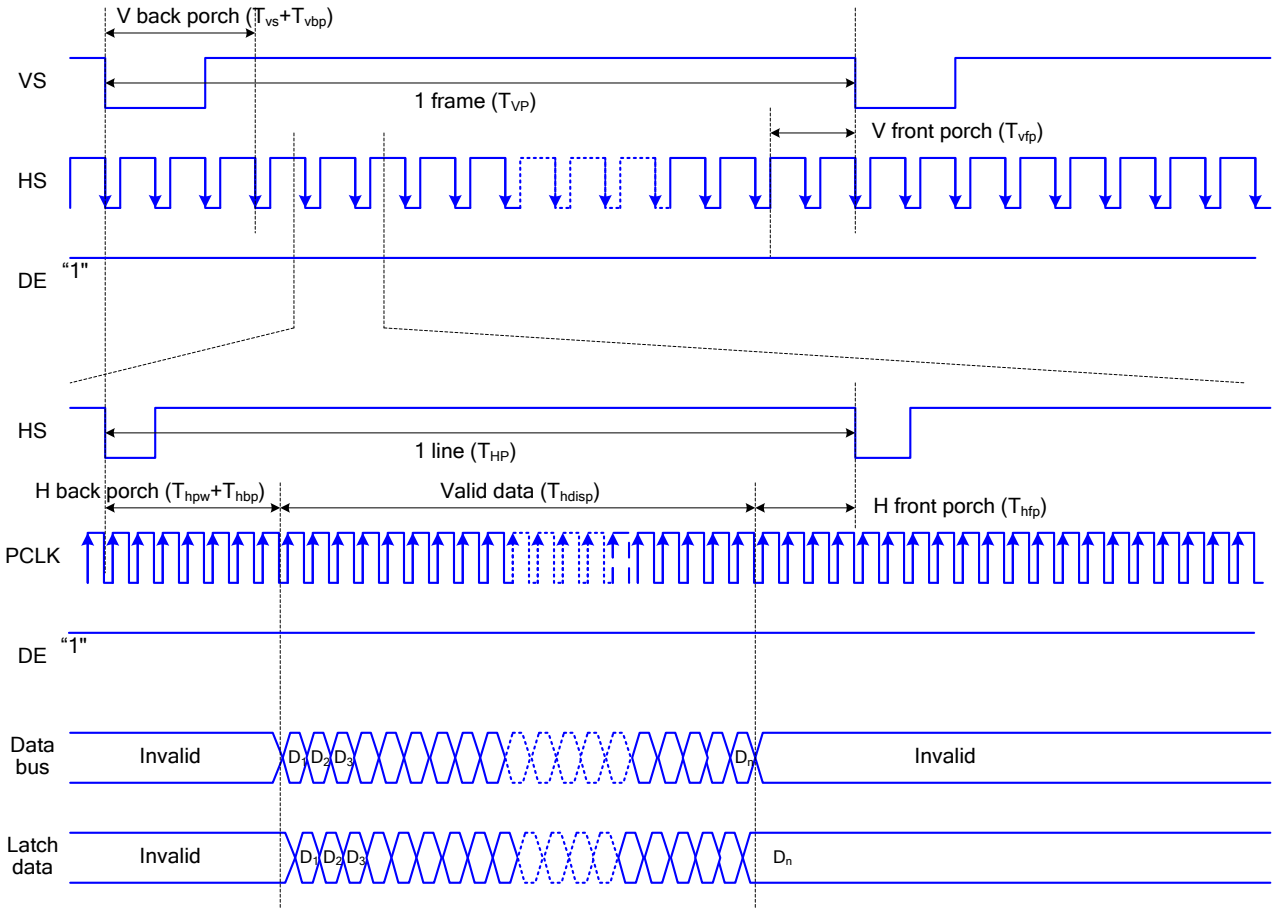


Figure 26 Timing chart of RGB interface HV mod

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

8.10 Mobile Industry Processor Interface (MIPI)

8.10.1 Display Serial Interface (DSI)

1.1.1.1 GENAL DESCRIPTION

The communication can be separated 2 different levels between the MCU and the display module:

1. Low level communication what is done on the interface level
2. High level communication what is done on the packet level

1.1.1.2 Interface Level Communication

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocols in each mode when there wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark – 0
LP-10	High (LP)	Low (LP)	Not Defined	LP – Request	Mark – 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

(1) Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

(2 If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

1.1.1.3 DSI-CLOCK Lanes

DSI-CLOCK_P/N lanes can be driven into three different power modes:

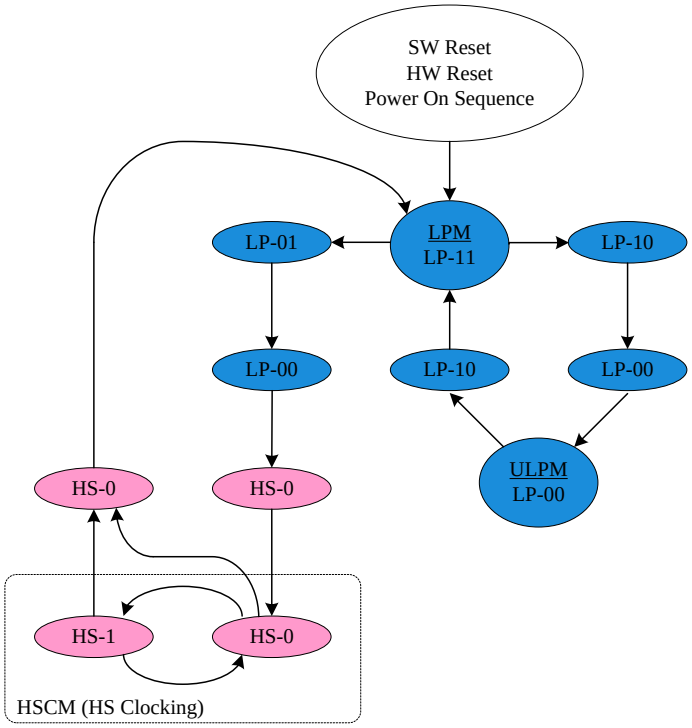
- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)
- High Speed Clock Mode (HSCM)

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power

Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

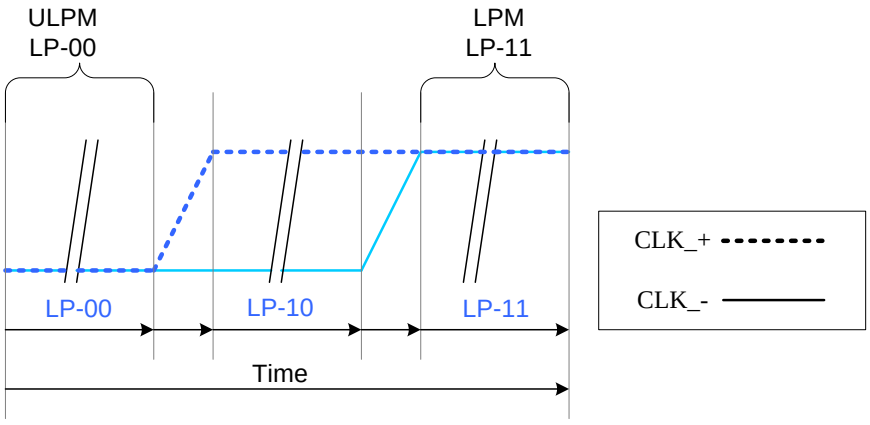


Flow chart of the different clock lanes

1. Low Power Mode (LPM)

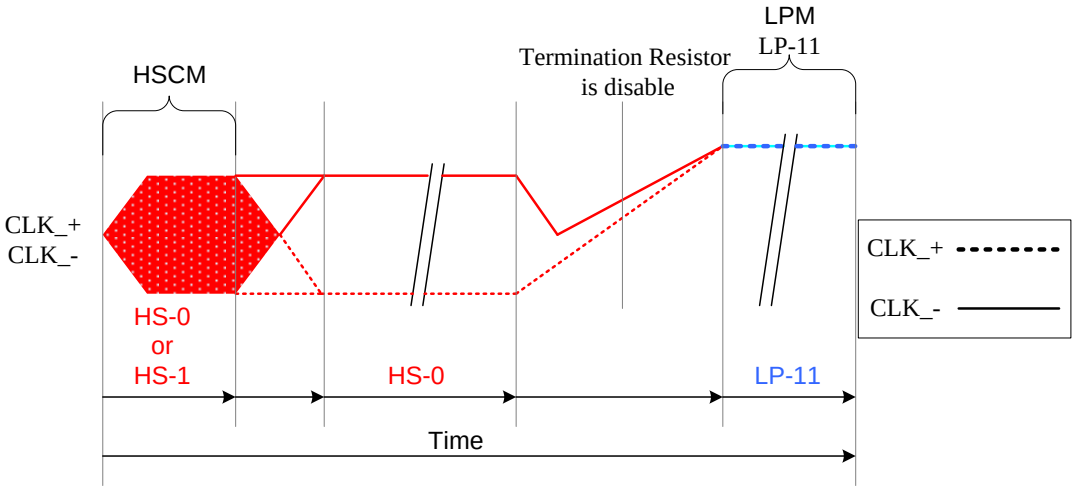
DSI-CLOCK_P/N lanes can be driven to the Low Power Mode (LPM), when DSI-CLOCK lanes are entering LP-11 State Code, in three different ways:

- After SW Reset, HW Reset or Power On Sequence =>LP-11 After DSI-CLOCK_P/N lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10
- LP-11 (LPM). This sequence is illustrated below.



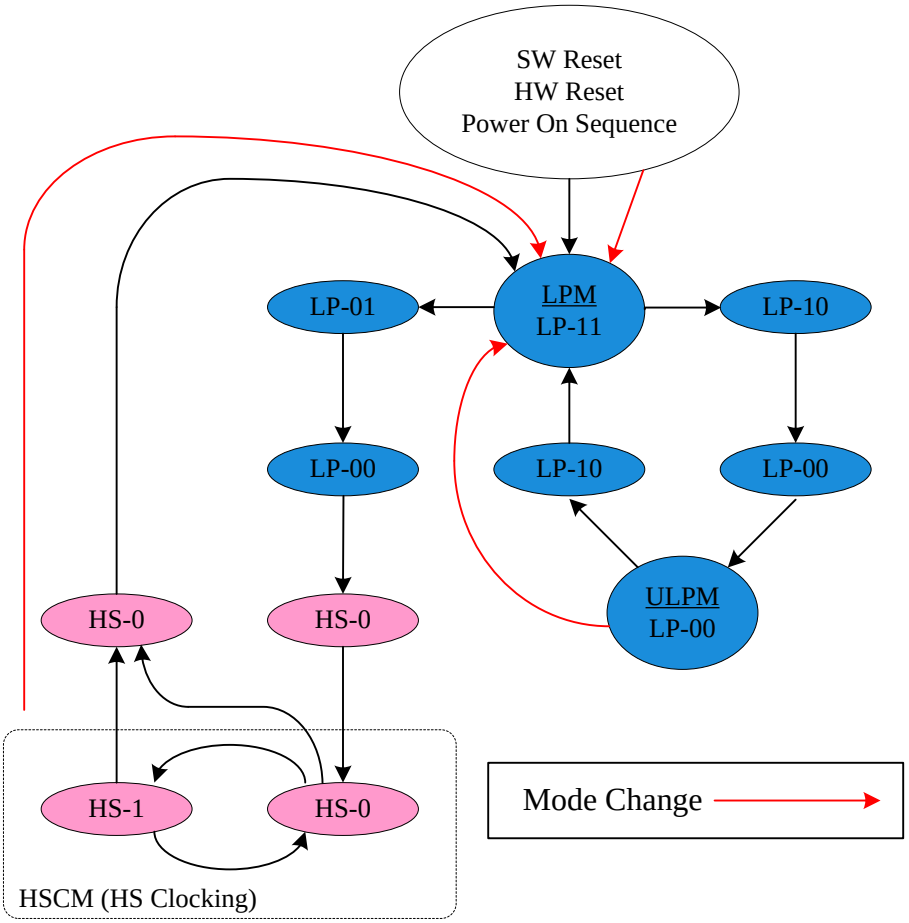
From ULPM to LPM

- After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.



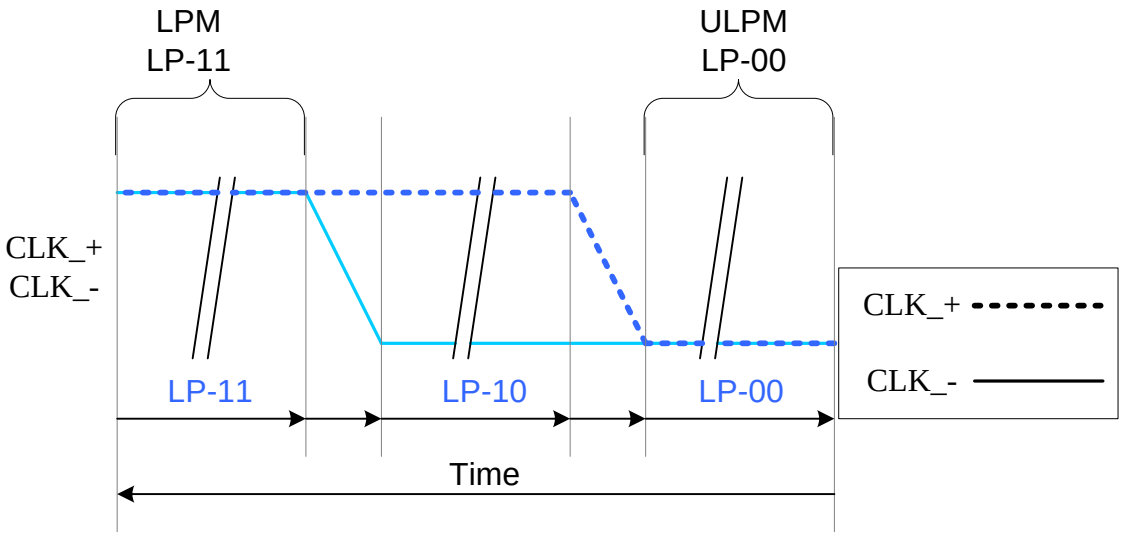
From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.



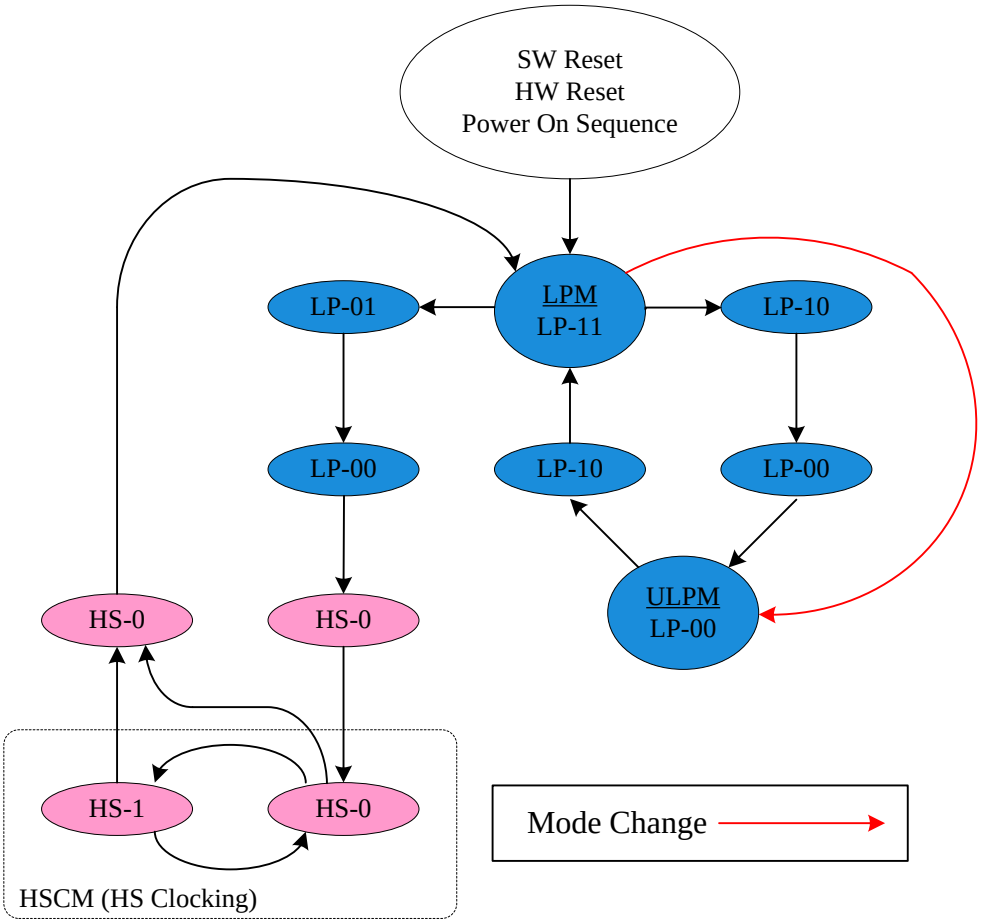
All Three Mode Changes to LPM on the Flow Chart

2. Ultra Low Power Mode (ULPM)



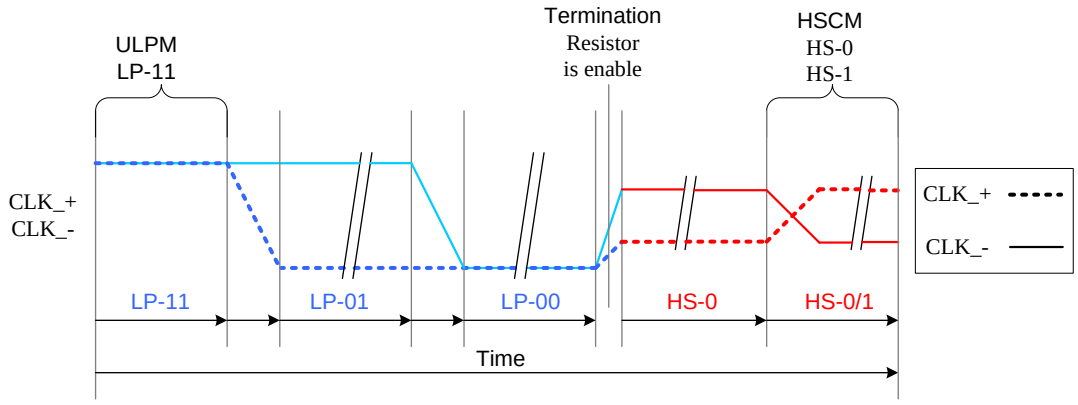
From LPM to ULPM

The mode change is also illustrated below.



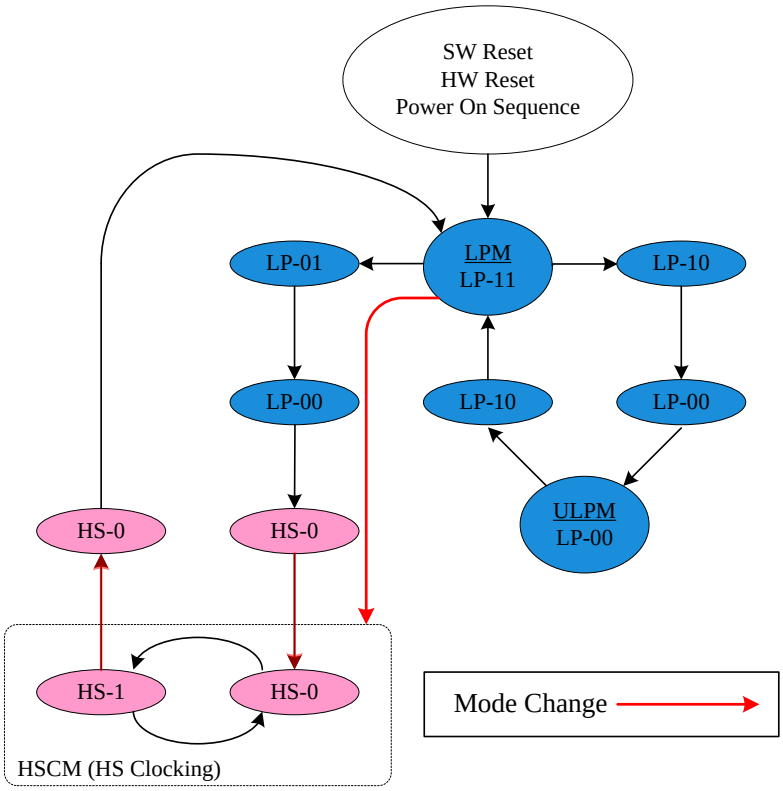
Mode Change from LPM to ULPM on the Flow Chart

3. High Speed Clock Mode (HSCM)



From LPM to HSCM

The mode change is also illustrated below.

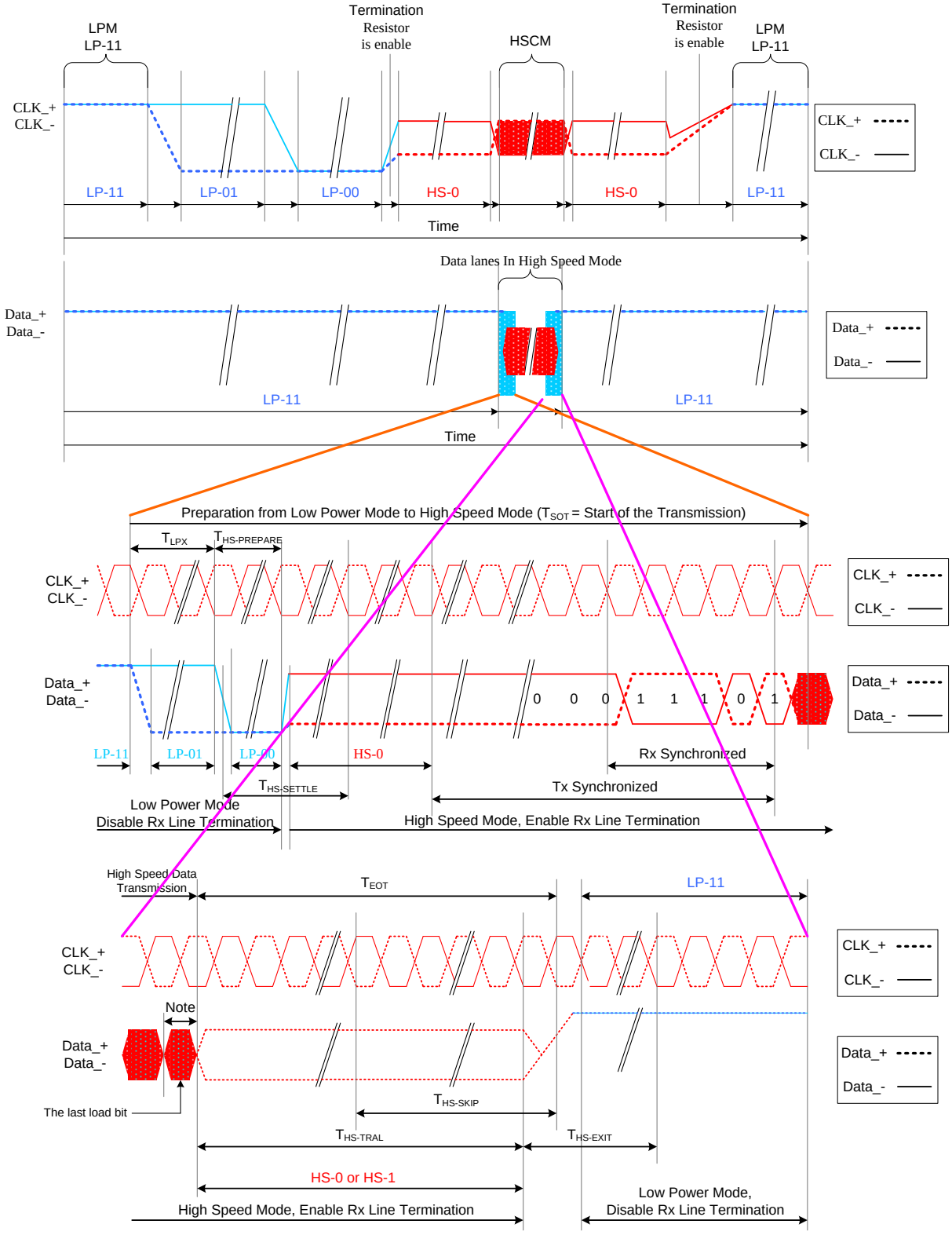


Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLOCK_P/N) is started before high speed data is sent via DSI-DATA_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



High Speed Clock Burst

Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0

1.1.1.4 DSI-DATA Lanes

DSI-DATA_P/N Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP-11(Mark-1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z, Note

1. **Escape Mode**

Data lanes (DSI-DATA_P/N) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

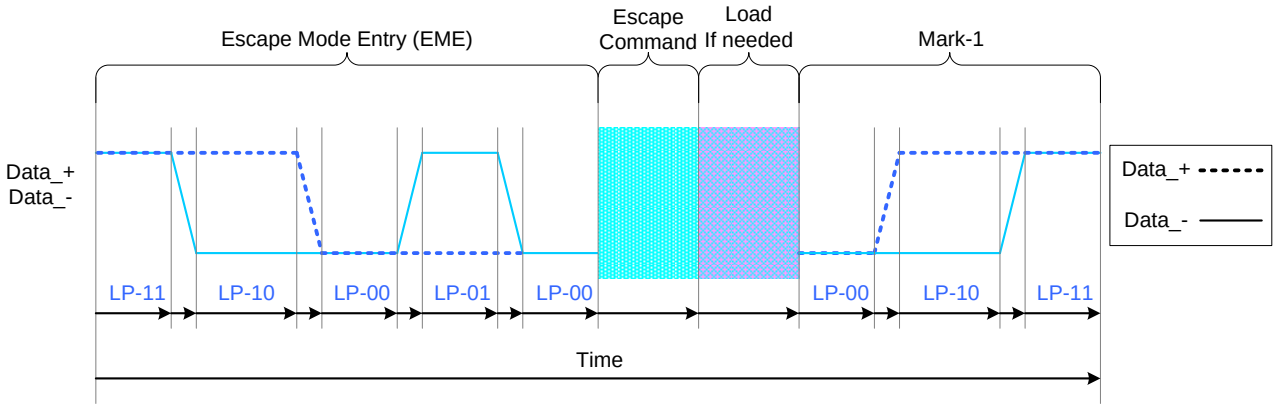
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is reset the display module
- Indicate “Tearing Effect”, which is used for a TE line event from the display module to the MCU
- Indicate (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different Escape Commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (RX_D0P/N) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module an event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.
Escape commands are defined on the next table.

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Last Bit Transmitted)
Low-Power Data	Mode	1110 0001 b
Ultra-Low Power Mode	Mode	0001 1110 b
Undefined-1, Note	Mode	1001 1111 b
Undefined-2, Note	Mode	1101 1110 b
Remote Application Reset	Trigger	0110 0010 b
Tearing Effect	Trigger	0101 1101 b
Acknowledge	Trigger	0010 0001 b
Uknown-5, Note	Trigger	1010 0000 b

Note: This Escape command support has not been implemented on the display module.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

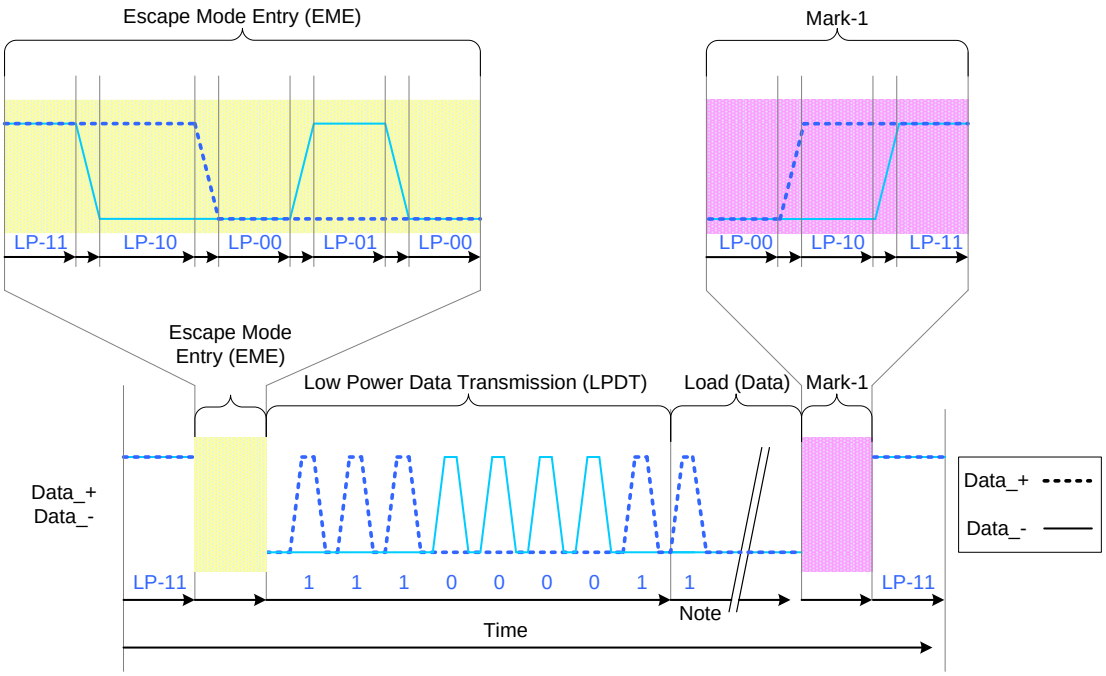
- Start: LP-11

- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):

  One or more bytes (8 bit)

  Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

The Low-Power Data Transmission (LPDT) is as below,



Note : Load (Data) is presenting that the first bit is logical “1” in this Exsample

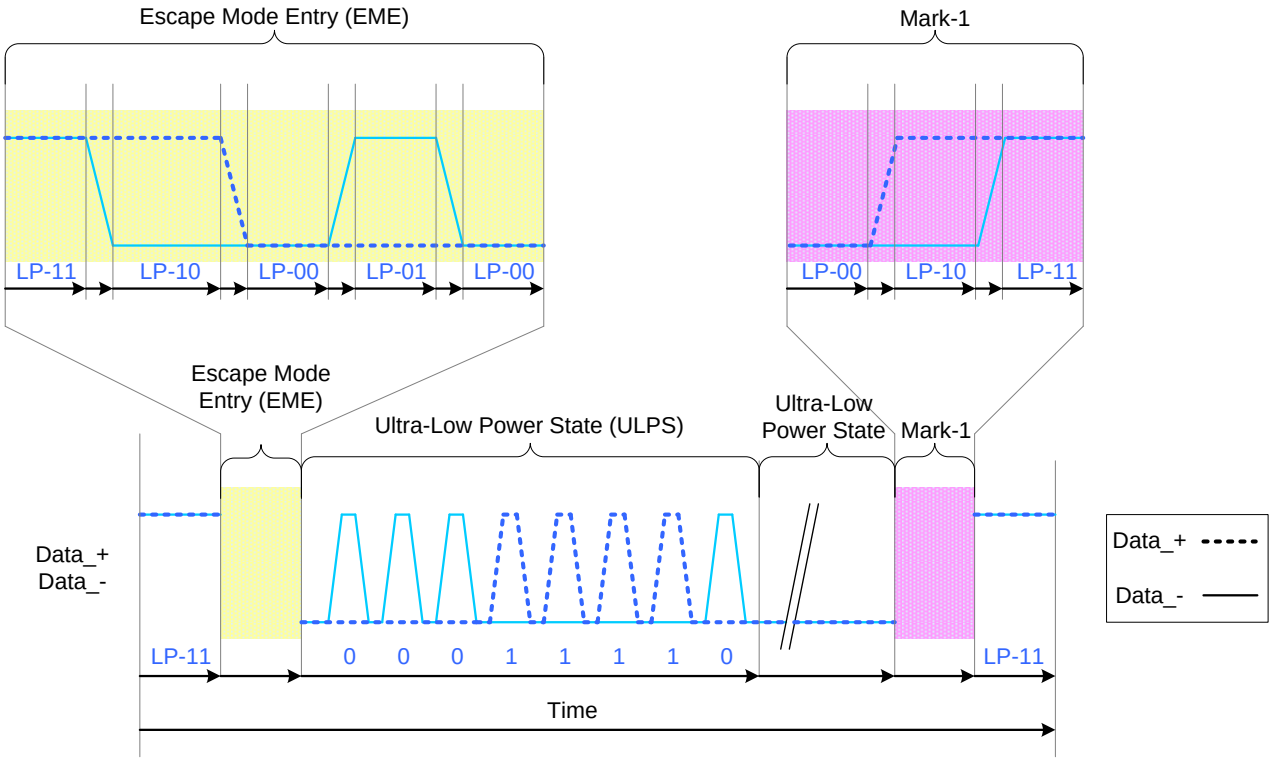
Low-Power Data Transmission (LPDT)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode. The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Ultra-Low Power State (ULPS)

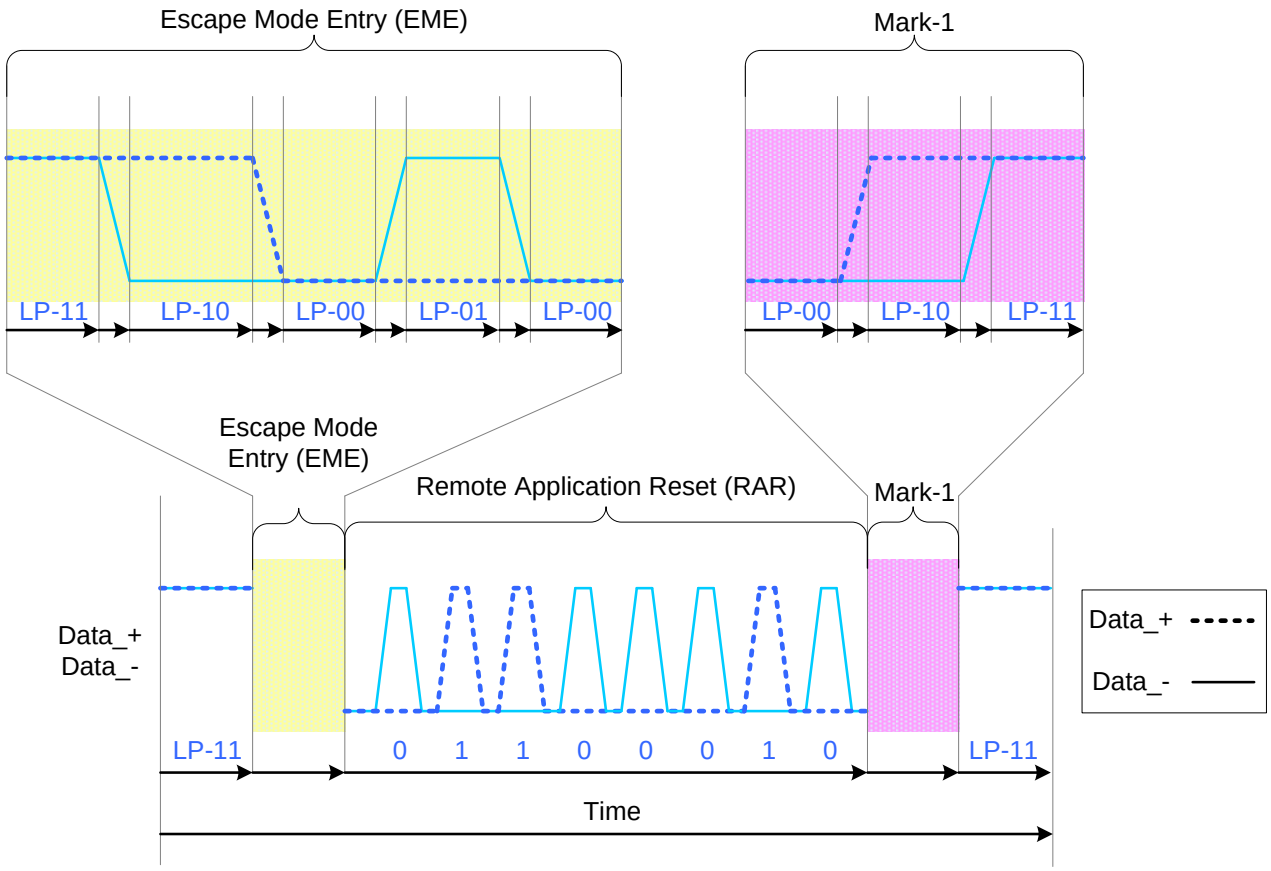
Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

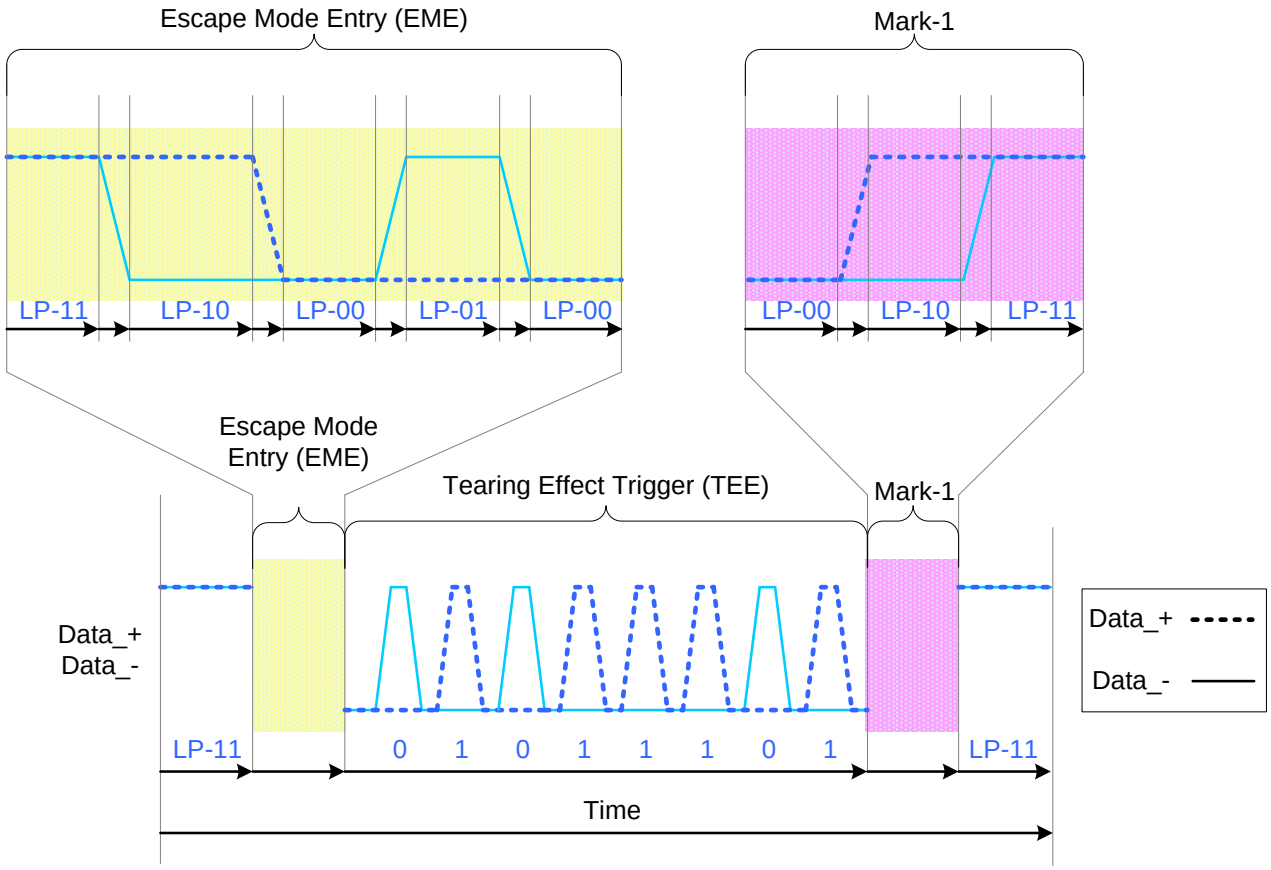
Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been appened on the display module by Tearing Effect (TEE).

The display module is sending the Tearing Effect (TEE) what is a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Tearing Effect (TEE)

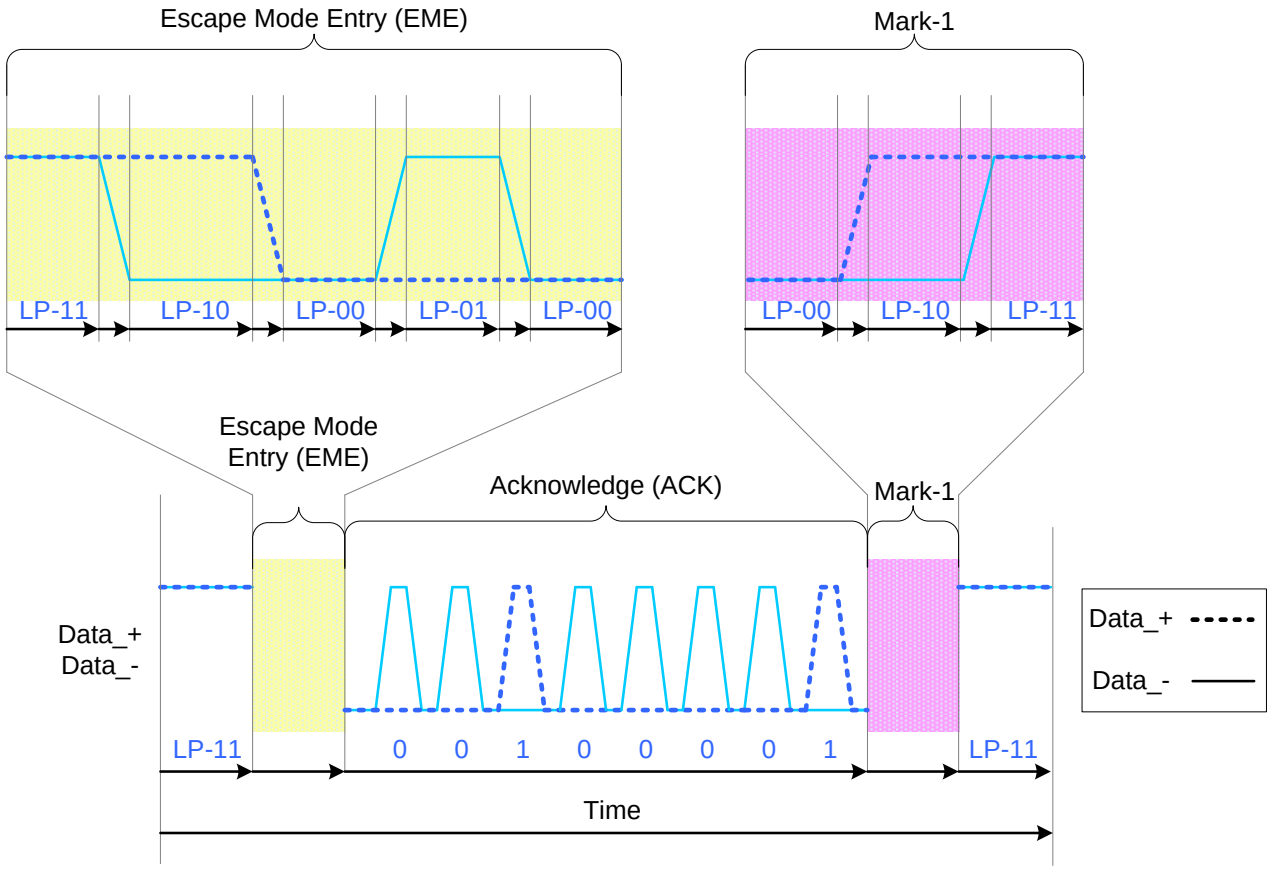
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Acknowledge (ACK)

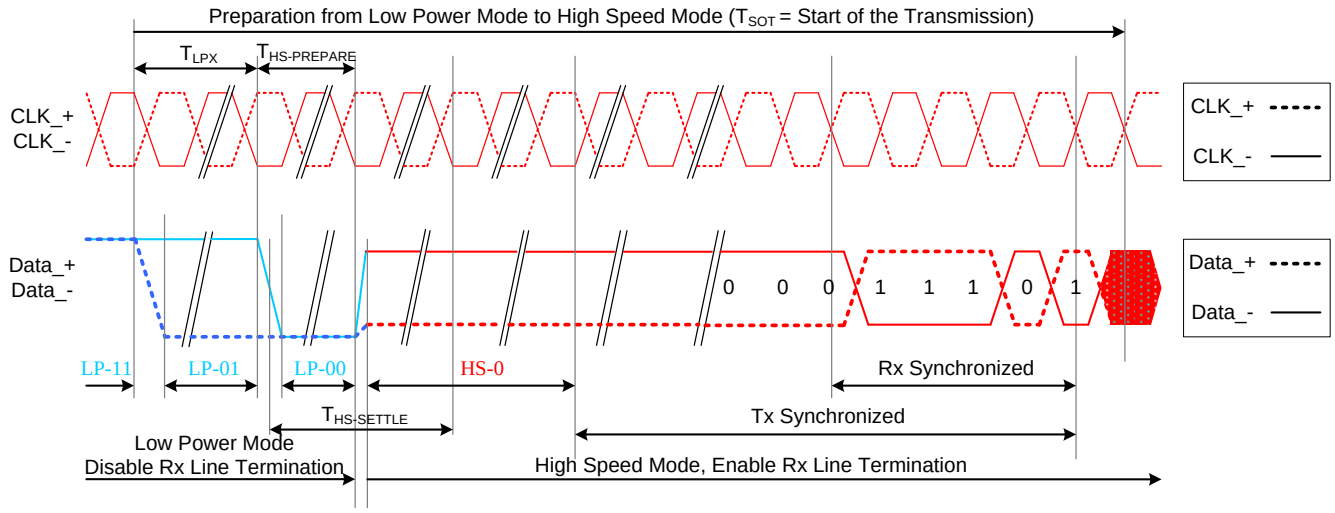
2. **High-Speed Data Transmission**

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes RX_CP/N have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



Entering High-Speed Data Transmission (T_{SOT} of HSDT)

Leaving High-Speed Data Transmission

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes RX_CP/N are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode.

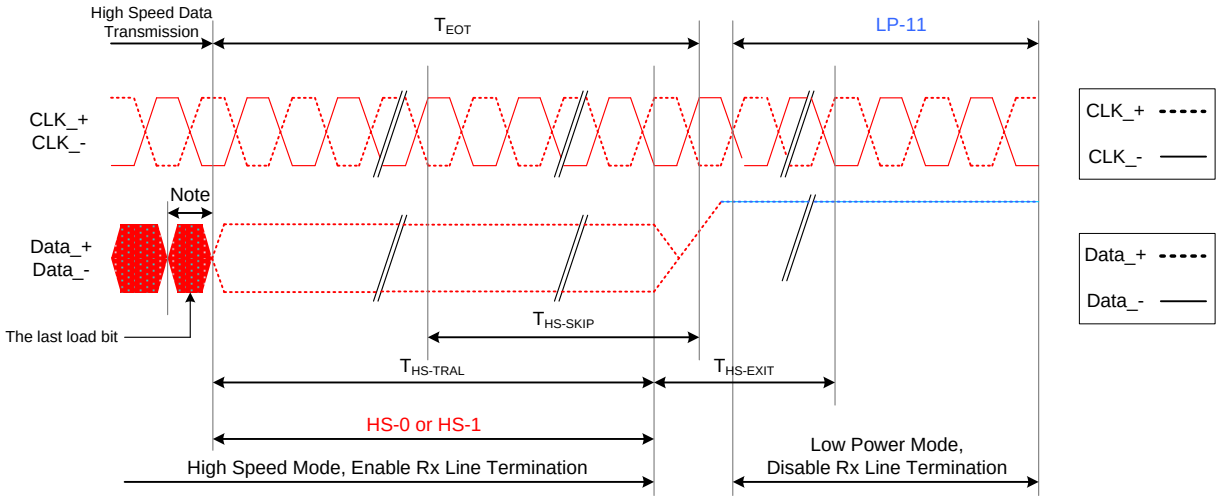
Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission

  MCU changes to HS-1, if the last load bit is HS-0

  MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

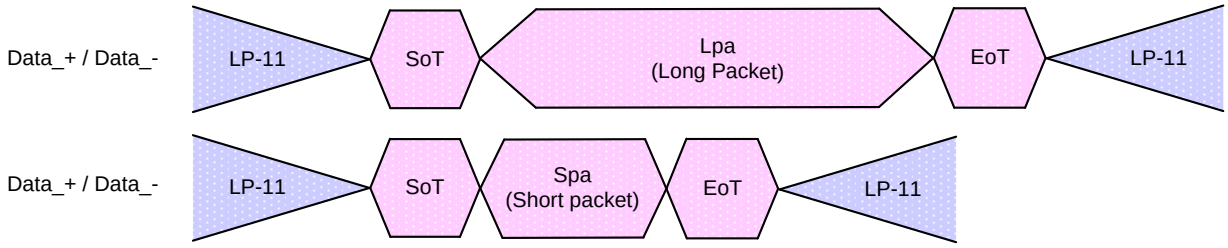


Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

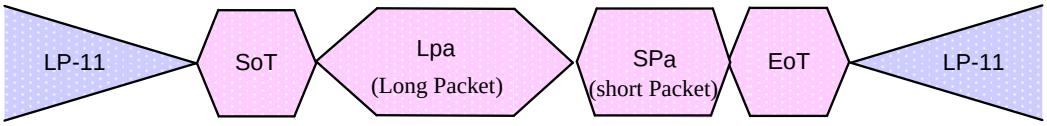
Burst of the High-Speed Data Transmission

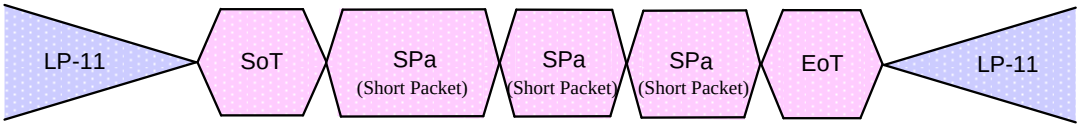
The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (Lpa) or Short (Spa) packets.

The single packet in High-Speed Data Transmission is illustrated for reference purposes below:



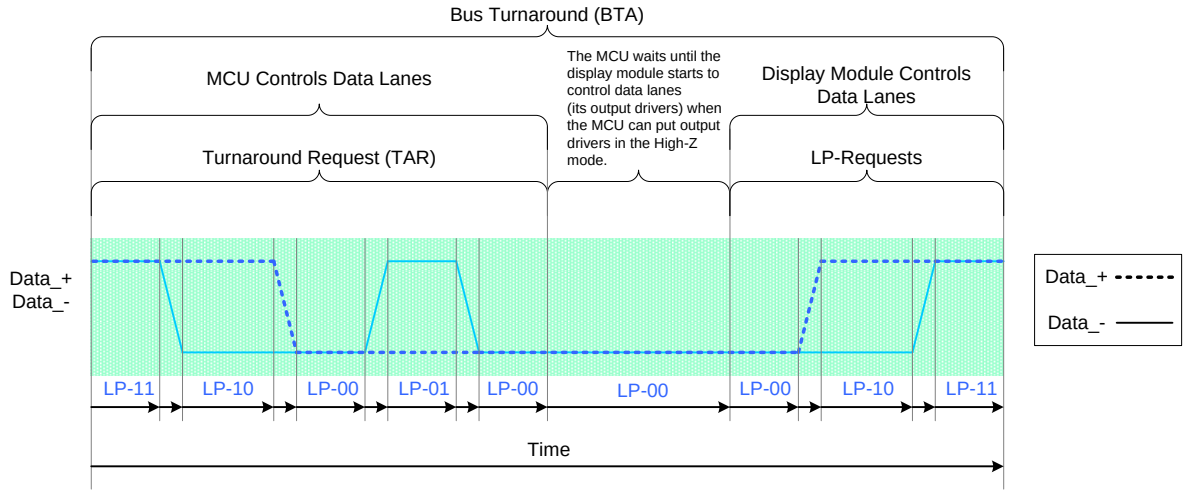
The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:





3. Bus Turnaround Request

The MCU which is controlling DSI-DATA_P/N Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or Display Module. The MCU and Display Module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to Display Module, as follows.

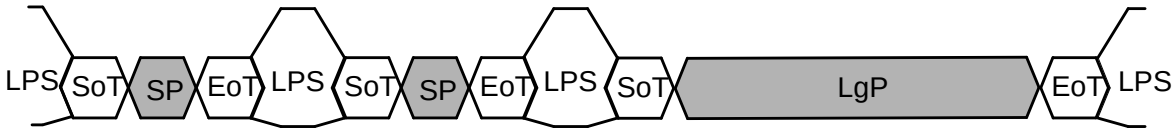


8.10.2 DSI protocol

The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The receiver side of a DSI Link performs the coverse of the transmitter side, decomposing the packet into parallel data, signal events and commands.

1.1.1.5 Multiple Packets per Transmission

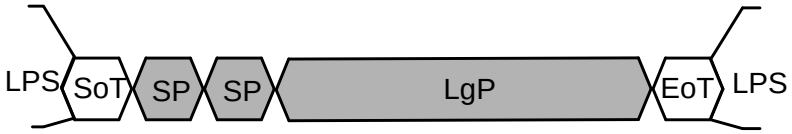
There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled.



Separate Transimssions

Key:

LPS -- Low power state
SoT -- Start of Transmission
EoT -- End of Transmission
SP -- Short Packet
LgP -- Long Packet



Single Transimssions

1.1.1.6 Packet Composition

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. For example, in Video Mode systems in a display application the logical unit for a packet may be one horizontal display line. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Packet sizes fall into two categories:

- **Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.
- **Long packets** specify the payload length using a two-byte Word Count field. Payloads may be

from 0 to 2^{16}-1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

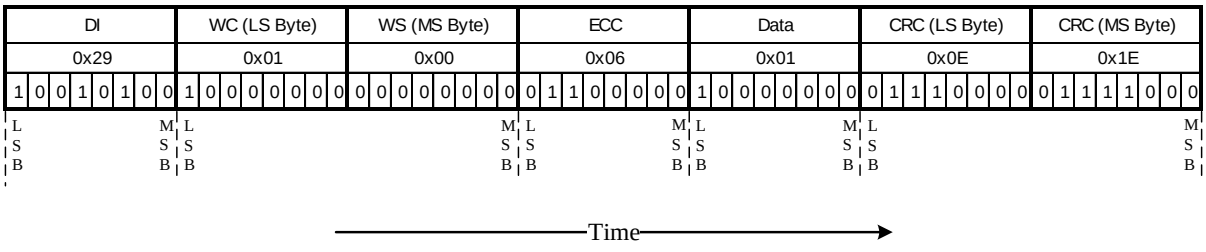
A special case of Command Mode operation is video-rate (update) streaming, which takes the form of an arbitrarily long stream of pixel or other data transmitted to the peripheral. As all DSI transactions use packets, the video stream shall be broken into separate packets. This “packetization” may be done by hardware or software. The peripheral may then reassemble the packets into a continuous video stream for display.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

1.1.1.7 Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

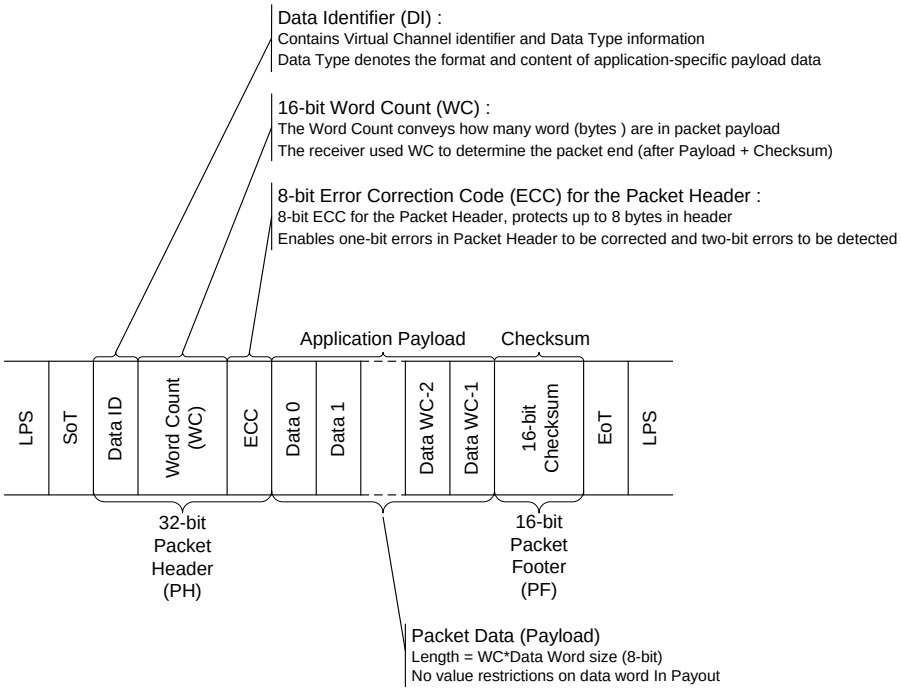
Figure 12 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.



Endian Example (Long Packet)

1.1.1.8 General Packet Structure(Long Packet Format)

A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.



Long Packet Structure

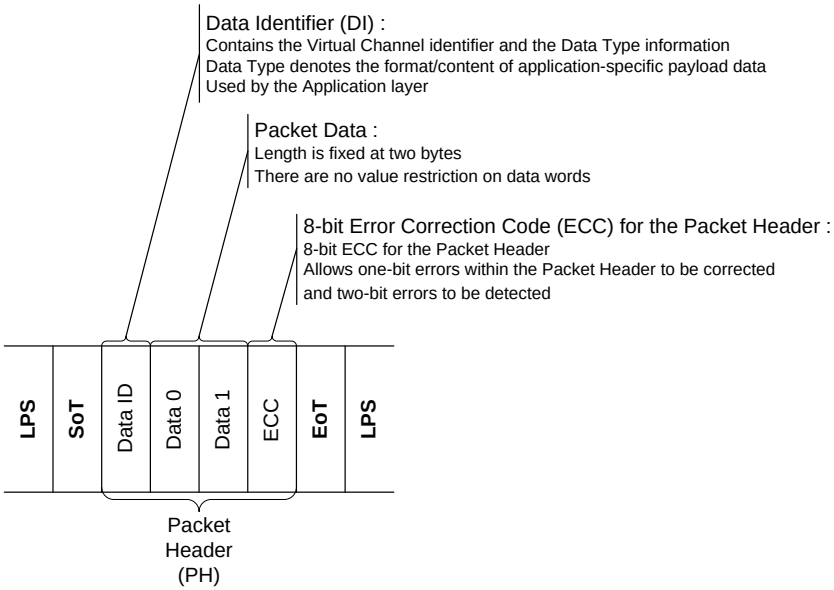
The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data. See sections 8.8 through 8.10 for descriptions of Data Types. The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields. After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used. Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (FFFFh). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0000h). See section 9 for more information on calculating the Checksum. In the generic case, the length of the Data Payload shall be a multiple of bytes. In addition, each data format may impose additional restrictions on the length of the payload data, e.g. multiple of four bytes. Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first

.

1.1.1.9 General Packet Structure(Short Packet Format)

A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code

(ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.



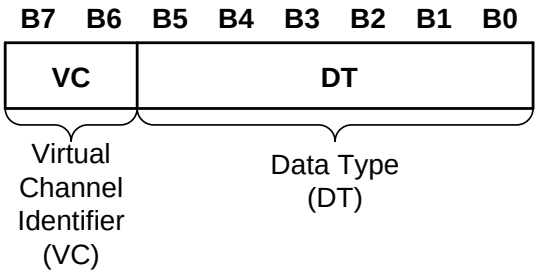
Short Packet Structure

1.1.1.10 Common Packet Elements

Long and Short packets have several common elements that are described in this section.

➢Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 15 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels.DI[5:0]: These six bits specify the Data Type.

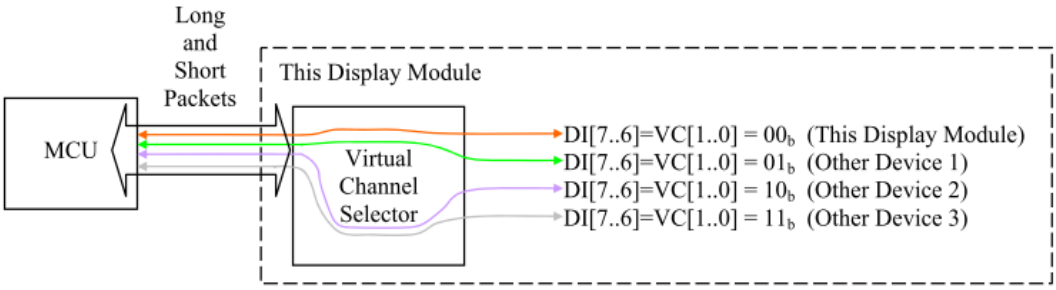


Data Identifier Byte

Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Note that packets sent in a single transmission each have their own Virtual Channel assignment and can be directed to different peripherals. Although the DSI protocol permits communication with multiple peripherals, this specification only addresses the connection of a host processor to a single peripheral. Implementation details for connection to more than one physical peripheral are beyond the scope

of this document.



Virtual Channel (VC) Configuration

Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

1.1.1.11 Error Correction Code

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

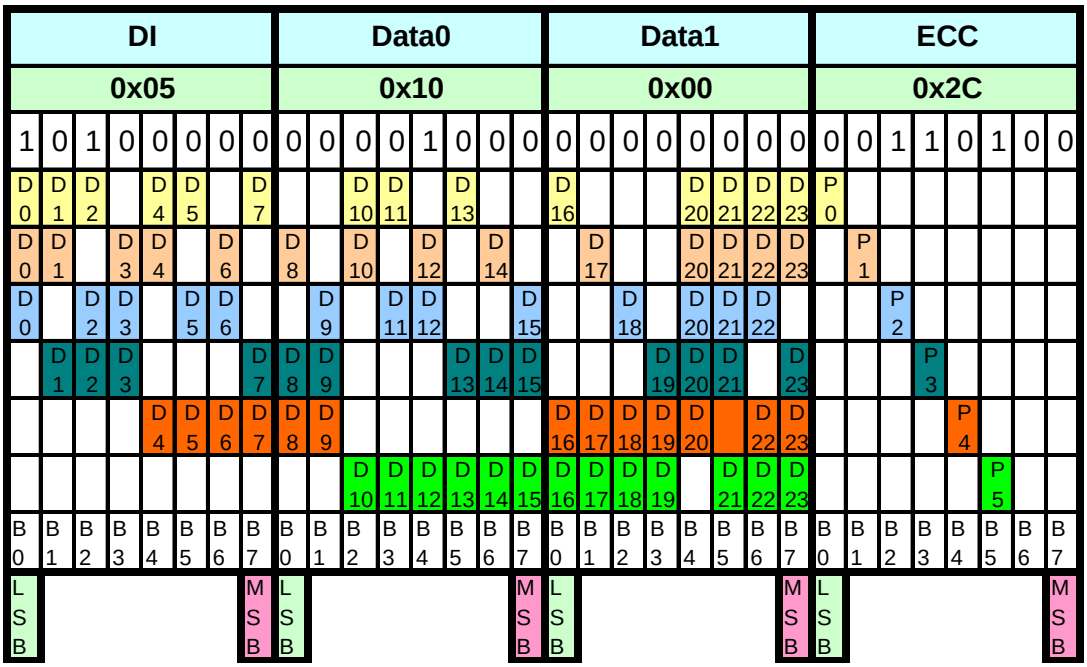
P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

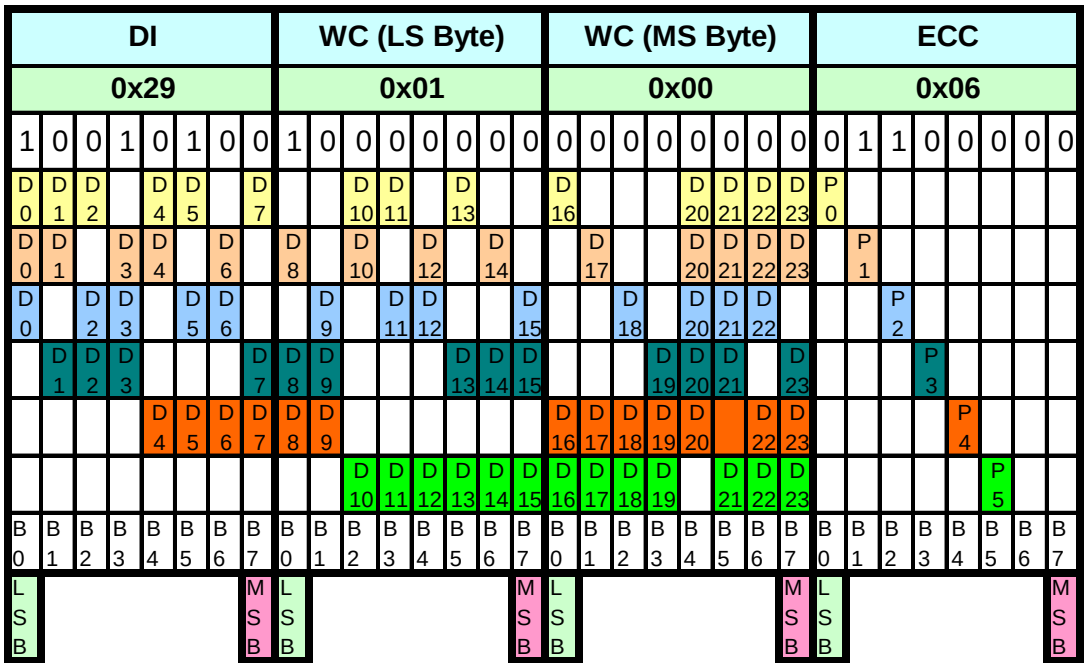
P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to ‘0’ because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, there is only needed 6 bits (P [5…0]) for Error Correction Code (ECC).



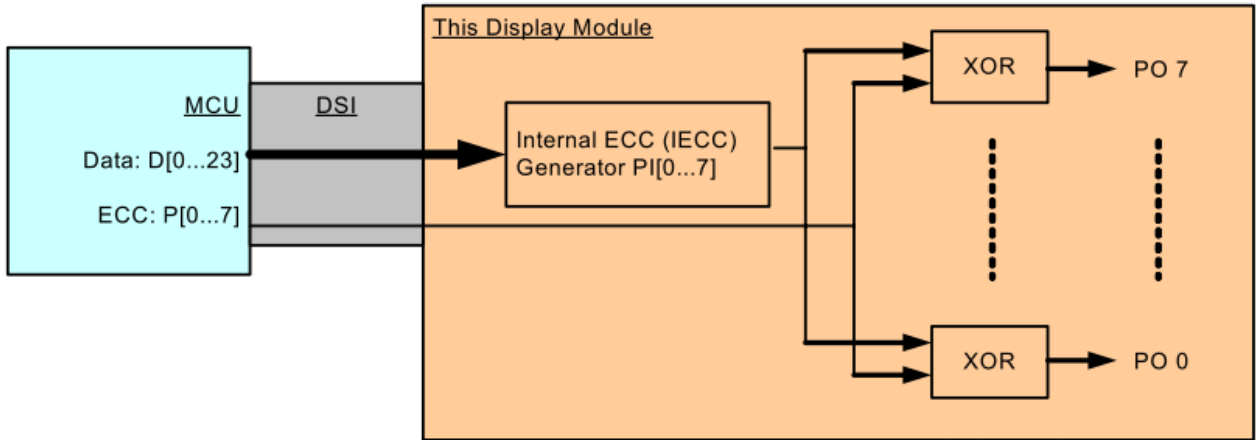
XOR Functionality on the Short Packet (Spa)



XOR Functionality on the Long Packet (Lpa)

The transmitter (The MCU or the Display Module) is sending data bits D[23:0] and Error Correction Code (ECC) P[7:0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction

Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7:0].



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23:0]) and ECC (P[7:0]) are received correctly, if a value of the PO[7:0]) is 00h. The sent data bits (D[23:0]) and ECC (P[7:0]) are not received correctly, if a value of the PO[7:0]) is not 00h.

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC	0	0	0	0	0	0	0	0	=00h => No Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC	0	0	1	1	0	0	0	0	=0Ch => Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values – Error

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

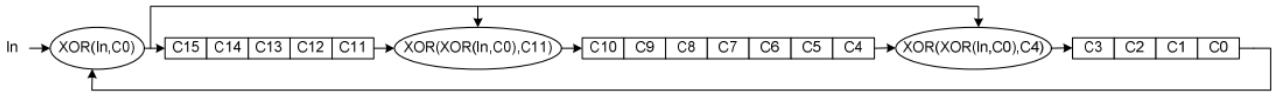
One error is detected if the value of the PO[7:0] is on the above table : One it Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23:0]), what is not correct, is D[3]

More than one error is detected if the value of the PO [7…0] is not on the above table: One Bit Error Value of the Error Correction Code (ECC) e.g. PO [7…0] = 0Ch.

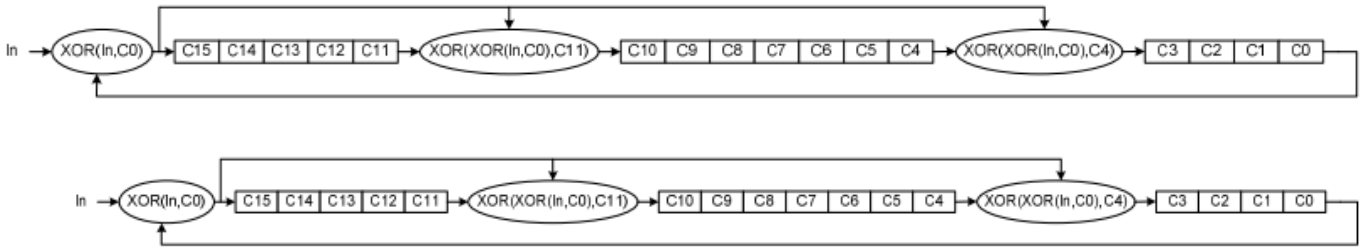
1.1.1.12 Packet Footer on the Long Packet

Packet Footer (PF) of the Long Packet (Lpa) is defined after the Packet Data (PD) of the Long Packet (Lpa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (Lpa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X_{16} + X_{12} + X_5 + X_0$ as it is illustrated below.



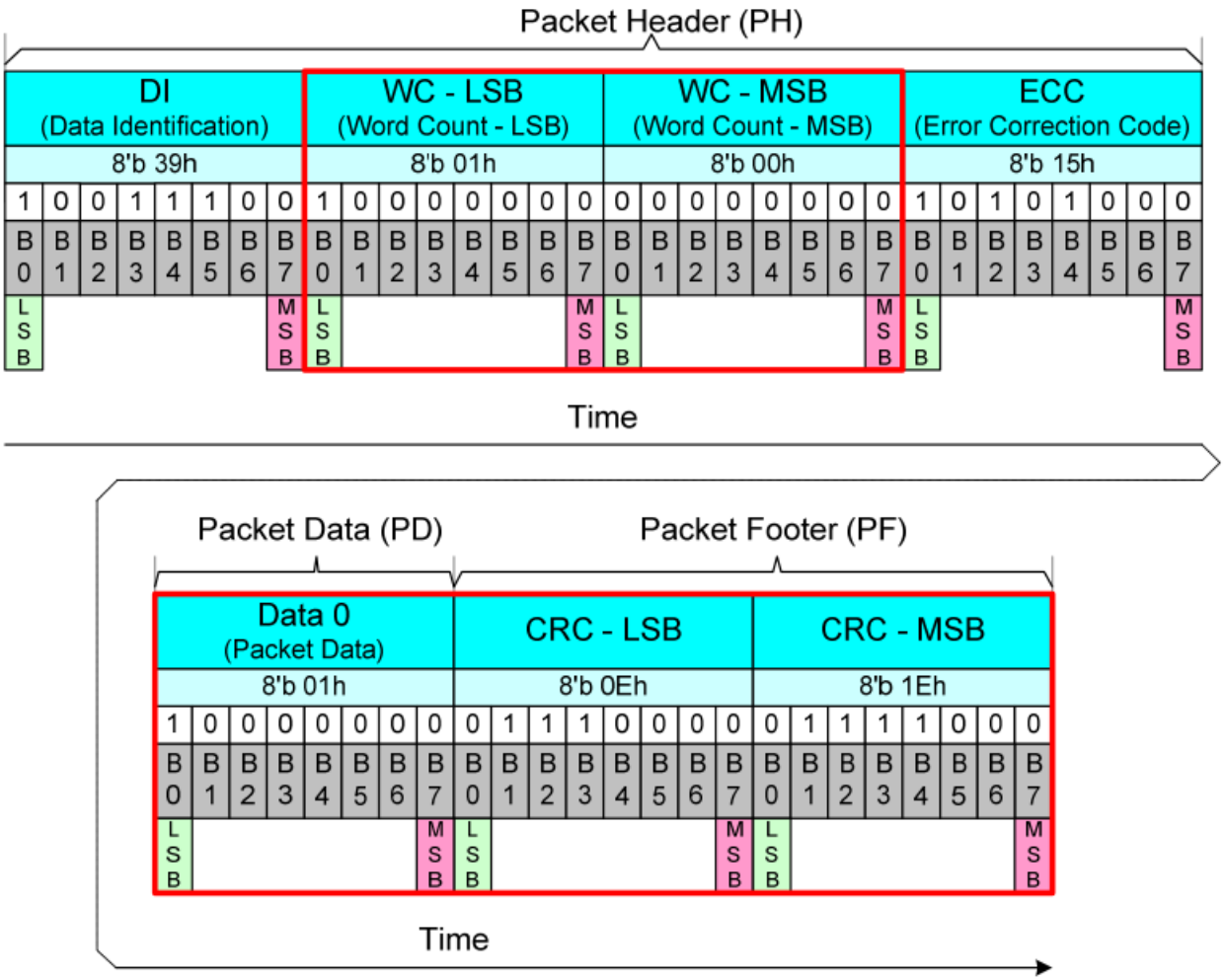
The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (Lpa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) is equal and vice versa the received Packet Data (PD) and Packet Footer(PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

1.1.1.13 Processor to Peripheral Direction Packet Data Types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are show as below table.

Data type	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h / XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Data Types for Processor-sourced Packets

All detail function of data types is as below：

Sync event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	**Function description**	**Number of bytes**
01h	Sync Event, V Sync Start	Short
11h	Sync Event, V Sync End	Short
21h	Sync Event, H Sync Start	Short
31h	Sync Event, H Sync End	Short
Note: In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.		

Color mode status (Color Mode On, Color Mode Off)		
Data type, hex	**Function description**	**Number of bytes**
02h	Color Mode On that switches a Video Mode display module to a low-color mode for power saving.	Short
12h	Color Mode Off that switches a Video Mode display module from low-color display to normal display.	Short

Display status (shutdown command, turn-on command)		
Data type, hex	**Function description**	**Number of bytes**
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	Short
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	Short
Note: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.		

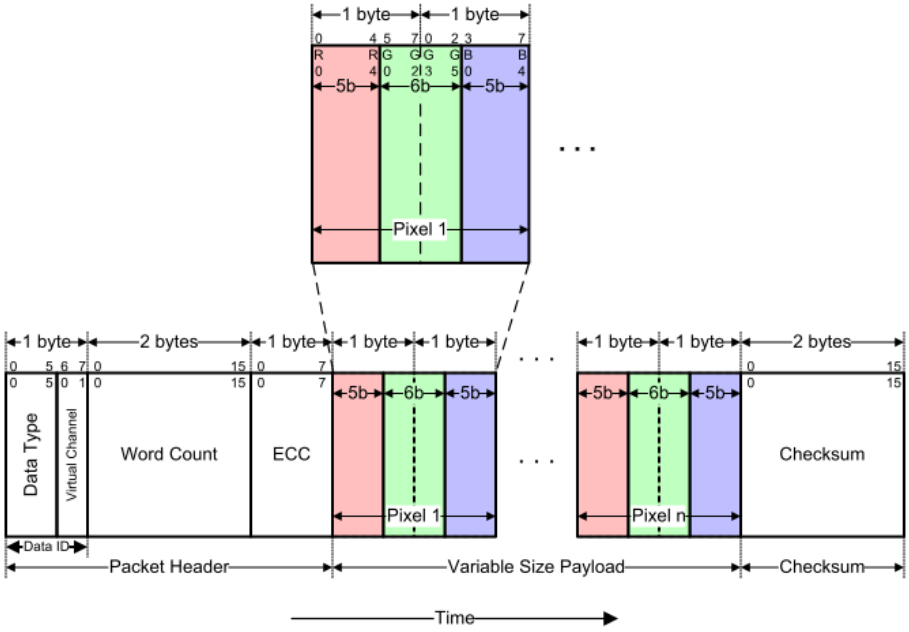
DCS command setting		
Data type, hex	**Function description**	**Number of bytes**
05/15h	DCS Short Write command is used to write a single data byte to a peripheral such as a display module. If a parameter is not required, the parameter byte shall be 00h.	Short
06h	DCS Read command, the returned data may be of Short or Long packet format.	Short

39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Long

Return packet size setting		
Data type, hex	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	Short
Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.		

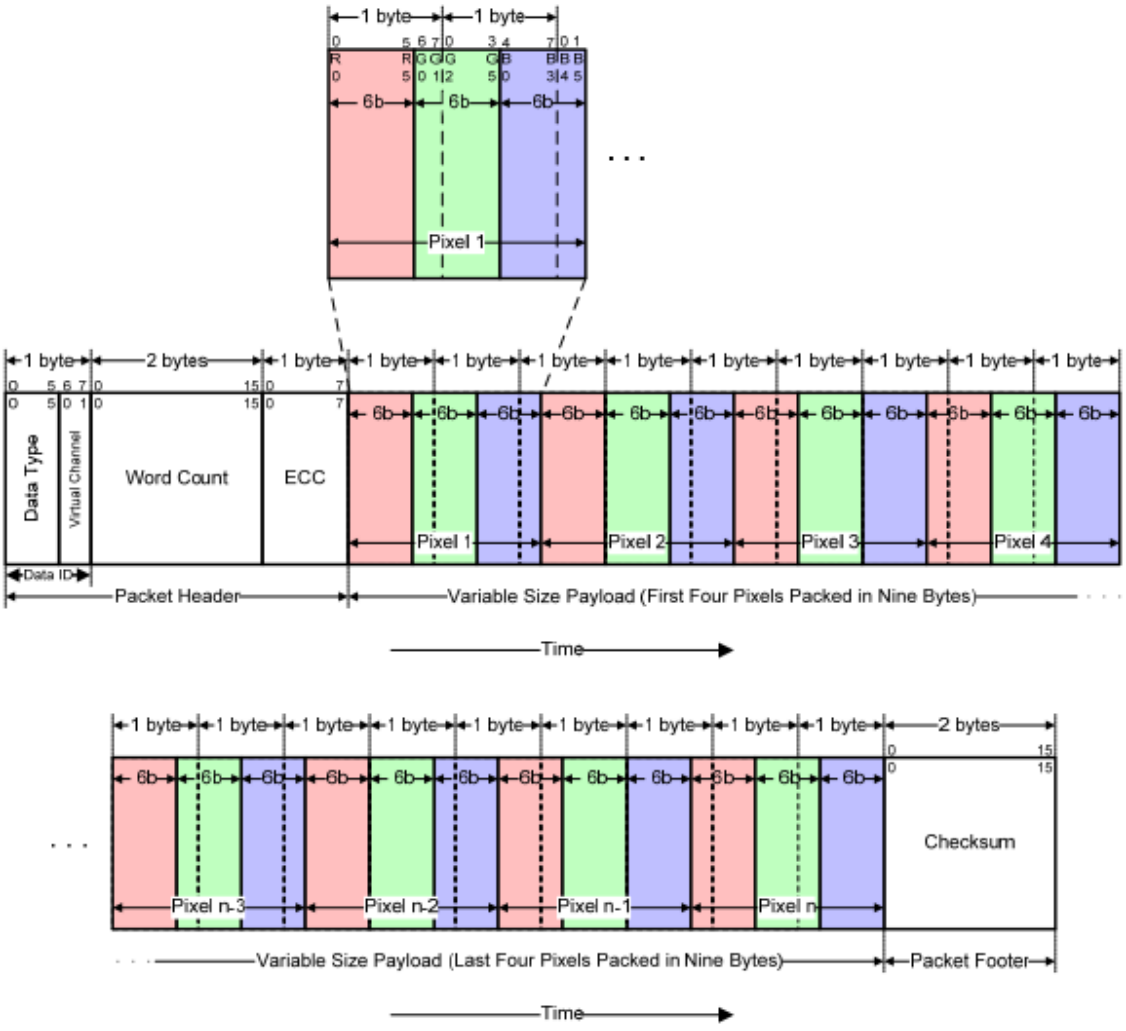
Variable data packet		
Data type, hex	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Short
19h	Blanking packet is used to convey blanking timing information in a Long packet.	Short
Note: (1) When Null Packet, the Payload Data belong “null” Data, actual data values sent are irrelevant because the peripheral does not capture or store the data. (2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display,		

Data stream format – 16bit Format

Data stream format – 16bit Format		
Data type, hex	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is five bits red, six bits green, five bits blue, in that order.	Long
		
Note: That the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.		

Data stream format – 18bit Format (mode1)

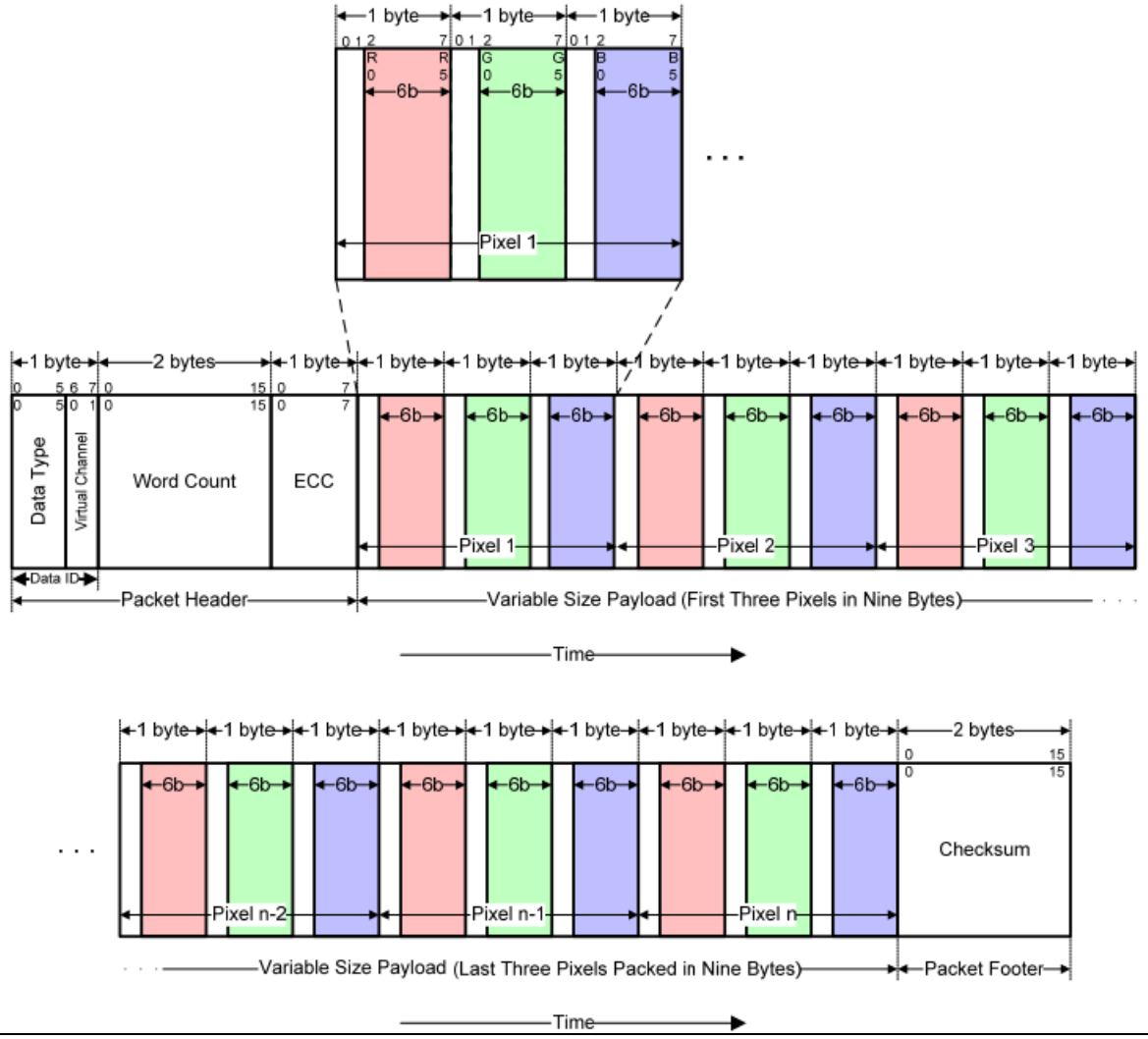
Data stream format – 18bit Format(Mode1)		
Data type, hex	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is six bits red, six bits green, six bits blue, in that order.	Long



Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a “clean start” for the next line.

Data stream format – 18bit Format(mode2)

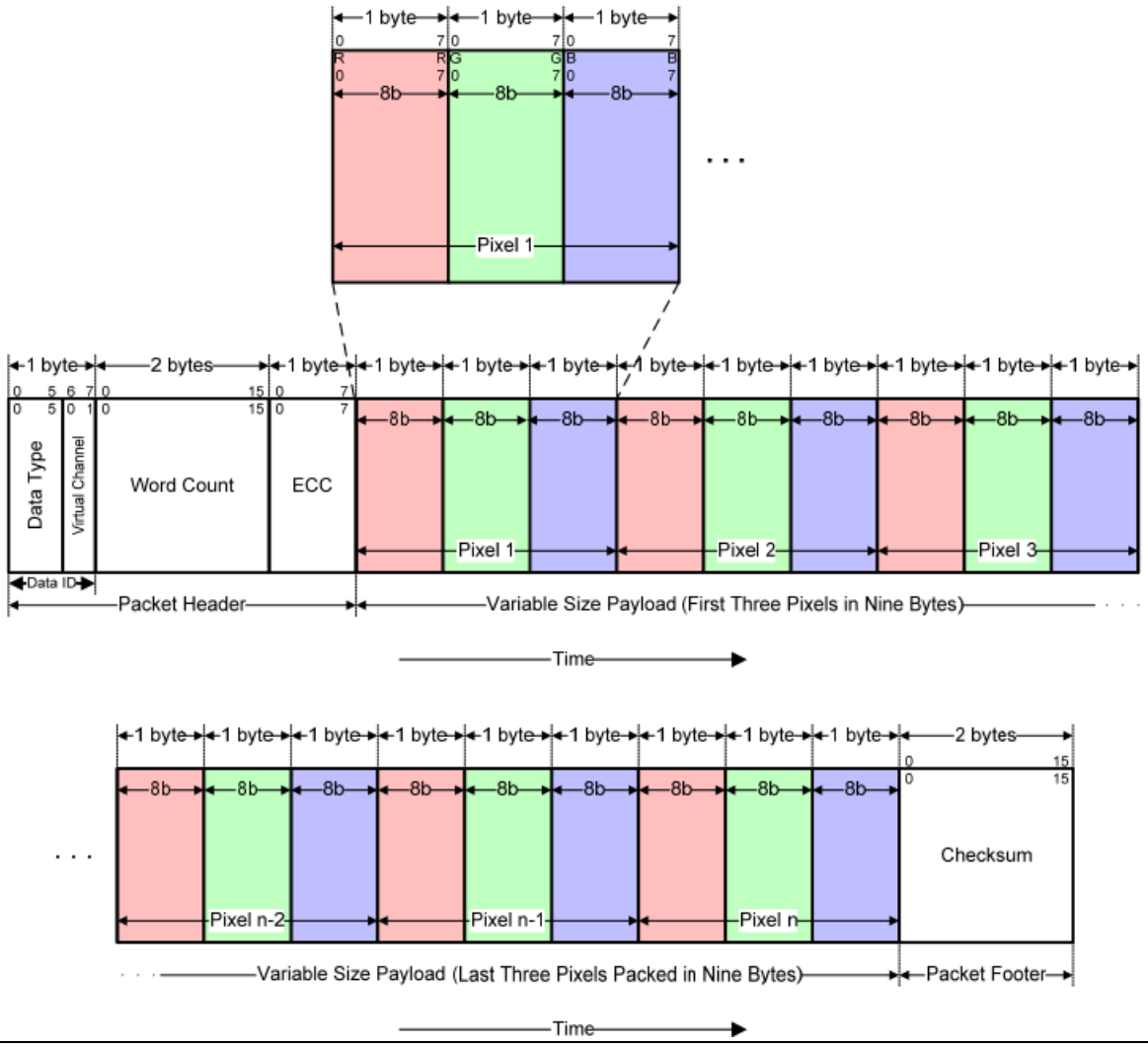
Data stream format – 18bit Format(Mode2)		
Data type, hex	**Function description**	**Number of bytes**
2Eh	In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits[1:0] of each payload byte representing active pixels are ignored.	Long



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Data stream format – 24bit Format

Data stream format –24bit Format		
Data type, hex	**Function description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Long



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

1.1.1.14 Peripheral-to-Processor (Reverse Direction) LP Transmissions

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions; other Lanes shall be unidirectional. Reverse-direction signaling shall only use LP (Low Power) mode of transmission.

Peripheral-to-processor transactions are of four basic types:

- Tearing Effect is a Trigger message sent to convey display timing information to the host processor. Trigger messages ate signal byte packets sent by a peripheral's PHY layer in response to a signal form the DSI protocol layer.
- Acknowledge is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
- Acknowledge and Error Report is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
- Response to Read Request may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command in which no error was detected, the peripheral shall respond with Acknowledge.
- Following a Read request in which no error was detected, the peripheral shall send the requested READ data.
- Following a Read request in which the ECC error was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
- Following a non-Read command in which the ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
- Following any command in which SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid was detected, or the DSI command was not

recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. Table 18 shows the bit assignment for all error reporting.

Bit	Error Report Bit Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

The table as below presents the complete set of peripheral-to-processor Data Types

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge and Error Report	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
1Ah	01 1010	Generic Long READ Response	Short
1Ch	01 1100	DCS Long READ Response	Short
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short

Data Types for Peripheral-sourced Packets

Acknowledge types		
Data type, hex	**Function description**	**Number of bytes**
02h	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error Acknowledge with error report, Without error Acknowledge.		

Generic Read types		
Data type, hex	**Function description**	**Number of bytes**
11h, 12h	This is the Generic Short Read Response, 1 or 2bytes, respectively.	4 bytes
1Ah	This is the long-packet response to Generic Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		

DCS Read types		
Data type, hex	**Function description**	**Number of bytes**
21h, 22h	This is the DCS Short Read Response, 1 or 2bytes, respectively..	4 bytes
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		