5 BLOCK DIAGRAM

S1 ~ S540

VAP   VAN

GIP

540 Source Buffer

Voltage Referene

GIP Buffer

DAC

Level Shifter

Gamma Circuit

GIP Decoder

Level Shifter

Data Latch

Gamma Table

VCOM

Display Ram
360 x 390 x 18 bits

Display Control

OSC1   OSC2

Instruction Register

NVM

Booster

Interface

TE RDY AUTO_DL_EN PSWAP MIPI_CLKP/N MIPI_D0P/N HSYNC VSYNC ENABLE DOTCLK RD WR CS DC SDA2 SDA1 SCK DB[7:0] IM[3:0] RESET VDDI VPP

VGL VGH AVCL AVDD VDD

6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDD	I	- Power Supply for Analog, Digital System and Booster Circuit.	VDD
VDDI	I	- Power Supply for I/O System. - VDDI must be lower than or equal to VDD.	VDDI
GND	I	- System Ground for Analog System, Digital System, I/O System and Booster Circuit.	GND
RGND	I	- System Ground for Reference Circuit.	GND
VPP	I	- Power Supply for Internal NVM. - When programming NVM, It needs external power supply voltage (7.5V). - The current of Ivpp must be more than 10mA. - If not used, Leaves these pins open.	External Power

6.2 Interface Logic Pins

Name	I/O	Description	Connect Pin
IM2P IM1P IM0P	I	-The System interface mode select. | IM2	IM1	IM0	MPU Interface Mode	Data pin
-----	-----	-----	---------------------	----------
0	0	0	3-line 9bit serial I/F	SDA: in/out
0	0	1	MIPI I/F	DP/DN
0	1	0	2 data lane serial I/F	SDA1: in/out、SDA2: in
0	1	1	QSPI I/F	SDA1: in/out、SDA[3:0]: in
1	0	0	RGB_3-line 9bit serial I/F	SDA: in/out、DB[5:0]: in
1	0	1	RGB_4-line 8bit serial I/F	SDA: in/out、DB[5:0]: in
1	1	0	4-line 8bit serial I/F	SDA: in/out
1	1	1	80-8bit parallel I/F	DB[7:0]: in/out		GND/VDDI
GRBP	I	-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.	MCU
D[7:0]P	I/O	-D[7:0]P are used as MCU parallel interface data bus. 8-bit parallel I/F: D[7:0]P are used. -D[7:0]P are used as SPI interface data bus. 8-bit serial I/F: D0P is used. (SDA) 9-bit serial I/F: D0P is used. (SDA)	MCU

Name	I/O	Description	Connect Pin
		2 data lane serial I/F: D[1:0]P are used. (SDA1、SDA2) -D[7:0]P are used as QSPI interface data bus. Single: D0P is used. (SDA0) Dual: D[1:0]P are used. (SDA0、SDA1) Quad: D[3:0]P are used. (SDA0、SDA1、SDA2、SDA3) - D[7:0]P are used as RGB interface data bus. 6-bit RGB I/F: D[7:2]P are used.；D1P is used. (DE) -If not used, please fix this pin at VDDI or GND.	
TEP	O	-Tearing effect signal is used to synchronize MCU to frame memory writing. -If not used, please let this pin open.	MCU
CSXP	I	-Chip select pin. Low enable. High disable	MCU
DCXP	I	-Display data/command selection pin in parallel interface. DCX='1': display data or parameter. DCX='0': command data. -Display data/command selection pin in 4-line serial interface. (A0) DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at VDDI or GND.	MCU
WRXP	I	-Write enable in MCU parallel interface. - Dot clock signal in RGB interface. (DOTCLK) -If not used, please fix this pin at VDDI or GND.	MCU
RDXP	I	-Read enable in MCU parallel interface. - Clock in SPI interface. (SCL) -If not used, please fix this pin at VDDI or GND.	MCU
HSYNCP	I	-Horizontal (Line) synchronizing input signal in RGB interface. -If not used, please fix to the VDDI or GND.	MCU
VSYNCP	I	-Vertical (Frame) synchronizing input signal in RGB interface. -If not used, please fix to the VDDI or GND.	MCU
PSWAP	I	-Differential clock polarity swap in MIPI-DSI interface. 	PSWAP	IM2	IM1	IM0	MIPI I/F (HSCP/HSCN/HSDP/HSDN)
---	---	---	---	---
0	0	0	1	HSCP HSCN HSDP HSDN
1				HSCN HSCP HSDN HSDP		GND/VDDI
CP	I	-MIPI-DSI clock lane positive-end input pin.	MCU

Name	I/O	Description	Connect Pin
		-If not used, please fix this pin at GND.	
CN	I	-MIPI-DSI clock lane negative-end input pin. -If not used, please fix this pin at GND.	MCU
DP	I/O	-MIPI-DSI data lane positive-end input pin. -If not used, please fix this pin at GND.	MCU
DN	I/O	-MIPI-DSI data lane negative-end input pin. -If not used, please fix this pin at GND.	MCU
AUTO_DL_ENP	I	-OTP trim function control pin. -When normal display, this pin should be set to "H" and the value in the OTP will be downloaded automatically.<table><tr><td>AUTO_DL_ENP</td><td>Function Description</td></tr><tr><td>L</td><td>Disable auto-refresh function</td></tr><tr><td>H</td><td>Enable auto-refresh function(Default)</td></tr></table>	GND/VDDI
RDYP	O	-Compressed processing busy flag is used to notice Host that compressed processing has completed. -If not used, please let this pin open.	MCU

6.3 Driver Output Pins

Name	I/O	Description	Connect pin
S[540:1]	O	-Source output voltage signals applied to liquid crystal.	LCD
GOR[10:1] GOL[10:1]	O	-Gate control signals and the swing voltage level is VGH to VGL.	LCD
VGHOR	O	-Power output (Positive) pin for gate driver.	LCD
VGHOL	O	-Power output (Positive) pin for gate driver.	LCD
VCOM	O	-A power supply for the TFT-LCD common electrode.	GND
VCOML	O	-A power supply for the TFT-LCD common electrode.	GND
VGH	O	-Power output pin for gate driver. -If not used, please let this pin open.	LCD
VGL	O	-Power output (Negative) pin for gate driver. -If not used, please let this pin open.	LCD
VGHS	O	-Power output pin for gate driver. -If not used, please let this pin open.	LCD
CABCPWM	O	-PWM output signal to driving LED. -If not used, please let this pin open.	-

Note: Use Power Pad(VGL、VGHOR、VGHOL) instead of assigning GIP, if VGL and VGH are needed in Panel.

6.4 Test and Other Pins

Name	I/O	Description	Connect pin
Dummy	-	-These pins are dummy. -Leave the pin open.	OPEN
SVEE	O	-Used for monitoring. -Leave the pin open.	OPEN
SVDD	O	-Used for monitoring. -Leave the pin open.	OPEN
VCC	O	-Used for monitoring. -Leave the pin open.	OPEN
AVDD	O	-Power Pad for analog Circuit. -Leave the pin open.	OPEN
AVEE	O	-Power Pad for analog Circuit. -Leave the pin open.	OPEN
VAPP	O	-A power output of grayscale voltage. -Leave the pin open.	OPEN
VANP	O	-A power output (negative) of gray scale voltage. -Leave the pin open.	OPEN
VAG	O	-This pin is for testing. -Leave the pin open.	OPEN
V20P	O	-Used for monitoring. -Leave the pin open.	OPEN
TESTOUTP[7:0]	O	-This pin is for testing -Leave the pin open.	OPEN
TEST_INP[3:0]	I	-This pin is for testing -Leave the pin open.	OPEN

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

| Item	Symbol	Range	Unit
Supply Voltage (Analog)	VDD	- 0.3 ~ +4.6	V
Supply Voltage (I/O)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VCC	-0.3 ~ +2	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	0.5 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	0.5 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC Characteristics

7.2.1 DC characteristics for MIPI DSI

● MIPI Signaling Voltage Levels
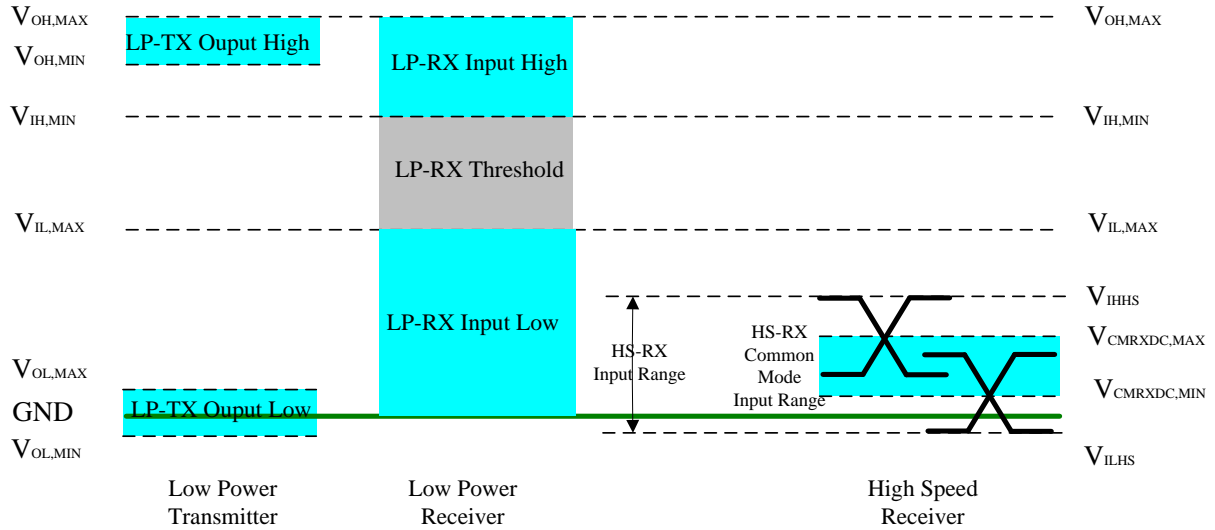
● MIPI DC characteristics

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

7.2.2 DC characteristics for Panel Driving

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.65	2.8	3.3	V	-
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	-
Gate Driver High Voltage	VGH	-	11.0	-	15.5	V	-
Gate Driver Low Voltage	VGL	-	-11.7	-	-8.4	V	-
Gate Driver Supply Voltage	-	| VGH-VGL |	-	-	27.2	V	-
Input / Output							
Logic-High Input Voltage	VIH	-	0.7VDDI	-	VDDI	V	Note 1
Logic-Low Input Voltage	VIL	-	GND	-	0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	GND	-	0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI	-	-	1	uA	Note 1
Logic-Low Input Current	IIL	VIN = GND	-1	-	-	uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1	-	+0.1	uA	Note 1
VCOM Voltage							
VCOM Voltage	VCOM	-	-	GND	-	V	-
Source Driver							
Gamma Reference Voltage(Positive)	VAP	-	3.65	-	6.2	V	-
Gamma Reference Voltage(Negative)	VAN	-	-4.2	-	-1.875	-	-
Source Output Settling Time	Tr	Below with 99% precision	-	-	20	us	Note 2
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note 3

Basic DC Characteristics

Notes:

1. TA= -30 to 85℃.

2. The max. value is between measured point of source output and gamma setting value.

3. The Max. Value is between measured point of source output and gamma setting value.

7.3 Power Consumption

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal Mode	Note	0.001	8	0.005	10
Sleep-in Mode	Note	0.001	0.030	0.005	0.150
Deep Standby Mode	Note	0.001	0.001	0.005	0.005

Notes:

1. Color Picture.

2. The Current Consumption is DC characteristics of ST77916.

3. Condition: VDDI=1.8V, VDD=2.8V.

7.4 AC Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 8-bit Bus

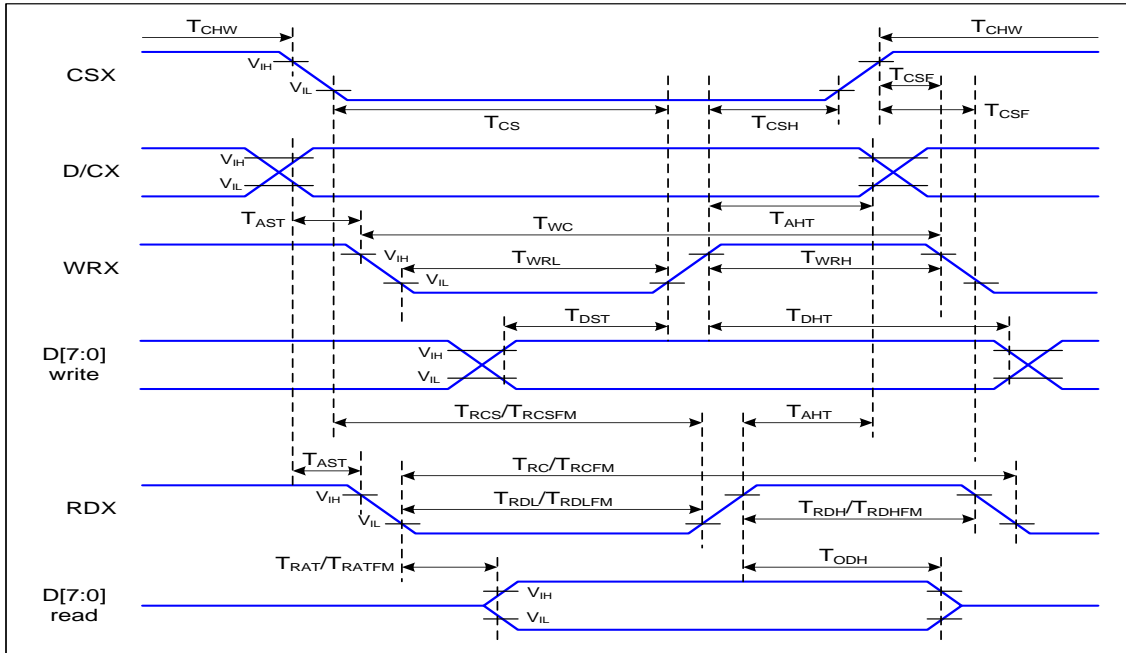**Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)**

VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter		Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time		0		ns	-
	T_{AHT}	Address hold time (Write/Read)		10		ns	
CSX	T_{CHW}	Chip select "H" pulse width		0		ns	-
	T_{CS}	Chip select setup time (Write)		15		ns	
	T_{RCS}	Chip select setup time (Read ID)		45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)		355		ns	
	T_{CSF}	Chip select wait time (Write/Read)		10		ns	
	T_{CSH}	Chip select hold time		10		ns	
WRX	T_{WC}	Write cycle		30		ns	
	T_{WRH}	Control pulse "H" duration		14		ns	
	T_{WRL}	Control pulse "L" duration		14		ns	
RDX (ID)	T_{RC}	Read cycle (ID)		160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)		90		ns	
	T_{RDL}	Control pulse "L" duration (ID)		45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)		450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)		90		ns	

	T_RDLFM	Control pulse "L" duration (FM)		355		ns	
D[7:0]	T_DST	Data setup time		10		ns	For CL=30pF
	T_DHT	Data hold time		10		ns	
	T_RAT	Read access time (ID)			40	ns	
	T_RATFM	Read access time (FM)			340	ns	
	T_ODH	Output disable time		20	80	ns	

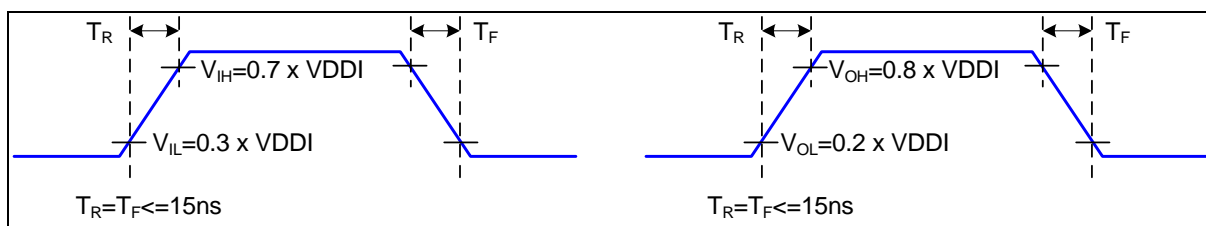**Table 1 8080 Parallel Interface Characteristics**

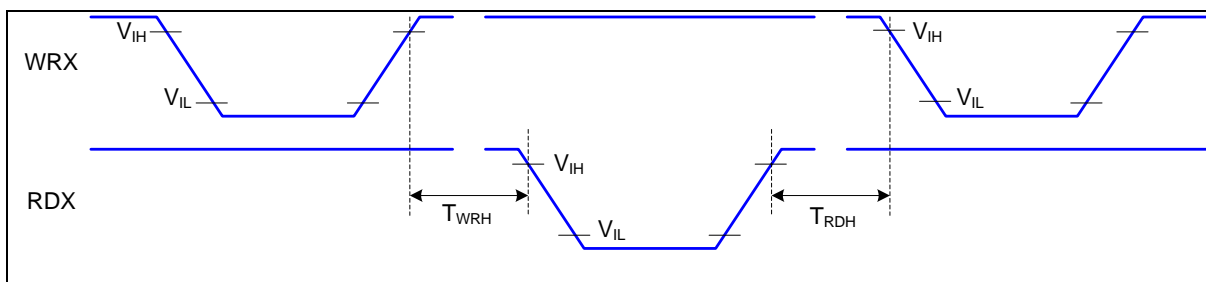**Figure 2 Rising and Falling Timing for I/O Signal**

Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

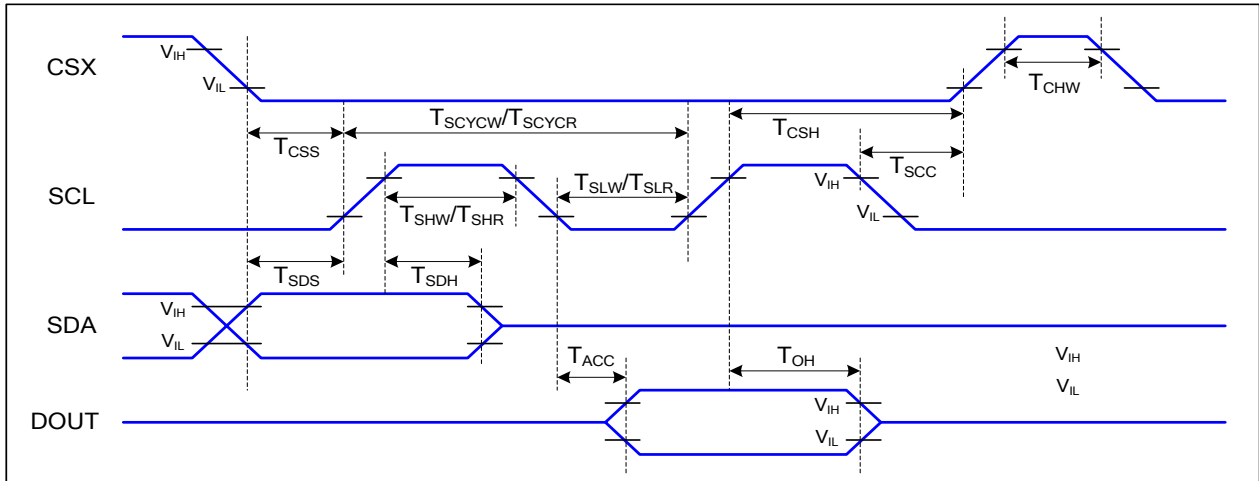### 7.4.2 Serial Interface Characteristics (3-line serial):

Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 2 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

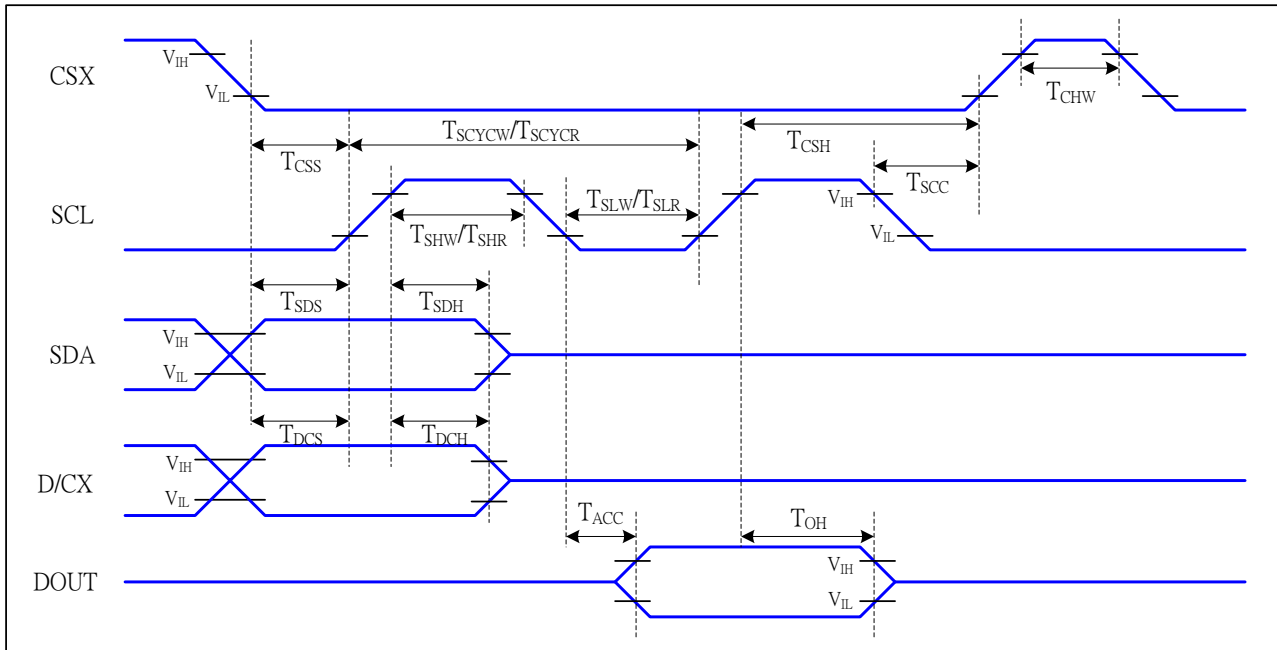### 7.4.3 Serial Interface Characteristics (4-line serial):

**Figure 5 4-line serial Interface Timing Characteristics**

VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	7		ns	
	T_{DCH}	D/CX hold time	7		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 3 4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.4 RGB Interface Characteristics:
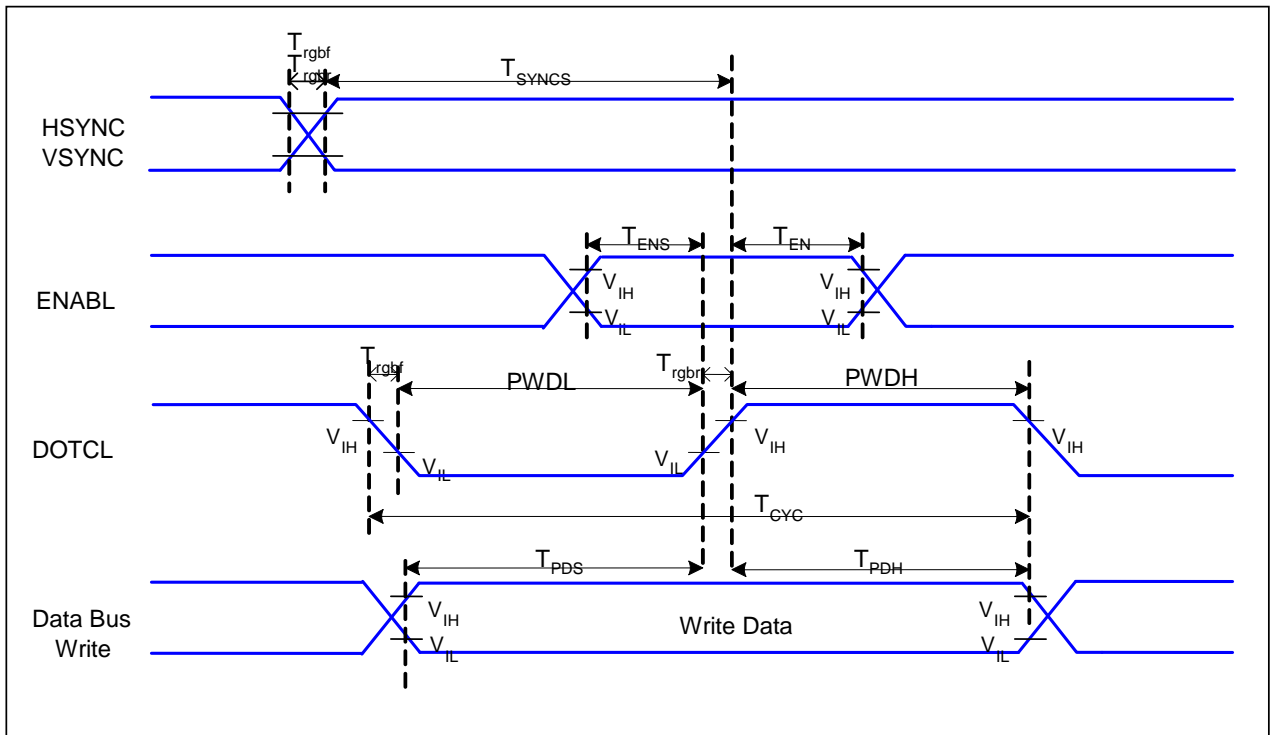
VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	35	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

Table 4 6 Bits RGB Interface Timing Characteristics
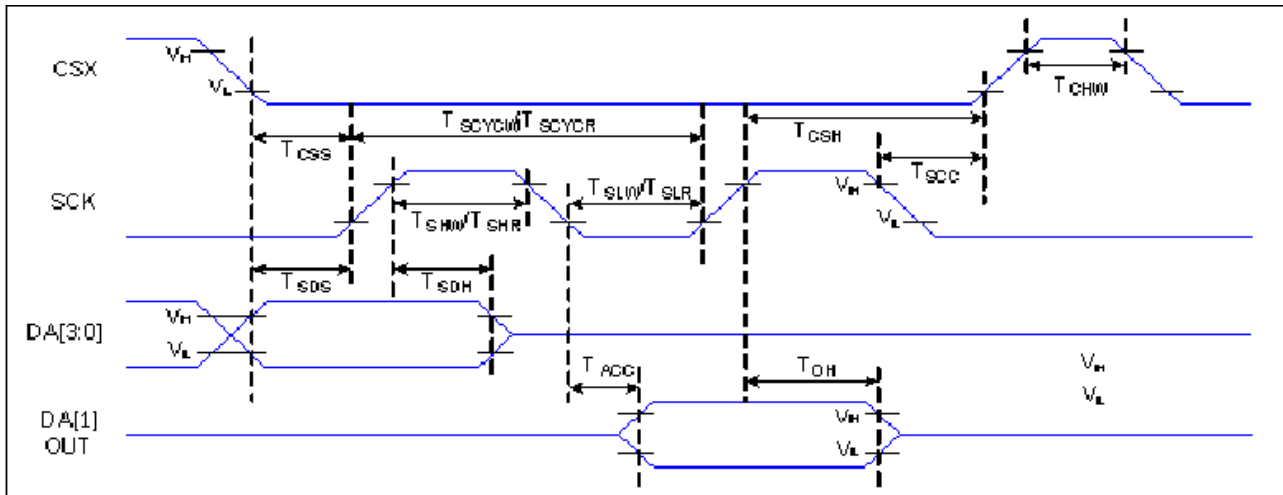
7.4.5 QSPI Interface Characteristics:

Figure 7 QSPI Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.65 to 3.3V, GND=RGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
			200		ns	*Note1*
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 QSPI Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.
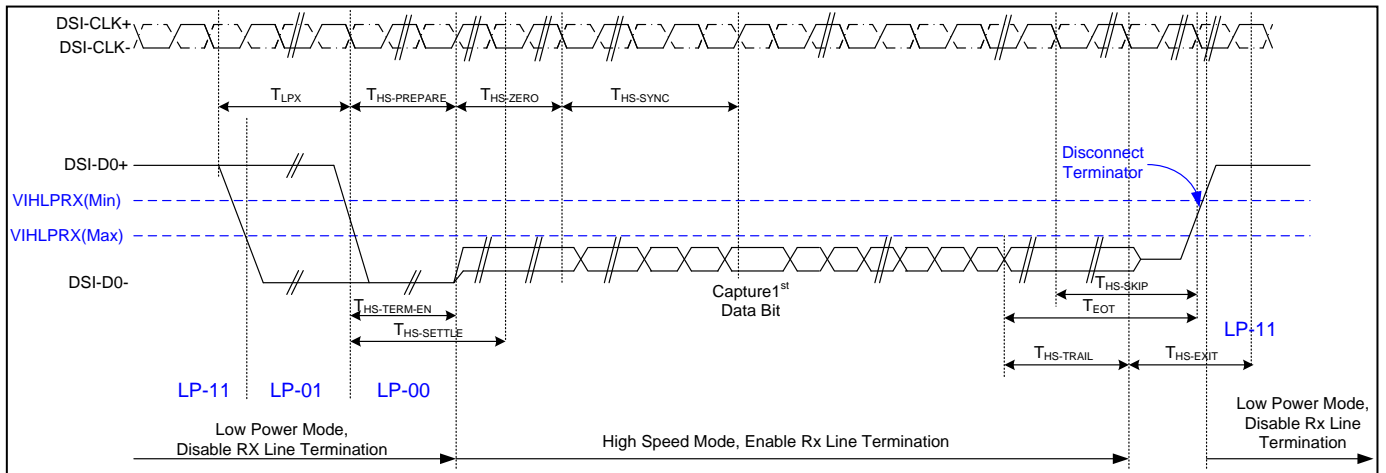

7.4.6 MIPI Interface Characteristics

High Speed Mode – Clock Channel Timing
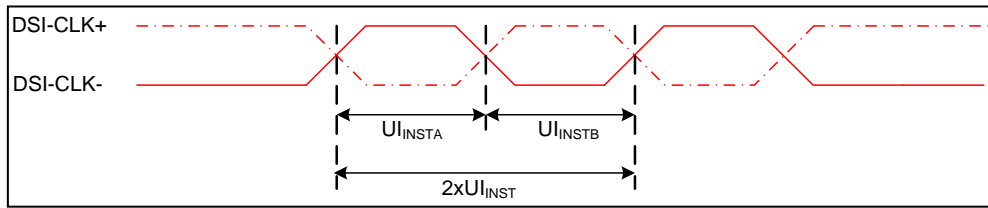
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI instantaneous	8	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	4	12.5	ns	

High-Speed Data Transmission

Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

## Switching the Clock Lane between Clock Transmission and Low-Power Mode
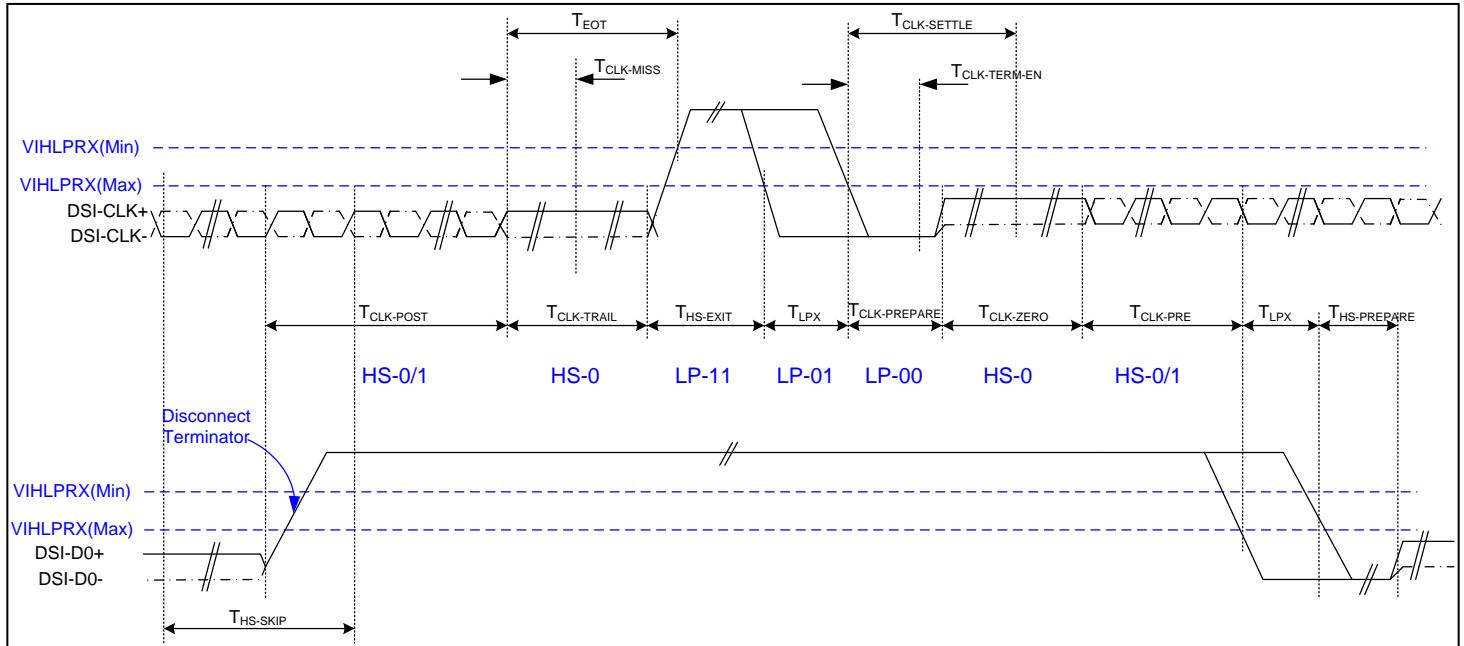
Parameter	Symbol	MIN	TYP	MAX	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	T CLK-POST	60+52UI			ns
Detection time that the clock has stopped toggling	T CLK-MISS			60	ns
Time to drive LP-00 to prepare for HS clock transmission	T CLK-PREPARE	38		95	ns
Minimum lead HS-0 drive period before starting Clock	T CLK-PREPARE +T CLK-ZERO	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	T HS-TERM-EN			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	T CLK-PRE	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	T CLK-TRAIL	60			ns

Bus Turnaround Procedure
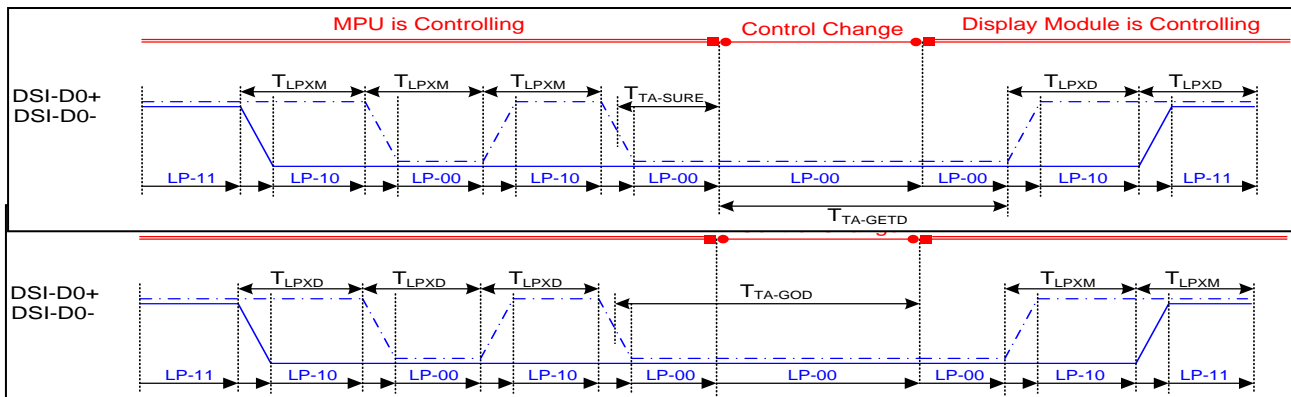
Parameter	Symbol	MIN	TYP	MAX	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	50	52.5	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		2 T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}		5 T_{LPX}		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		4 T_{LPX}		ns

7.4.7 Reset Timing
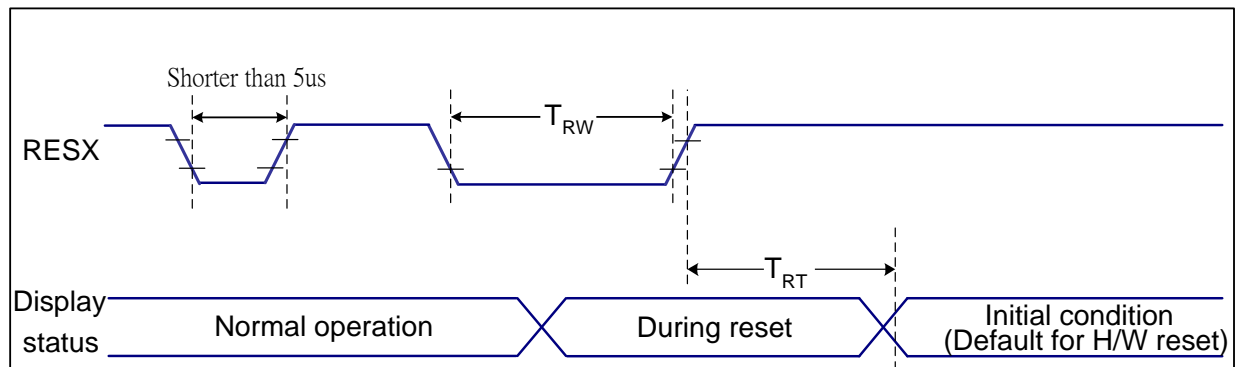
VDDI=1.8V,VDD=2.8V, GND=RGND=0V, Ta=25℃

| Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to

registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:
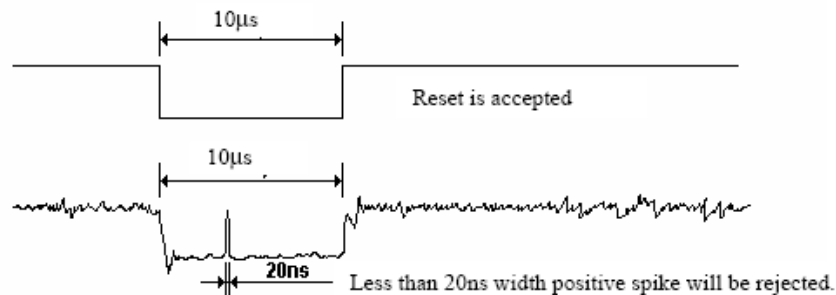
5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.