Layout Guidelines for IS31FL3731-SALS2

Abstract: IS31FL3731-SALS2 is SSOP28 package and it is usually used in display panel of white goods products like washing machine and air-condition, RGB gamming keyboard, or gamming mouse/mouse MAT, etc. IS31FL3731-SALS2 maximum total driving current is about 550mA so the chip power is very large and the layout is very important. Using a good layout can solve many problems especially associated with I2C data transmission stability. The problems due to a bad layout are often seen I2C office feedback non-acknowledge, and the master will get stuck easily.

Some of the main problems are loss of regulation at high output current and/or large input to output voltage differentials, excessive noise on the ground and switch waveforms, and instability. Using the simple guidelines that follow will help minimize these problems.

Key Words: FxLED, IS31FL3731 Layout

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1 Filter Capacitors

When using a low value ceramic (0.1uF) input filter capacitor, it should be located as close to the VCC pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

2 R_{EXT} Current setting resistor

According Formula (1):

$$I_{OUT(Peak)} = 680 / R_{EXT}$$ (1, 680=64.7/(1/10.5), 1/10.5 is the duty cycle)

$$I_{LED} = 64.7 / R_{EXT}$$ (2, same as datasheet formula (2))

R_{EXT} pin is about 1.3V and all the output current reference so R_{EXT} should be located as close to the R_{EXT} pin of the IC as possible too.

3 Signal and Sensing Traces

Signal and sensing pins are responsible for sensing and receiving signals. These traces carry small signals to the device, such as measuring audio through IN pin, control signals from the SDB pin, I2C communication such as SCL and SDA, and so forth.

Signal and sensing traces are the most sensitive to noise; the sensing signal amplitudes are usually measured in mV, which is comparable to the noise amplitude of power traces. Make sure that noisy and power traces are not interfering with signal and sensing traces.

High dv/dt voltage change on one conductor will couple currents to another through the parasitic capacitance. To reduce the noise coupling from the noisy traces, it is necessary to keep the noisy switching paths far from the sensitive small signal traces. If possible, route the noisy and sensitive traces on different layers, with an internal ground layer in between for noise shielding. The following is a list of signal and sensing pins IS31FL373x device family:

SDA and SCL: These pins are used for I2C communication. The data and clock are high frequency and very sensitive impedance tracking and noise. Make sure these traces are as short as possible. Also, an RC filter (100-Ω 100pF) in series is always a good practice.

SDB and INTB: SDB is the shutdown mode enable pin to enable or disable the IC, INTB is Open Drain output that allows the user to know the feedback form IS31FL373x

IN and C_Filt: audio related and the trace usually very short (The IN/C_FILT capacitor is close to the IC).

AD: This pin is used for setting I2C slave address. This pin can't be very long or the IC may not able to get the right slave address and the I2C communication will fail.

REXT: This pin is used for setting the operating current and the trace usually very short (The R_{EXT} resistor is close to the IC).

4 Power Traces

The power traces includes the components that conduct high current such as VCC, GND return. In general, they should be placed first and sized properly. Then, small signal paths are subsequently placed in specific spot in the layout. The large current traces should be short and wide to minimize PCB inductance, resistance and voltage drop. This is especially critical for the traces with high dv/dt pulsating current flow.

5 Layout Recommendations

5.1 Primary Concerns on PCB Layout

The primary concerns when laying a custom IS31FL3731-SALS2 PCB are:

A: GND/VCC connection,

B: REXT connection

C: Thermal dissipation (consider first)

D: SDA/SCL/SDB/INTB/AD connection

E: Other pin connection

5.2 Current Rating Example

For a R_{EXT}=20k application, the current rating for each net is as follows:

- VCC = 544mA, recommend trace width: 0.3mm~0.5mm
- SDA/SCL and other pins< 2 mA, recommend trace width: 0.2mm
- Output CXx = 34mA at 8/9 time and 272mA and 1/9 time, so maximum current is 272mA, recommend trace width: 0.2mm~0.3mm

5.3 Step-by-Step PCB Layout Guidelines

5.3.1 GND/VCC connection, the bypass capacitor (as well as R_{EXT} resistor) should place as close to the IC as possible (#1), especially the GND pin of the cap/res should be close to the IC (#2). After finishing the two wires to the IC, also the power trace from the connector/other power source should consider first (#3).

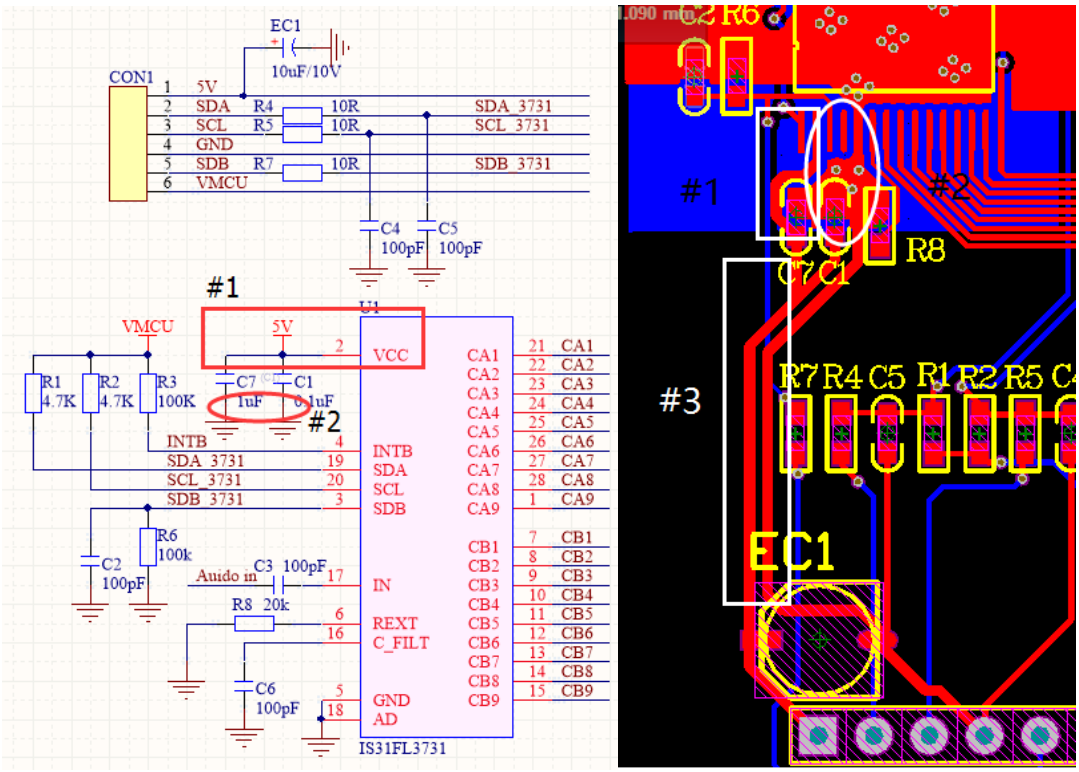

Figure 1 GND/VCC connection

5.3.2 R_{EXT} connection, as the bypass capacitor places as close to the IC as possible, especially the GND pin of the res should be close to the IC.

5.3.3 Thermal dissipation consideration, IS31FL3731-SALS2 doesn't have thermal pad so the chip could be very hot if power is large. So do consider the ground area connects to the GND pin. Other traces should keep away and ensure the ground area below the package is integrality, also the back layer, should also be considered, the via interconnect the top-layer and bottom-layer is also important and must be optimized near the GND pins for thermal.

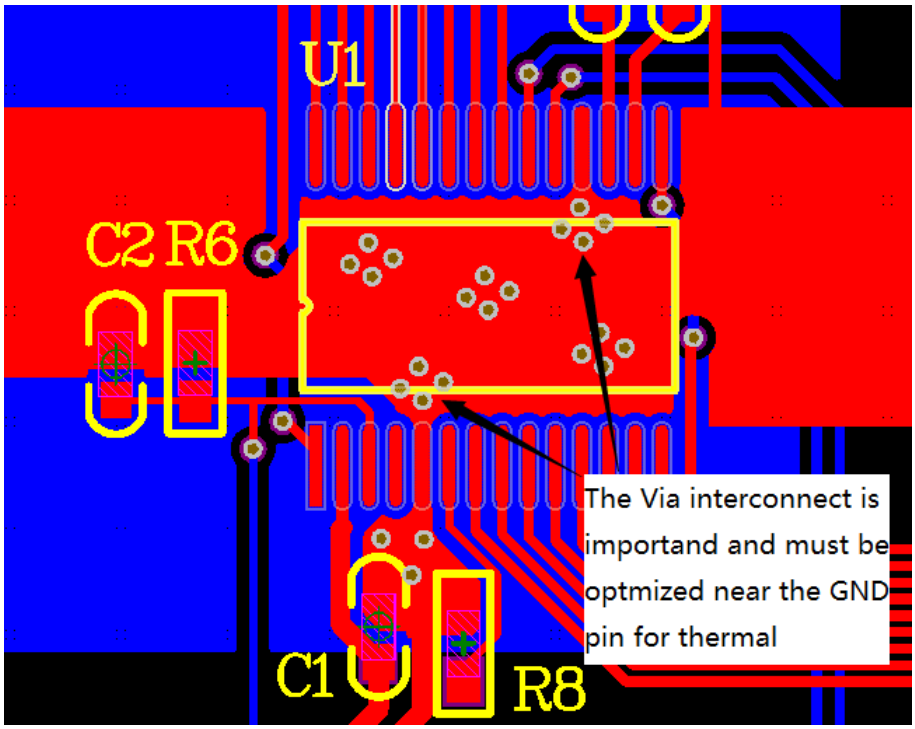

Figure 2 Ground thermal dissipation

5.3.4 SDA/SCL/SDB/INTB/AD and other pin connection. SDA/SCL RC filter and pull-high resistors and all other components don't require much so don't need to be so closed to the IC, this wires should consider to give way to ground area, but still, several points need to think about:

A The SDA/SCL is 400kHz maximum speed and should not in parallel with outputs (CXx) and power traces.

B For those needs to pass the EFT test, the SDB pin should have a 0.1uF capacitor and this capacitor should well grounded (C2).

C AD pin decides the device address and normally connect to GND net, this trace should not be very long, otherwise the master may can't recognize the slave address.

5.3.5 An Layout Example

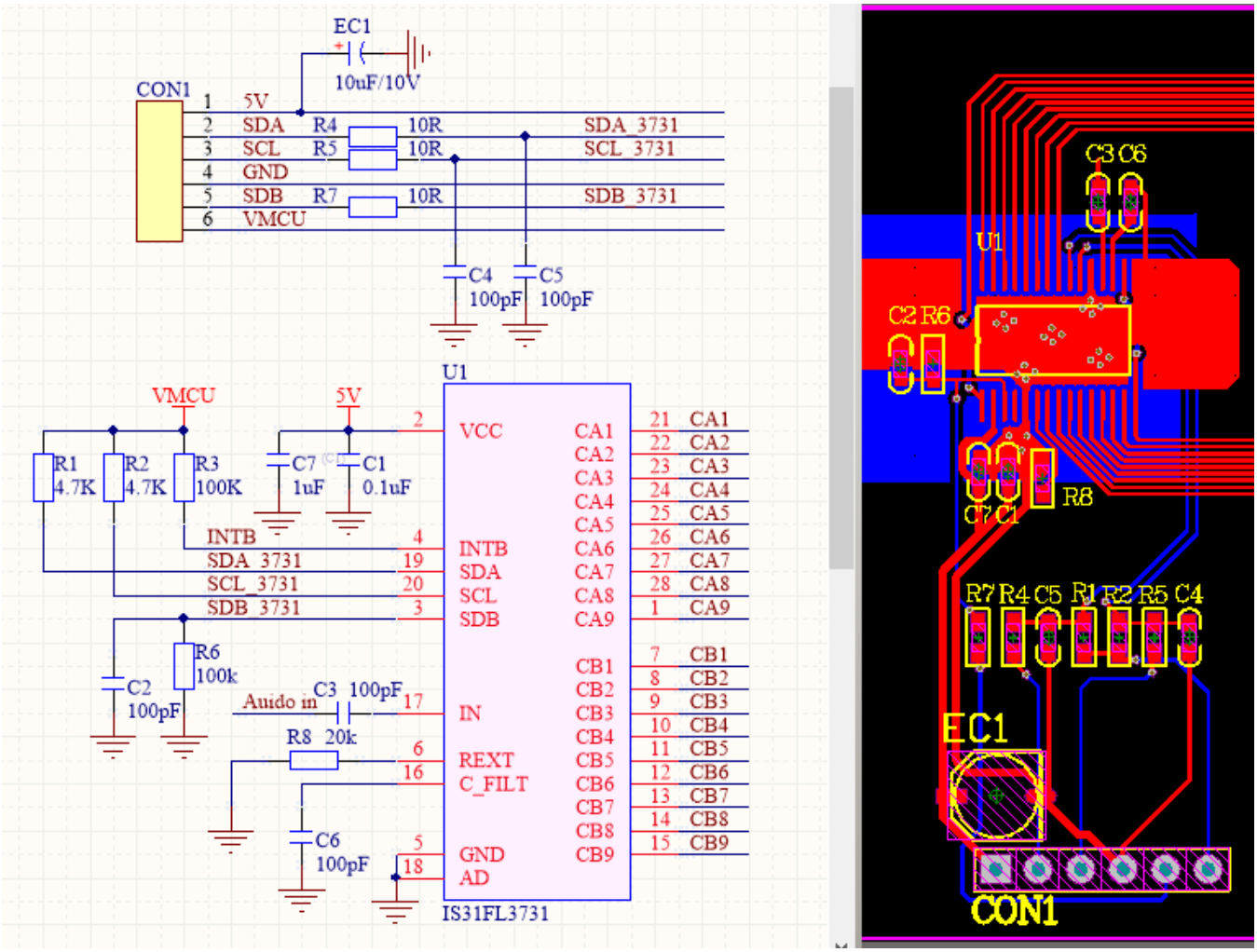

Figure 3 Layout example-Top layer

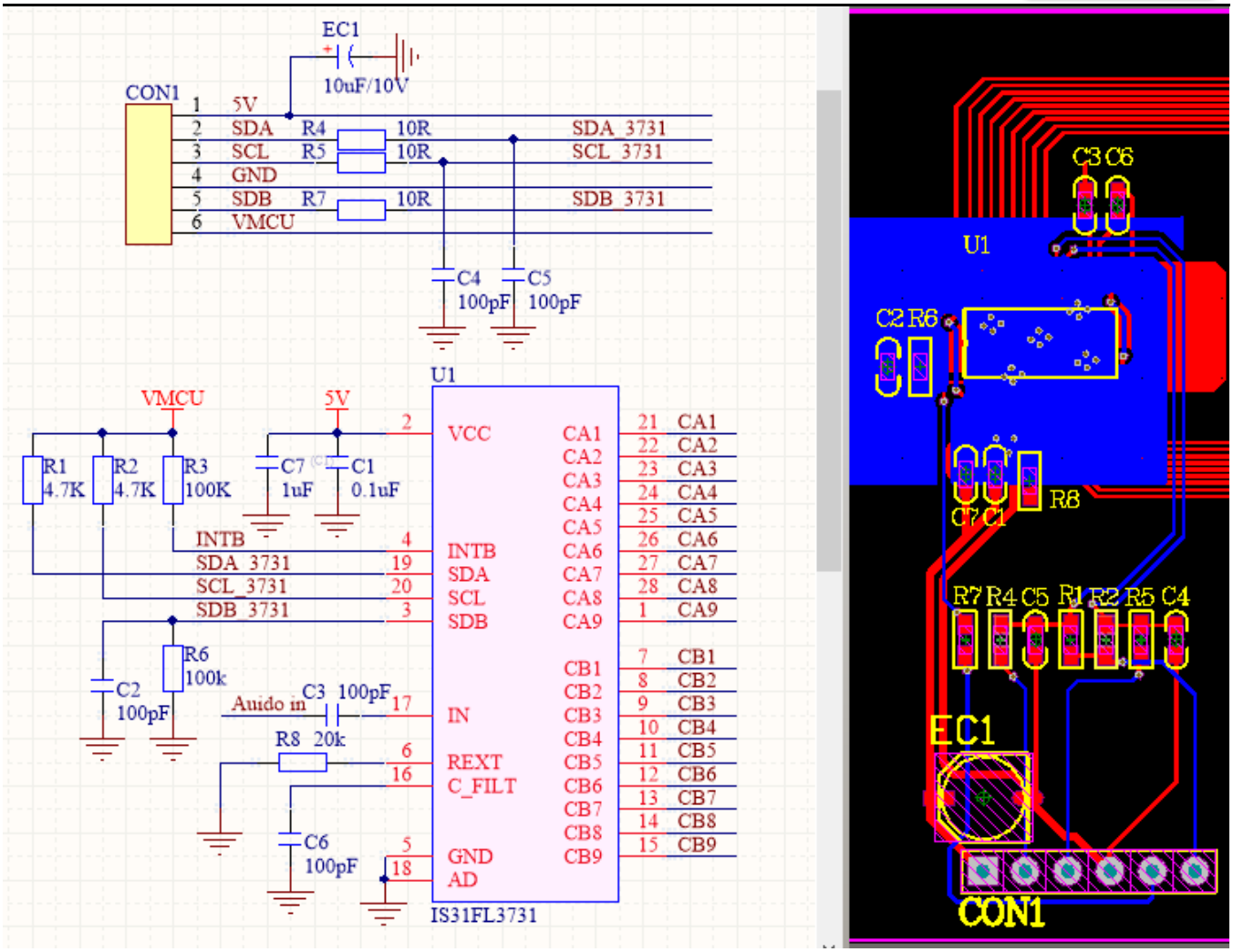

Figure 4 Layout example-Bottom layer

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2017.07.21