Experiment 1
Characterization of a CMOS Inverter

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1 Overview of the experiment

The CMOS inverter is the simplest static complementary CMOS logic gate and also an essential component of all logic gates . In this experiments we characeterized CMOS and observed its DC & AC behaviour, particularly we observed following -

- DC Transfer Characteristics
- Output Characteristics
- Delay Characteristics
- Delay variation with supply voltage
- Current drawn by the Ring Oscillator

For transfer & output characteristics hex inverter IC *MM74C04* was used and for ring measurement tasks, a ring oscillator with 17 inveters was used to obtain a good estimate of the delay.

2 Experiment setup and Obeservation

Each part of the experiment essentially involves the CMOS inverter (IC MM74C04) as the elementary unit.The delay of a single CMOS inverter as their order of magnitude is very smallto measure and that is why a ring

oscillator with 17 inverters was used . The Opamp buffer (TL072) was introduced so that the DSO does not add extra load to the circuit during the measurement.
In further section, Circuit layouts for the various parts of the experiment are shown with relevant details.

Components used :
IC MM74C04 $*4$, TL072, Decoupling Capacitors (0.1 μF) $*2$,
20 KΩ potentiometer, Resistors(1.2KΩ,1Ω))

2.1 DC Transfer Characteristics

The transfer characteristic of the CMOS inverter is the plot of the output voltage as a function of the input voltage. As we vary the input voltage from 0V to V_{DD}, the output voltage will change from V_{DD} to 0V. The point in the transfer characteristics where the input and output voltages equal is called the *Switching point*. This is an important factor for any switching circuit. The observation is tabulated in Table 1 and the characteristics have been plotted in Figure 1.
From these observed values we get that $\mathbf{V}_{SW} \approx \mathbf{2.56V}$.
But as we know that,

$$V_{SW} = \frac{\sqrt{\beta_p}(V_{DD} - V_t) + \sqrt{\beta_n}V_t}{\sqrt{\beta_p} + \sqrt{\beta_n}} \tag{1}$$

Substituting the values we get $\frac{\beta_p}{\beta_n} = 1.3$

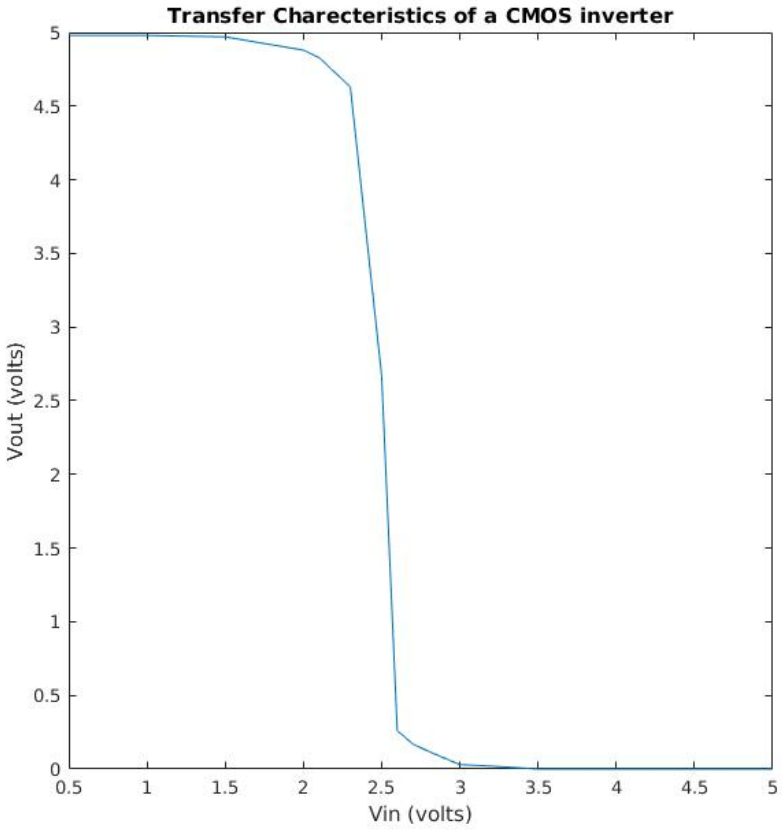

Figure 1: The observed transfer characteristics of the CMOS inverter

Vin (V)	Vout (V)
0.5	4.98
1	4.98
1.5	4.97
2	4.88
2.1	4.83
2.3	4.63
2.5	2.67
2.6	0.26
2.7	0.17
2.8	0.12
3	0.03
3.2	0.02
3.5	0
4	0
5	0

Table 1: DC Transfer Characteristics of the CMOS inverter

2.2 Output Characteristics

In this part we try to measure the output characteristics of the CMOS inverter. The figures 2 and 3 represent the output characteristics of the device.

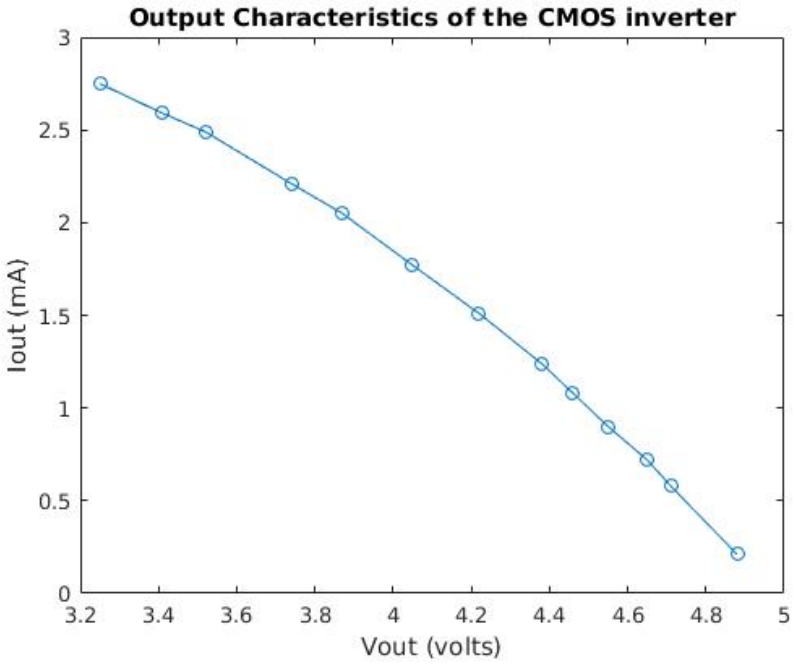

Figure 2: Observed nature of the output characteristics at low input

we can also conclude from the linear characteristics of the graphs that the output impedance of the device is constant. The observed values are given in Table 2 and 3.

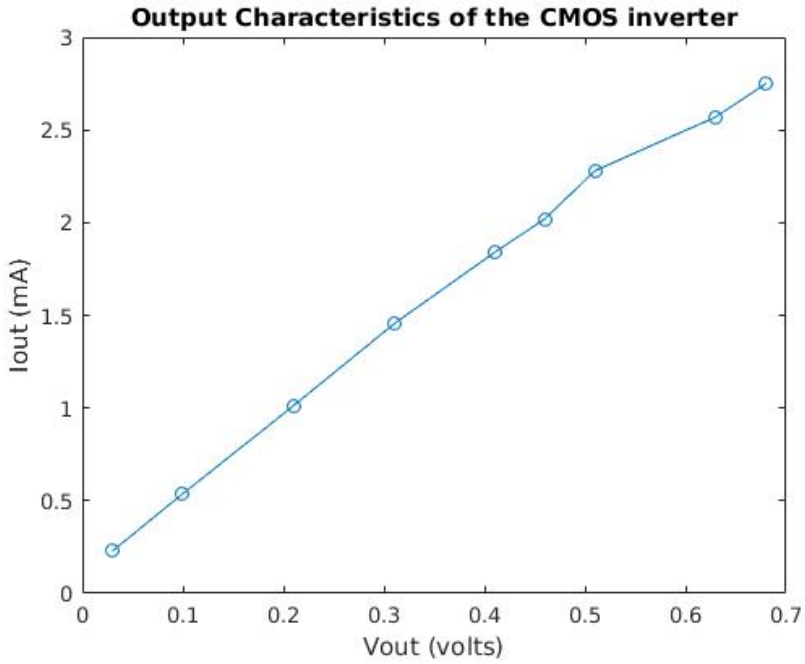

Figure 3: Observed nature of the output characteristics at high input

Vout (V)	**Iout (mA)**
3.25	2.75
3.41	2.59
3.52	2.49
3.74	2.21
3.87	2.05
4.05	1.77
4.22	1.51
4.38	1.24
4.46	1.08
4.55	0.9

Table 2: Output characteristics at low input

Vout (V)	Iout (mA)
0.03	0.229
0.1	0.538
0.21	1.012
0.31	1.454
0.41	1.839
0.46	2.02
0.51	2.28
0.63	2.57
0.68	2.75

Table 3: Output Characteristics at high input

2.3 Delay Characteristics of the CMOS Inverter

In any digital circuit, an important characteristic of any device is the delay caused by it. However, this delay is very small for each independent inverter and hence would require a very sophisticated equipment for measurement. In this part of the experiment we have achieved this task by using a 17- stage ring oscillator.

The delay in this circuit can be modelled as-

$$d_{abs} = k_o + k_1 C_{load} \tag{2}$$

Here, k_o and k_1 are constants, C_{load} is the load capacitance being driven by the inverter, and d_{abs} is the delay measured in seconds. It is convenient to express the C_{load} as a multiple of the input capacitance C_{in} of the inverter. The equation (2) can be re-written as-

$$d_{abs} = k_o + \tau_{inv} \frac{C_{load}}{C_{in}} \tag{3}$$

The delay can be expressed in multiples of τ_{inv} as

$$d_{inv} = p_{inv} + \frac{C_{load}}{C_{in}} \tag{4}$$

where, $p_{inv} = \frac{k_o}{\tau_{inv}}$

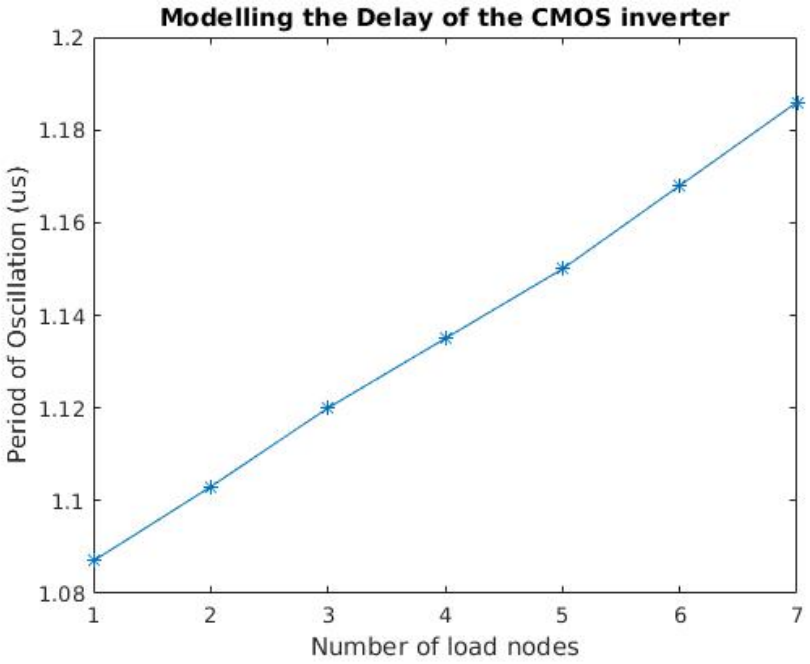

Figure 4: Variation of the time period of oscillation with respect to the number of loads at V_{DD}= 5V

In table 4, the observed data for the variation of frequency or time period with load is presented. The results are summarized in the figure 4 and the snapshots are presented in Table 5.

Number of Load	**Time Period (μs)**
1	1.087
2	1.103
3	1.12
4	1.135
5	1.15
6	1.168
7	1.186

Table 4: Variation of time period with number of loads

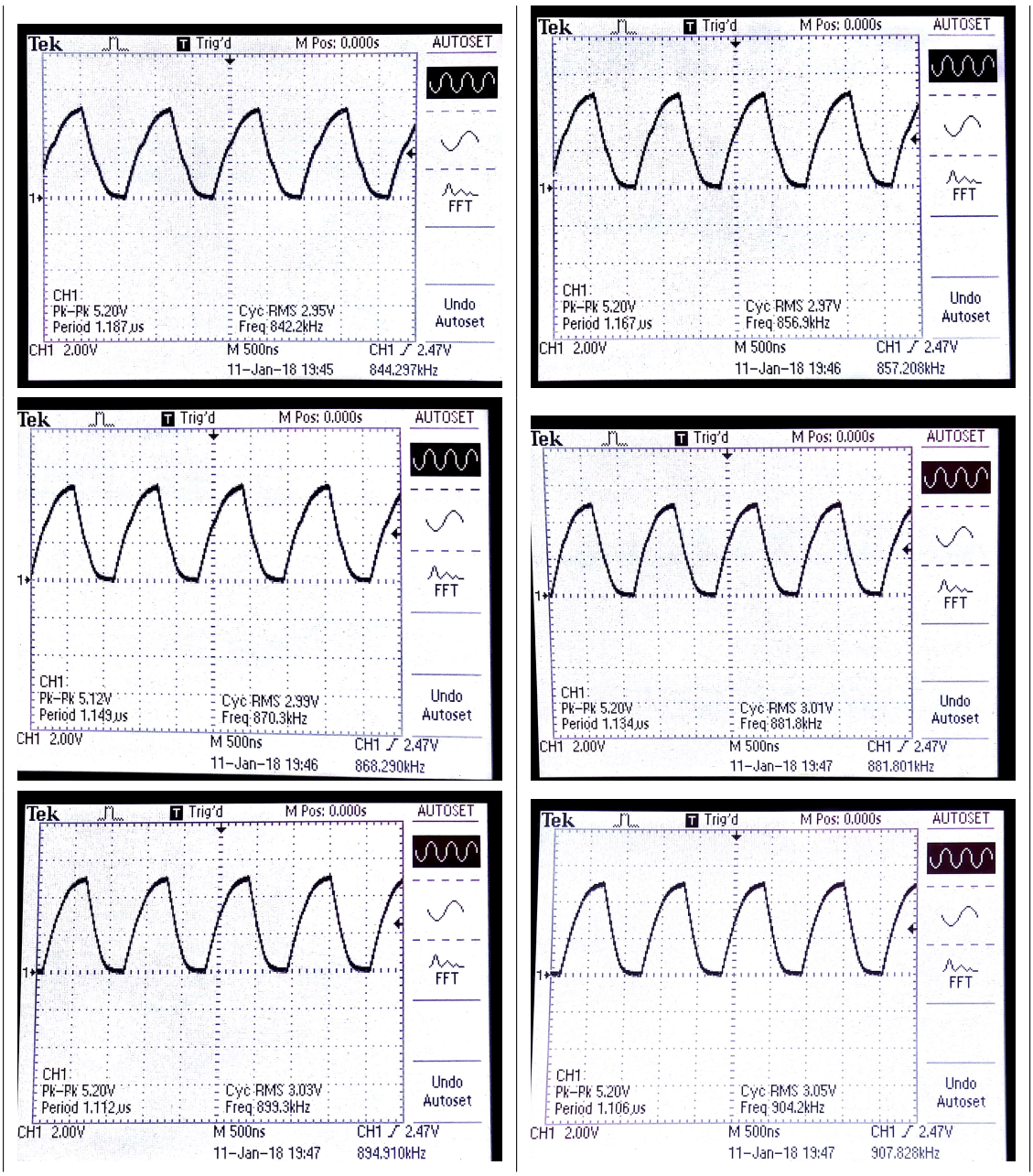

Table 5: Snapshots at different number of loads VDD=5V

The time period of oscillation is given by

$$\tau_{inv} \times (34p_{inv} + (32 + (2 \times (1 + Additionaloutputload))) \tag{5}$$

As the rise and fall times are equal we have,

$$Slope = 2\tau_{inv} = 0.019\mu s \tag{6}$$

$$Intercept = 34\tau_{inv}(p_{inv} + 1) = 1.07 \tag{7}$$

$$\tau_{inv} = 0.008\mu s \tag{8}$$

$$p_{inv} = 2.13 \tag{9}$$

2.4 Delay variation with Supply Voltage

The delay of the CMOS inverter varies with the supply voltage V_{DD}. This dependency is given below-

$$Time\ Period\ \alpha\ \frac{V_{DD}}{(V_{DD} - V_t)^2} \tag{10}$$

This part of the experiment is meant to verify this relation experimentally. The observed values are presented in Table 6.

$\mathbf{V_{DD}}$ **(V)**	**Time Period** (μs)
3	2.42
3.5	2.112
4	1.612
4.5	1.325
5	1.09
5.5	0.956
6	0.861

Table 6: Variation of time period of oscillation with Vdd at load=2

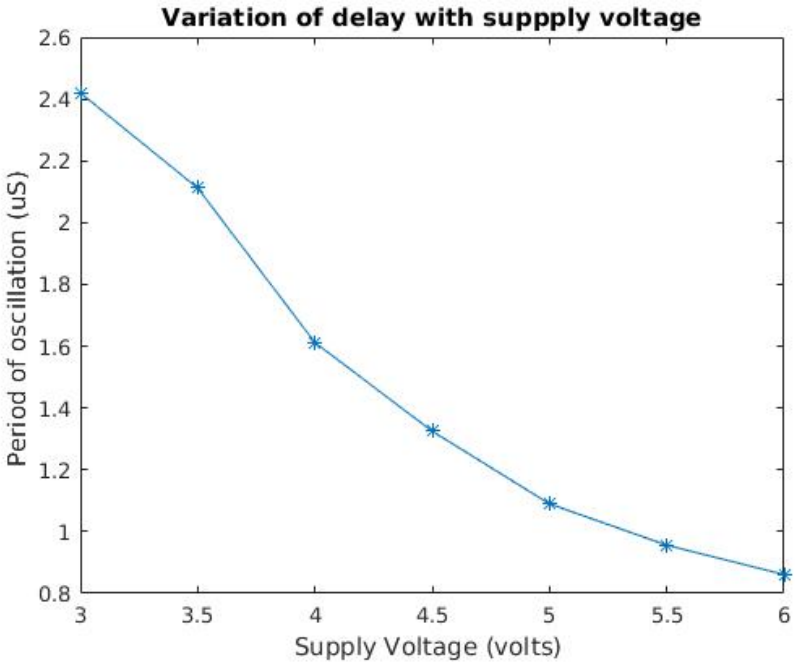

Figure 5: Variation of time period of oscillation with sipply voltage(V_{DD}) at load = 2

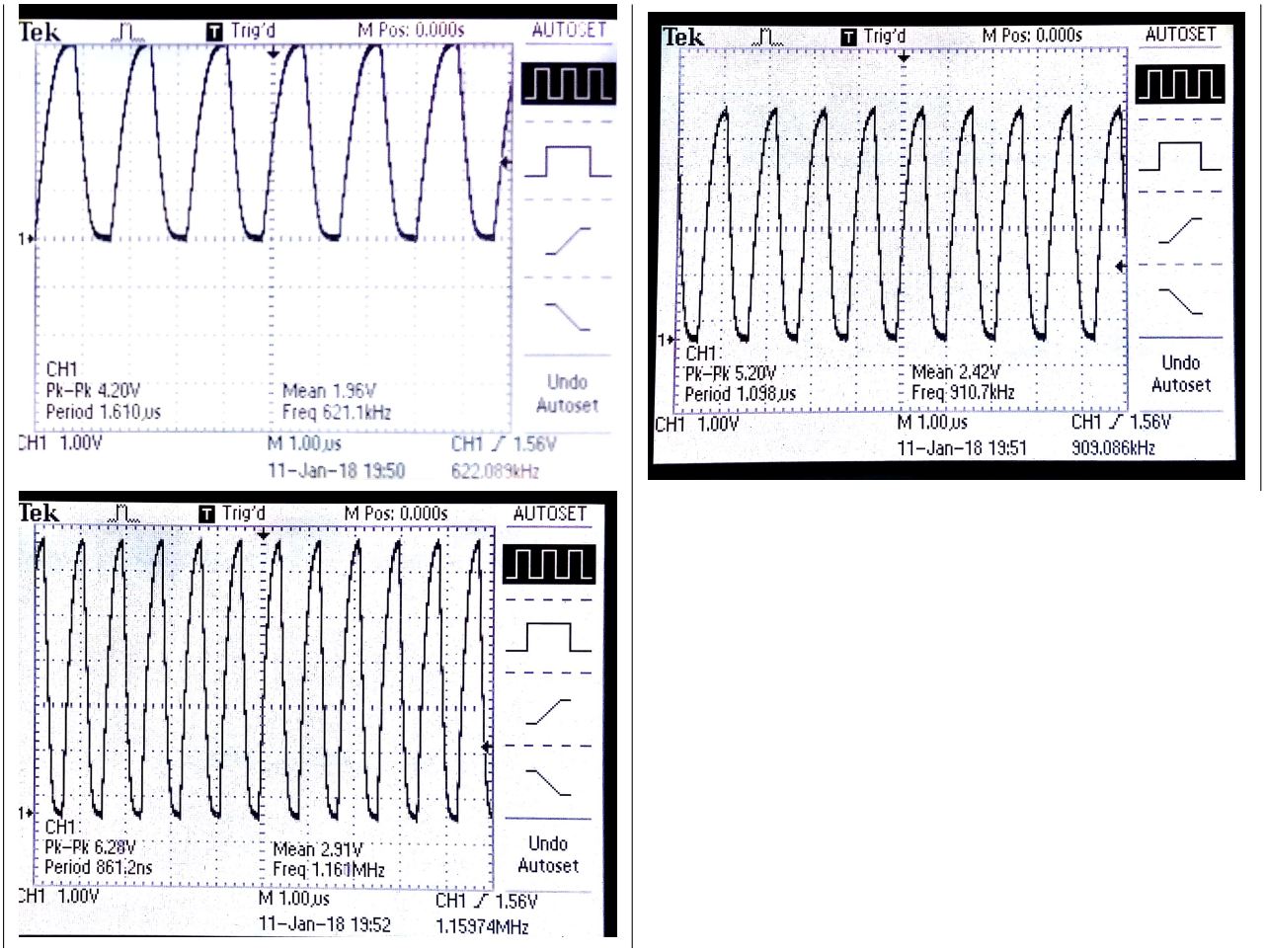

Table 7: Snaps of DSO for load = 2 at V_{DD} 4V, 5V and 6V respectively

2.5 Current drawn by the Ring Oscillator

As in the CMOS technology the steady power loss is zero and so is the current and so when the inverter output switches from low to high or vice versa,it draws current from the power supply.In the experimental set up, the current drawn by the ring oscillator is the sum of the currents drawn by the individual inverters which can be seen in the snapshot of the DSO below.

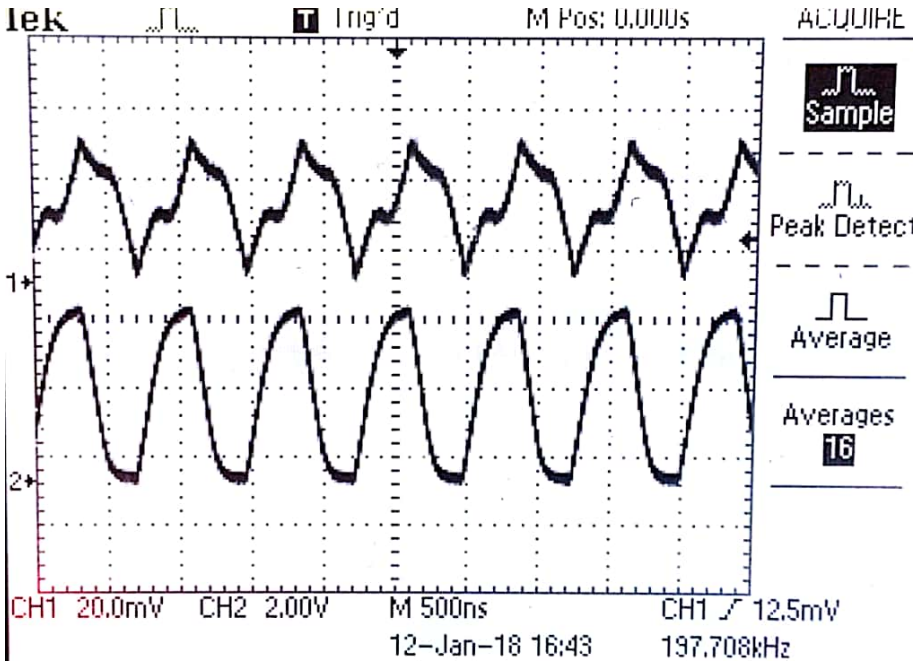

Figure 6: Snapshot of the DSO measuring the switching current and Vout

The measured values of $<\mathbf{I}>$= 2.1 mA and $\mathbf{I}_{P-P}$**=20.9 mA.**