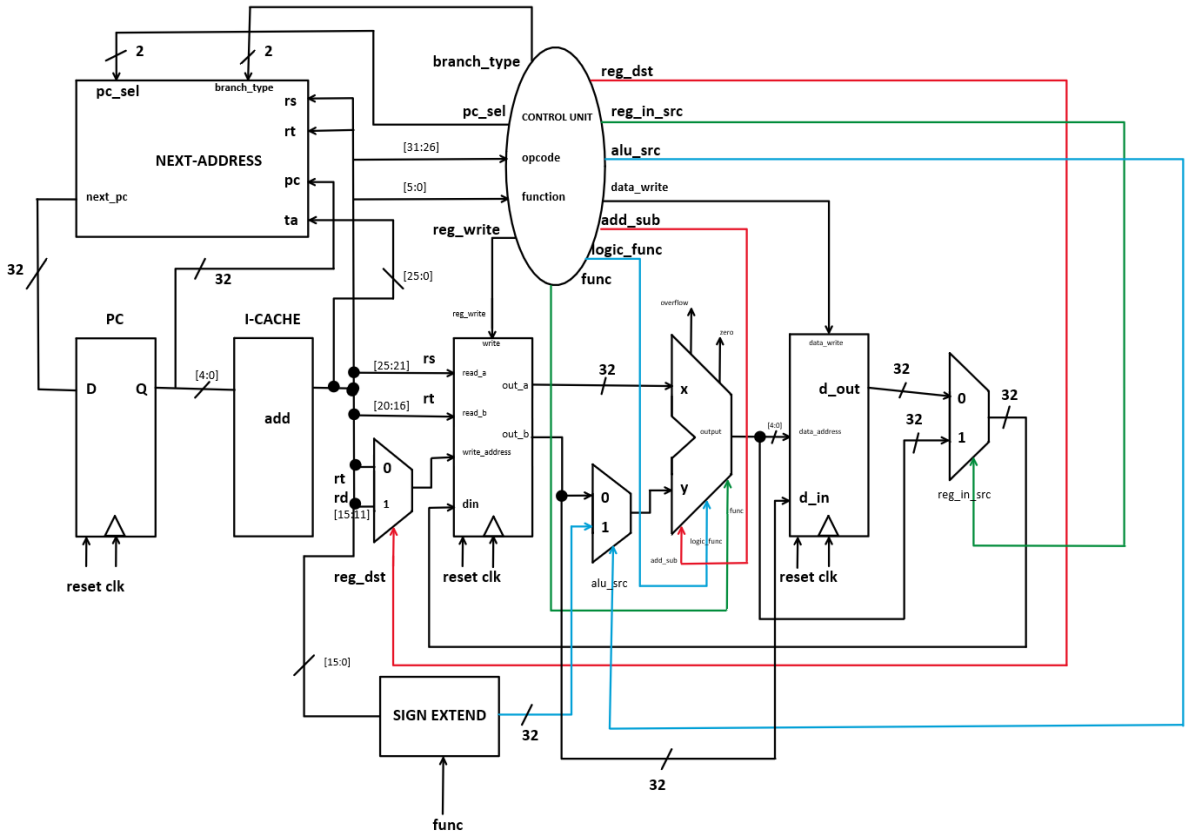
CONCORDIA UNIVERSITY
Department of Electrical and Computer Engineering
COEN 316 Computer Architecture and Design
Lab 4
Datapath Design & Control Unit and Testing
Summer 2021
Umaid Malik
27576110

PART: 1 Datapath Design

Objective

This part of the lab requires us to design the Datapath for CPU components made in previous labs. More component will be needed to complete the Datapath design. These additional hardware components are the Program Counter register, I-Cache, Sign Extend unit, D-Cache, and three 2-to-1 muxes.

Complete Datapath



PC Register ModelSim Result

```
[poise] [/home/u/u_mal/COEN316/LAB4/Code] >
[poise] [/home/u/u_mal/COEN316/LAB4/Code] >
[poise] [/home/u/u_mal/COEN316/LAB4/Code] > vsim -c -do ../DO/pc_reg.do pc_reg
Reading /nfs/sw_cmc/x86_64.EL7/tools/mentor.2011/modelsim_6.6g/modeltech/tcl/vsim/pref.tcl

# 6.6g

# vsim -do ../DO/pc_reg.do -c pc_reg
# ** Note: (vsim-3812) Design is being optimized...
# //  ModelSim SE-64 6.6g May 23 2012 Linux 3.10.0-1160.24.1.el7.x86_64
# //
# //  Copyright 1991-2012 Mentor Graphics Corporation
# //             All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND
# //  PROPRIETARY INFORMATION WHICH IS THE PROPERTY
# //  OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading ieee.std_logic_arith(body)
# Loading ieee.std_logic_unsigned(body)
# Loading work.pc_reg(pc_reg_arch)#1
# do ../DO/pc_reg.do
# 1 0 00000000000000000000000000000000 00000
# 00000000
# 0 1 11111111001100110000001100010111 10111
# FF330317
# 1 1 00000000000000000000000000000000 00000
# 00000000
#
#
VSIM 2>
```

	reset	clk	out_pc	q
Run # 1	**1**	**0**	**0000 0000 0000 0000 0000 0000 0000 0000 (0x00000000)**	**00000**
Run # 2	**0**	**1**	**1111 1111 0011 0011 0000 0011 0001 0111 (0xFF330317)**	**10111**
Run # 3	**1**	**1**	**0000 0000 0000 0000 0000 0000 0000 0000 (0x00000000)**	**00000**

I-Cache ModelSim Result

```
[poise] [/home/u/u_mal/COEN316/LAB4/Code] > vcom i_cache.vhd
Model Technology ModelSim SE-64 vcom 6.6g Compiler 2012.05 May 23 2012
-- Loading package standard
-- Loading package std_logic_1164
-- Loading package std_logic_arith
-- Loading package std_logic_unsigned
-- Compiling entity i_cache
-- Compiling architecture i_cache_arch of i_cache
[poise] [/home/u/u_mal/COEN316/LAB4/Code] > vsim -c -do ../DO/i_cache.do i_cache
Reading /nfs/sw_cmc/x86_64.EL7/tools/mentor.2011/modelsim_6.6g/modeltech/tcl/vsim/pref.tcl

# 6.6g

# vsim -do ../DO/i_cache.do -c i_cache
# ** Note: (vsim-3812) Design is being optimized...
# //  ModelSim SE-64 6.6g May 23 2012 Linux 3.10.0-1160.24.1.el7.x86_64
# //
# //  Copyright 1991-2012 Mentor Graphics Corporation
# //             All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND
# //  PROPRIETARY INFORMATION WHICH IS THE PROPERTY
# //  OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading ieee.std_logic_arith(body)
# Loading ieee.std_logic_unsigned(body)
# Loading work.i_cache(i_cache_arch)#1
# do ../DO/i_cache.do
# 00000
# 00100000000000110000000000000000
# 20030000
# 00001
# 00100000000000010000000000000000
# 20010000
# 00010
# 00100000000000010000000000000101
# 20020005
# 00011
# 00000000001000100000100000100000
# 00220820
# 00100
# 00100000010000101111111111111111
# 2042FFFF
# 00101
# 00010000010000110000000000000001
# 10430001
```

	input_address	output_instruction
Run # 1	**00000**	**0010 0000 0000 0011 0000 0000 0000 0000 (0x20030000)**
Run # 2	**00001**	**0010 0000 0000 0001 0000 0000 0000 0000 (0x20010000)**
Run # 3	**00010**	**0010 0000 0000 0010 0000 0000 0000 0101 (0x20020005)**
Run # 4	**00011**	**0000 0000 0010 0010 0000 1000 0010 0000 (0x00220820)**
Run # 5	**00100**	**0010 0000 0100 0010 1111 1111 1111 1111 (0x2042FFFF)**
Run # 6	**00101**	**0001 0000 0100 0011 0000 0000 0000 0001 (0x10430001)**
Run # 7	**00110**	**0000 1000 0000 0000 0000 0000 0000 0011 (0x08000003)**

Sign-Extend ModelSim Result

```
Reading /nfs/sw_cmc/x86_64.EL7/tools/mentor.2011/modelsim_6.6g/modeltech/tcl/vsim/pref.tcl

# 6.6g

# vsim -do ../DO/sign_extend.do -c sign_extend
# ** Note: (vsim-3812) Design is being optimized...
# //  ModelSim SE-64 6.6g May 23 2012 Linux 3.10.0-1160.24.1.el7.x86_64
# //
# //  Copyright 1991-2012 Mentor Graphics Corporation
# //             All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND
# //  PROPRIETARY INFORMATION WHICH IS THE PROPERTY
# //  OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading ieee.std_logic_arith(body)
# Loading ieee.std_logic_signed(body)
# Loading work.sign_extend(sign_arch)#1
# do ../DO/sign_extend.do
# 00
# 1000111100110011
# 8F33
# 10001111001100110000000000000000
# 8F330000
# 01
# 1000111100110011
# 8F33
# 11111111111111111000111100110011
# FFFF8F33
# 10
# 1000111100110011
# 8F33
# 11111111111111111000111100110011
# FFFF8F33
# 11
# 1000111100110011
# 8F33
# 00000000000000001000111100110011
# 00008F33
#
#
VSIM 2>
VSIM 2>
VSIM 2>
VSIM 2>
```

	in_16bit	func	out_32bit
Run # 1	**1000 1111 0011 0011 (0x8F33)**	**00**	**1000 1111 0011 0011 0000 0000 0000 0000 (0x8F330000)**
Run # 2	**1000 1111 0011 0011 (0x8F33)**	**01**	**1111 1111 1111 1111 1000 1111 0011 0011 (0xFFFF8F33)**
Run # 3	**1000 1111 0011 0011 (0x8F33)**	**10**	**1111 1111 1111 1111 1000 1111 0011 0011 (0xFFFF8F33)**
Run # 4	**1000 1111 0011 0011 (0x8F33)**	**11**	**0000 0000 0000 0000 1000 1111 0011 0011 (0x00008F33)**

D-Cache ModelSim Result

```
Model Technology ModelSim SE-64 vcom 6.6g Compiler 2012.05 May 23 2012
-- Loading package standard
-- Loading package std_logic_1164
-- Loading package std_logic_arith
-- Loading package std_logic_unsigned
-- Compiling entity d_cache
-- Compiling architecture d_cache_arch of d_cache
[poise] [/home/u/u_mal/COEN316/LAB4/Code] >
[poise] [/home/u/u_mal/COEN316/LAB4/Code] > vsim -c -do ../DO/d_cache.do d_cache
Reading /nfs/sw_cmc/x86_64.EL7/tools/mentor.2011/modelsim_6.6g/modeltech/tcl/vsim/pref.tcl

# 6.6g

# vsim -do ../DO/d_cache.do -c d_cache
# ** Note: (vsim-3812) Design is being optimized...
# //  ModelSim SE-64 6.6g May 23 2012 Linux 3.10.0-1160.24.1.el7.x86_64
# //
# //  Copyright 1991-2012 Mentor Graphics Corporation
# //             All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND
# //  PROPRIETARY INFORMATION WHICH IS THE PROPERTY
# //  OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading ieee.std_logic_arith(body)
# Loading ieee.std_logic_unsigned(body)
# Loading work.d_cache(d_cache_arch)#1
# do ../DO/d_cache.do
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 0  Instance: /d_cache
# ** Warning: CONV_INTEGER: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, and it has been converted to 0.
#    Time: 0 ns  Iteration: 0  Instance: /d_cache
# 0 1 1 00001
# FDFEA73C
# 0 0 1 00001
# FDFEA73C
# 0 1 1 00010
# FFEFBFED
# 0 1 0 00001
# FDFEA73C
# 1 1 0 00001
# 00000000
# 1 1 0 00010
# 00000000
#
#
VSIM 2>
```

	reset	clk	data_write	data_address	d_in	d_out
Run # 1	**0**	**1**	**1**	**00001**	**0xFDFEA73C**	**0xFDFEA73C**
Run # 2	**0**	**0**	**1**	**00001**	**0xFDFEA73C**	**0xFDFEA73C**
Run # 3	**0**	**1**	**1**	**00010**	**0xFFEFBFED**	**0xFFEFBFED**
Run # 4	**0**	**1**	**0**	**00001**	**0xFFEFBFED**	**0xFDFEA73C**
Run # 5	**1**	**1**	**0**	**00001**	**0xFFEFBFED**	**0x00000000**
Run # 6	**1**	**1**	**0**	**00010**	**0xFFEFBFED**	**0x00000000**

Part 1 Summary

All the new VHDL components were simulated to verify the correct logic before moving onto the second part. The control unit in the design will be used as VHDL process.

DO file: pc_reg.do

```
force reset 1
force clk 0
force d X"00000000"
run 2
examine reset clk out_pc q
examine -radix X out_pc

force reset 0
force clk 1
force d X"FF330317"
run 2
examine reset clk out_pc q
examine -radix X out_pc

force reset 1
run 2
examine reset clk out_pc q
examine -radix X out_pc
```

DO file: i_cache.do

```
force input_address 00000
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 00001
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 00010
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 00011
run 2
```

```
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 00100
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 00101
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 00110
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 00111
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 01000
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 01001
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 01010
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction
```

```
force input_address 01011
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction

force input_address 01100
run 2
examine input_address
examine output_instruction
examine -radix X output_instruction
```

DO file: sign_extend.do

```
force in_16bit 1000111100110011
force func 00
run 2

examine func
examine in_16bit
examine -radix X in_16bit
examine out_32bit
examine -radix X out_32bit

force func 01
run 2

examine func
examine in_16bit
examine -radix X in_16bit
examine out_32bit
examine -radix X out_32bit

force func 10
run 2

examine func
examine in_16bit
examine -radix X in_16bit
examine out_32bit
examine -radix X out_32bit

force func 11
run 2
```

```
examine func
examine in_16bit
examine -radix X in_16bit
examine out_32bit
examine -radix X out_32bit
```

DO file: d_cache.do

```
force reset 1
force clk 0
force data_write 0
force data_address 00000
force d_in X"00000000"
run 2

force reset 0
force clk 1
force data_write 1
force data_address 00001
force d_in X"FDFEA73C"
run 2
examine reset clk data_write data_address
examine -radix X d_out

force clk 0
run 2
examine reset clk data_write data_address
examine -radix X d_out

force data_address 00010
force d_in X"FFEFBFED"
force clk 1
run 2
examine reset clk data_write data_address
examine -radix X d_out

force data_write 0
force data_address 00001
run 2
examine reset clk data_write data_address
examine -radix X d_out

force reset 1
run 2
examine reset clk data_write data_address
examine -radix X d_out
```

```
force data_address 00010
run 2
examine reset clk data_write data_address
examine -radix X d_out
```

VHDL file: pc_reg.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity pc_reg is
port(
        reset       : in std_logic;
        clk         : in std_logic;
        d           : in std_logic_vector(31 downto 0);
        out_pc      : out std_logic_vector(31 downto 0);
        q           : out std_logic_vector(4 downto 0)
    );
end pc_reg;

architecture pc_reg_arch of pc_reg is

begin
    process(reset, clk, d)
    begin
        if (reset = '1') then
            out_pc <= (others => '0');
            q <= (others => '0');
        elsif (rising_edge(clk)) then
            out_pc <= d;
            q <= d(4 downto 0);
        end if;
    end process;


end pc_reg_arch;
```

VHDL file: i_cache.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity i_cache is
```

```
port(
    input_address       : in std_logic_vector(4 downto 0);
    output_instruction  : out std_logic_vector(31 downto 0)
    );
end i_cache;

architecture i_cache_arch of i_cache is

begin
    process(input_address)
    begin
        case input_address is
            when "00000" => output_instruction <= "00100000000000110000000000000000"; -- addi r3, r0, 0
            when "00001" => output_instruction <= "00100000000000010000000000000000"; -- addi r1, r0, 0
            when "00010" => output_instruction <= "00100000000000100000000000000101"; -- addi r2, r0, 5
            when "00011" => output_instruction <= "00000000001000100000100000100000"; -- add  r1, r1, r2
            when "00100" => output_instruction <= "00100000100000101111111111111111"; -- addi r2, r2, -1
            when "00101" => output_instruction <= "00010000100000110000000000000001"; -- beq  r2, r3 (+1) THERE
            when "00110" => output_instruction <= "00001000000000000000000000000011"; -- jump 3 (LOOP)
            when "00111" => output_instruction <= "10101100000000010000000000000000"; -- sw   r1, 0(r0)
            when "01000" => output_instruction <= "10001100000001000000000000000000"; -- lw   r4, 0(r0)
            when "01001" => output_instruction <= "00110000100001000000000000001010"; -- andi r4, r4, 0x000A
            when "01010" => output_instruction <= "00110100100001000000000000000001"; -- ori  r4, r4, 0x0001
            when "01011" => output_instruction <= "00111000100001000000000000001011"; -- xori r4, r4, 0xB
            when "01100" => output_instruction <= "00111000100001000000000000000000"; -- xori r4, r4, 0x0000
            when others  => output_instruction <= "00000000000000000000000000000000"; -- don't care
        end case;
    end process;
end i_cache_arch;
```

VHDL file: sign_extend.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity sign_extend is
port(
        in_16bit    : in std_logic_vector(15 downto 0);
        func        : in std_logic_vector(1 downto 0);
        out_32bit   : out std_logic_vector(31 downto 0)
    );
end sign_extend;

architecture sign_arch of sign_extend is

begin
    process(in_16bit, func)
    begin
        case func is
            when "00" => out_32bit <= (in_16bit & (15 downto 0 => '0')); -
- load upper immediate
            when "01" => out_32bit <= ((31 downto 16 => in_16bit(15)) & in_16bit(
15 downto 0)); -- set less immediate
            when "10" => out_32bit <= ((31 downto 16 => in_16bit(15)) & in_16bit(
15 downto 0)); -- arithmetic
            when "11" => out_32bit <= ((31 downto 16 => '0') & in_16bit); -
- logical
            when others =>
        end case;
    end process;
end sign_arch;
```

VHDL file: d_cache.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity d_cache is
port(
    reset           : in std_logic;
    clk             : in std_logic;
    data_write      : in std_logic;
```

```
    data_address    : in std_logic_vector(4 downto 0);
    d_in            : in std_logic_vector(31 downto 0);
    d_out           : out std_logic_vector(31 downto 0)
    );
end d_cache;

architecture d_cache_arch of d_cache is

type d_cache_array is array (0 to 31) of std_logic_vector(31 downto 0);
signal d_cache_data: d_cache_array;

begin
    process(data_address, d_cache_data)
    begin
        d_out <= d_cache_data(conv_integer(data_address));
    end process;

    process(d_in, reset, clk, data_write, data_address, d_cache_data)
    begin
        if (reset = '1') then
            for i in 0 to 31 loop
                d_cache_data(i) <= (others => '0');
            end loop;

        elsif ((rising_edge(clk)) AND (data_write = '1')) then
            d_cache_data(conv_integer(data_address)) <= d_in;
        end if;
    end process;
end d_cache_arch;
```

XDC: pc_reg.xdc

```
# Vivado does not support old UCF syntax
# must use XDC syntax

# input port(s) are left unspecified
# of the Nexys board
# output port(s) is left unspecified
#
# we use the set_property IOSTANDARD LVCMOS33 to eliminate
# the error during bitgen about unspecified IOSTANDARD
# without bothering to specify any mapping of ports to pins
# since we will not be downloading to the FPGA board

# XDC file for pc_reg.vhd
```

```
set_property  IOSTANDARD LVCMOS33  [ get_ports { reset }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { clk }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { d }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { out_pc }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { q }  ] ;
```

XDC: i_cache.xdc

```
# Vivado does not support old UCF syntax
# must use XDC syntax

# input port(s) are left unspecified
# of the Nexys board
# output port(s) is left unspecified
#
# we use the set_property IOSTANDARD LVCMOS33 to eliminate
# the error during bitgen about unspecified IOSTANDARD
# without bothering to specify any mapping of ports to pins
# since we will not be downloading to the FPGA board

# XDC file for i_cache.vhd

set_property  IOSTANDARD LVCMOS33  [ get_ports { input_address }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { output_instruction }  ] ;
```

XDC: sign_extend.xdc

```
# Vivado does not support old UCF syntax
# must use XDC syntax

# input port(s) are left unspecified
# of the Nexys board
# output port(s) is left unspecified
#
# we use the set_property IOSTANDARD LVCMOS33 to eliminate
# the error during bitgen about unspecified IOSTANDARD
# without bothering to specify any mapping of ports to pins
# since we will not be downloading to the FPGA board

# XDC file for sign_extend.vhd

set_property  IOSTANDARD LVCMOS33  [ get_ports { in_16bit }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { func }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { out_32bit }  ] ;
```

XDC: d_cache.xdc

```
# Vivado does not support old UCF syntax
```

```
# must use XDC syntax

# input port(s) are left unspecified
# of the Nexys board
# output port(s) is left unspecified
#
# we use the set_property IOSTANDARD LVCMOS33 to eliminate
# the error during bitgen about unspecified IOSTANDARD
# without bothering to specify any mapping of ports to pins
# since we will not be downloading to the FPGA board

# XDC file for d_cache.vhd

set_property  IOSTANDARD LVCMOS33  [ get_ports { reset }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { clk }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { data_write }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { data_address }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { d_in }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { d_out }  ] ;
```

TCL Vivado synthesis script: pc_reg.tcl

```
# TCL script for running vivado in batch mode to synthesize pc_reg.vhd

# To run the script first source the Vivado env file:
# source /CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/settings64_CMC_central_lic
ense.csh
#
#Then issue the following command from the Linux prompt:
# vivado -log pc_reg.log -mode batch -source pc_reg.tcl

# read in the VHDL source code files and the xdc constraints file

# to allow for unconstrained ports
# we must set this property, this will
# generated only Warnings about unconstrained ports, but no errors
# and bitgen will generate the .bit file
# we intentionally did not specify any pin constraints in the
# .xdc file since we are not programming the board

set_property SEVERITY {Warning} [get_drc_checks UCIO-1]


read_vhdl  { ./Code/pc_reg.vhd }
read_xdc  pc_reg.xdc
```

```
# the -top refers to the top level VHDL entity name
# the -part specfies the target Xilinx FPGA

synth_design -top pc_reg -part xc7a100tcsg324-1
opt_design
place_design
route_design

# generate the bitsteam file
write_bitstream -force pc_reg.bit
```

TCL Vivado synthesis script: i_cache.tcl

```
# TCL script for running vivado in batch mode to synthesize i_cache.vhd

# To run the script first source the Vivado env file:
# source /CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/settings64_CMC_central_lic
ense.csh
#
#Then issue the following command from the Linux prompt:
# vivado -log i_cache.log -mode batch -source i_cache.tcl

# read in the VHDL source code files and the xdc constraints file

# to allow for unconstrained ports
# we must set this property, this will
# generated only Warnings about unconstrained ports, but no errors
# and bitgen will generate the .bit file
# we intentionally did not specify any pin constraints in the
# .xdc file since we are not programming the board

set_property SEVERITY {Warning} [get_drc_checks UCIO-1]


read_vhdl  { ./Code/i_cache.vhd }
read_xdc  i_cache.xdc

# the -top refers to the top level VHDL entity name
# the -part specfies the target Xilinx FPGA

synth_design -top i_cache -part xc7a100tcsg324-1
opt_design
place_design
route_design
```

```
# generate the bitsteam file
write_bitstream -force i_cache.bit
```

TCL Vivado synthesis script: sign_extend.tcl

```
# TCL script for running vivado in batch mode to synthesize sign_extend.vhd

# To run the script first source the Vivado env file:
# source /CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/settings64_CMC_central_lic
ense.csh
#
#Then issue the following command from the Linux prompt:
# vivado -log sign_extend.log -mode batch -source sign_extend.tcl

# read in the VHDL source code files and the xdc constraints file

# to allow for unconstrained ports
# we must set this property, this will
# generated only Warnings about unconstrained ports, but no errors
# and bitgen will generate the .bit file
# we intentionally did not specify any pin constraints in the
# .xdc file since we are not programming the board

set_property SEVERITY {Warning} [get_drc_checks UCIO-1]


read_vhdl  { ./Code/sign_extend.vhd }
read_xdc  sign_extend.xdc

# the -top refers to the top level VHDL entity name
# the -part specfies the target Xilinx FPGA

synth_design -top sign_extend -part xc7a100tcsg324-1
opt_design
place_design
route_design

# generate the bitsteam file
write_bitstream -force sign_extend.bit
```

TCL Vivado synthesis script: d_cache.tcl

```
# TCL script for running vivado in batch mode to synthesize d_cache.vhd

# To run the script first source the Vivado env file:
```

```
# source /CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/settings64_CMC_central_lic
ense.csh
#
#Then issue the following command from the Linux prompt:
# vivado -log d_cache.log -mode batch -source d_cache.tcl

# read in the VHDL source code files and the xdc constraints file

# to allow for unconstrained ports
# we must set this property, this will
# generated only Warnings about unconstrained ports, but no errors
# and bitgen will generate the .bit file
# we intentionally did not specify any pin constraints in the
# .xdc file since we are not programming the board

set_property SEVERITY {Warning} [get_drc_checks UCIO-1]


read_vhdl  { ./Code/d_cache.vhd }
read_xdc  d_cache.xdc

# the -top refers to the top level VHDL entity name
# the -part specfies the target Xilinx FPGA

synth_design -top d_cache -part xc7a100tcsg324-1
opt_design
place_design
route_design

# generate the bitsteam file
write_bitstream -force d_cache.bit
```

Vivado synthesis log file: pc_reg.log

```
#-----------------------------------------------------------
# Vivado v2018.2 (64-bit)
# SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
# IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
# Start of session at: Thu Jun 24 23:11:02 2021
# Process ID: 38769
# Current directory: /nfs/home/u/u_mal/COEN316/LAB4
# Command line: vivado -log pc_reg.log -mode batch -source pc_reg.tcl
# Log file: /nfs/home/u/u_mal/COEN316/LAB4/pc_reg.log
# Journal file: /nfs/home/u/u_mal/COEN316/LAB4/vivado.jou
#-----------------------------------------------------------
source pc_reg.tcl
```

```
# set_property SEVERITY {Warning} [get_drc_checks UCIO-1]
# read_vhdl  { ./Code/pc_reg.vhd }
# read_xdc  pc_reg.xdc
# synth_design -top pc_reg -part xc7a100tcsg324-1
Command: synth_design -top pc_reg -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 38794
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory
 (MB): peak = 1468.582 ; gain = 86.727 ; free physical = 1661 ; free virtual = 15
3025
---------------------------------------------------------------------------------
INFO: [Synth 8-
638] synthesizing module 'pc_reg' [/nfs/home/u/u_mal/COEN316/LAB4/Code/pc_reg.vhd
:15]
INFO: [Synth 8-
256] done synthesizing module 'pc_reg' (1#1) [/nfs/home/u/u_mal/COEN316/LAB4/Code
/pc_reg.vhd:15]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory
 (MB): peak = 1513.223 ; gain = 131.367 ; free physical = 1674 ; free virtual = 1
53037
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:
05 . Memory (MB): peak = 1513.223 ; gain = 131.367 ; free physical = 1673 ; free
virtual = 153036
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
```

```
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05
 . Memory (MB): peak = 1513.223 ; gain = 131.367 ; free physical = 1673 ; free vi
rtual = 153036
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/pc_reg.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/pc_reg.xdc]
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01
. Memory (MB): peak = 1867.188 ; gain = 0.000 ; free physical = 1399 ; free virtu
al = 152762
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:14 ; elapsed = 00:00:45 .
Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1478 ; free virtu
al = 152841
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:14 ; elapsed
 = 00:00:45 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 147
8 ; free virtual = 152841
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:14 ; ela
psed = 00:00:45 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical =
 1480 ; free virtual = 152843
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:14 ; elapsed = 00:00:46
 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1478 ; free vi
rtual = 152842
```

```
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Registers :
                32 Bit    Registers := 1
                 5 Bit    Registers := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module pc_reg
Detailed RTL Component Info :
+---Registers :
                32 Bit    Registers := 1
                 5 Bit    Registers := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
INFO: [Synth 8-3886] merging instance 'q_reg[0]' (FDC) to 'out_pc_reg[0]'
INFO: [Synth 8-3886] merging instance 'q_reg[1]' (FDC) to 'out_pc_reg[1]'
INFO: [Synth 8-3886] merging instance 'q_reg[2]' (FDC) to 'out_pc_reg[2]'
```

```
INFO: [Synth 8-3886] merging instance 'q_reg[3]' (FDC) to 'out_pc_reg[3]'
INFO: [Synth 8-3886] merging instance 'q_reg[4]' (FDC) to 'out_pc_reg[4]'
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:14 ; elapse
d = 00:00:46 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 14
77 ; free virtual = 152841
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:21 ; elapsed = 0
0:00:59 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ;
free virtual = 152722
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:59 . Me
mory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; free virtual
 = 152722
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:21 ; elapsed = 00:00:59 . Mem
ory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; free virtual
= 152722
---------------------------------------------------------------------------------

Report RTL Partitions:
```

```
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
--------------------------------------------------------------------------------
Start IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Flattening Before IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Final Netlist Cleanup
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Final Netlist Cleanup
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00 . Memory (M
B): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; free virtual = 1527
22
--------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
--------------------------------------------------------------------------------
Start Renaming Generated Instances
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:22 ; elapsed = 00:0
1:00 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; fre
e virtual = 152722
--------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
```

```
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:22 ; elapsed = 00:01:0
0 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; free v
irtual = 152722
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Ports
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00
 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; free vi
rtual = 152722
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:22 ; elapsed = 00:01:
00 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; free
virtual = 152722
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00
. Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; free vir
tual = 152722
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
```

```
+------+-----+------+
|1     |BUFG |     1|
|2     |FDCE |    32|
|3     |IBUF |    34|
|4     |OBUF |    37|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |   104|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00
 . Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1357 ; free vi
rtual = 152722
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:13 ; elapsed = 00:00:23 .
Memory (MB): peak = 1867.188 ; gain = 131.367 ; free physical = 1410 ; free virtu
al = 152775
Synthesis Optimization Complete : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00 .
 Memory (MB): peak = 1867.188 ; gain = 485.332 ; free physical = 1420 ; free virt
ual = 152785
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 34 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/pc_reg.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/pc_reg.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
18 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:23 ; elapsed = 00:01:01 . Memory (MB): peak =
 1867.188 ; gain = 498.059 ; free physical = 1399 ; free virtual = 152764
# opt_design
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
```

```
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-
462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1875.195 ; ga
in = 8.008 ; free physical = 1396 ; free virtual = 152761

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 1a646b229

Time (s): cpu = 00:00:07 ; elapsed = 00:00:33 . Memory (MB): peak = 2218.367 ; ga
in = 343.172 ; free physical = 1062 ; free virtual = 152427

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 1a646b229

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2218.36
7 ; gain = 0.000 ; free physical = 1085 ; free virtual = 152450
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 1a646b229

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2218.36
7 ; gain = 0.000 ; free physical = 1085 ; free virtual = 152450
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: 1a646b229

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2218.36
7 ; gain = 0.000 ; free physical = 1085 ; free virtual = 152450
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
```

```
Phase 4 BUFG optimization | Checksum: 1a646b229

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2218.36
7 ; gain = 0.000 ; free physical = 1085 ; free virtual = 152450
INFO: [Opt 31-
662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 c
ells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 1a646b229

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2218.36
7 ; gain = 0.000 ; free physical = 1085 ; free virtual = 152450
INFO: [Opt 31-
389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 1a646b229

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2218.36
7 ; gain = 0.000 ; free physical = 1085 ; free virtual = 152450
INFO: [Opt 31-
389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2218.367 ; ga
in = 0.000 ; free physical = 1085 ; free virtual = 152450
Ending Logic Optimization Task | Checksum: 1a646b229

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2218.36
7 ; gain = 0.000 ; free physical = 1085 ; free virtual = 152450

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 1a646b229

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2218.367 ;
 gain = 0.000 ; free physical = 1085 ; free virtual = 152450

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 1a646b229

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2218.367 ; ga
in = 0.000 ; free physical = 1085 ; free virtual = 152450
```

```
INFO: [Common 17-83] Releasing license: Implementation
16 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:35 . Memory (MB): peak = 2
218.367 ; gain = 351.180 ; free physical = 1085 ; free virtual = 152450
# place_design
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-
611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2282.398 ; gain = 0.000 ; free physical = 1080 ; free virtual = 1524
45
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: fdb046eb

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2282.398 ;
 gain = 0.000 ; free physical = 1080 ; free virtual = 152445
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2282.398 ; gain = 0.000 ; free physical = 1080 ; free virtual = 1524
45

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 1b236db8
8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2306.410 ;
 gain = 24.012 ; free physical = 1075 ; free virtual = 152440
```

```
Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 2a0aa7b0e

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.72 . Memory (MB): peak = 2306.410 ;
 gain = 24.012 ; free physical = 1076 ; free virtual = 152441

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 2a0aa7b0e

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.72 . Memory (MB): peak = 2306.410 ;
 gain = 24.012 ; free physical = 1076 ; free virtual = 152441
Phase 1 Placer Initialization | Checksum: 2a0aa7b0e

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.72 . Memory (MB): peak = 2306.410 ;
 gain = 24.012 ; free physical = 1076 ; free virtual = 152441

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 2a0aa7b0e

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2306.410 ;
 gain = 24.012 ; free physical = 1074 ; free virtual = 152439
WARNING: [Place 46-
29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: 26405405f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.99 . Memory (MB): peak = 2434.469 ;
 gain = 152.070 ; free physical = 1046 ; free virtual = 152411

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 26405405f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1046 ; free virtual = 152411

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 203192c34

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1046 ; free virtual = 152411
```

```
Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 20af7b0de

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1046 ; free virtual = 152411

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 20af7b0de

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1046 ; free virtual = 152411

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 1900cbf06

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1042 ; free virtual = 152407

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 1900cbf06

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1042 ; free virtual = 152407

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 1900cbf06

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1042 ; free virtual = 152407
Phase 3 Detail Placement | Checksum: 1900cbf06

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1042 ; free virtual = 152407

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 1900cbf06

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1042 ; free virtual = 152407

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 1900cbf06
```

```
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1043 ; free virtual = 152408

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 1900cbf06

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1043 ; free virtual = 152408

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 1900cbf06

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1043 ; free virtual = 152408
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1900cbf06

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1043 ; free virtual = 152408
Ending Placer Task | Checksum: 10ee27c2a

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2434.469 ; ga
in = 152.070 ; free physical = 1059 ; free virtual = 152425
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
# route_design
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.


Starting Routing Task
INFO: [Route 35-
254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: 1132353f ConstDB: 0 ShapeSum: fdb046eb RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: dd2a28bc
```

```
Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2438.098 ; ga
in = 3.629 ; free physical = 917 ; free virtual = 152282
Post Restoration Checksum: NetGraph: 346eb00d NumContArr: a8bb78af Constraints: 0
 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-
64] No timing constraints were detected. The router will operate in resource-
optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: dd2a28bc

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2444.086 ; ga
in = 9.617 ; free physical = 885 ; free virtual = 152250

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: dd2a28bc

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2444.086 ; ga
in = 9.617 ; free physical = 885 ; free virtual = 152250
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: df515fec

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2454.352 ; ga
in = 19.883 ; free physical = 877 ; free virtual = 152242

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: 103bde23a

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2454.352 ; ga
in = 19.883 ; free physical = 875 ; free virtual = 152240

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: 15ab1db18

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2454.352 ; ga
in = 19.883 ; free physical = 875 ; free virtual = 152240
Phase 4 Rip-up And Reroute | Checksum: 15ab1db18

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2454.352 ; ga
in = 19.883 ; free physical = 875 ; free virtual = 152240
```

```
Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: 15ab1db18

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2454.352 ; ga
in = 19.883 ; free physical = 875 ; free virtual = 152240

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: 15ab1db18

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2454.352 ; ga
in = 19.883 ; free physical = 875 ; free virtual = 152240
Phase 6 Post Hold Fix | Checksum: 15ab1db18

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2454.352 ; ga
in = 19.883 ; free physical = 875 ; free virtual = 152240

Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization    = 0.082822 %
  Global Horizontal Routing Utilization  = 0.0122194 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets               = 0
  Number of Unrouted Nets             = 0
  Number of Partially Routed Nets     = 0
  Number of Node Overlaps             = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 46.8468%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 7.35294%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 16.1765%, No Congested Regions.

------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
```

```
Direction: South
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 15ab1db18

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2454.352 ; ga
in = 19.883 ; free physical = 875 ; free virtual = 152240

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: 15ab1db18

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.352 ; ga
in = 21.883 ; free physical = 874 ; free virtual = 152239

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 15ab1db18

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.352 ; ga
in = 21.883 ; free physical = 874 ; free virtual = 152239
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.352 ; ga
in = 21.883 ; free physical = 911 ; free virtual = 152276

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
8 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:28 ; elapsed = 00:00:24 . Memory (MB): peak =
 2456.352 ; gain = 21.883 ; free physical = 911 ; free virtual = 152276
# write_bitstream -force pc_reg.bit
Command: write_bitstream -force pc_reg.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
```

```
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-
2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/
data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-
1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CO
NFIG_VOLTAGE voltage property is set in the current_design.  Configuration bank v
oltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set
 to the correct configuration voltage, in order to determine the I/O voltage supp
ort for the pins in bank 0.  It is suggested to specify these either using the 'E
dit Device Properties' function in the GUI or directly in the XDC file using the
following syntax:

 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
WARNING: [DRC UCIO-
1] Unconstrained Logical Port: 71 out of 71 logical ports have no user assigned s
pecific location constraint (LOC). This may cause I/O contention or incompatibili
ty with the board power or connectivity affecting performance, signal integrity o
r in extreme cases cause damage to the device or the components to which it is co
nnected. To correct this violation, specify all pin locations. This design will f
ail to generate a bitstream unless all logical ports have a user specified site L
OC constraint defined.  To allow bitstream creation with unspecified pin location
s (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_c
hecks UCIO-
1].  NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl comman
d), add this command to a .tcl file and add that file as a pre-
hook for write_bitstream step for the implementation run.  Problem ports: d[31:0]
, out_pc[31:0], q[4:0], clk, and reset.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 2 Warnings
INFO: [Vivado 12-
3200] Please refer to the DRC report (report_drc) for more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
```

```
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./pc_reg.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:12 ; elapsed = 00:00:15 . Memory (MB): pea
k = 2802.172 ; gain = 345.820 ; free physical = 869 ; free virtual = 152237
INFO: [Common 17-206] Exiting Vivado at Thu Jun 24 23:13:32 2021...
```

Vivado synthesis log file: i_cache.log

```
#-----------------------------------------------------------
# Vivado v2018.2 (64-bit)
# SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
# IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
# Start of session at: Thu Jun 24 20:24:44 2021
# Process ID: 38178
# Current directory: /nfs/home/u/u_mal/COEN316/LAB4
# Command line: vivado -log i_cache.log -mode batch -source i_cache.tcl
# Log file: /nfs/home/u/u_mal/COEN316/LAB4/i_cache.log
# Journal file: /nfs/home/u/u_mal/COEN316/LAB4/vivado.jou
#-----------------------------------------------------------
source i_cache.tcl
# set_property SEVERITY {Warning} [get_drc_checks UCIO-1]
# read_vhdl  { ./Code/i_cache.vhd }
# read_xdc  i_cache.xdc
# synth_design -top i_cache -part xc7a100tcsg324-1
Command: synth_design -top i_cache -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 38196
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory
 (MB): peak = 1468.586 ; gain = 86.727 ; free physical = 1632 ; free virtual = 15
2981
---------------------------------------------------------------------------------
```

```
INFO: [Synth 8-
638] synthesizing module 'i_cache' [/nfs/home/u/u_mal/COEN316/LAB4/Code/i_cache.v
hd:12]
INFO: [Synth 8-
256] done synthesizing module 'i_cache' (1#1) [/nfs/home/u/u_mal/COEN316/LAB4/Cod
e/i_cache.vhd:12]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory
 (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 1645 ; free virtual = 1
52994
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:
05 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 1645 ; free
virtual = 152993
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05
 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 1645 ; free vi
rtual = 152993
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/i_cache.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/i_cache.xdc]
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
```

```
Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . M
emory (MB): peak = 1794.191 ; gain = 0.000 ; free physical = 1391 ; free virtual
= 152740
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:14 ; elapsed = 00:00:45 .
Memory (MB): peak = 1794.191 ; gain = 412.332 ; free physical = 1460 ; free virtu
al = 152808
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:14 ; elapsed
 = 00:00:45 . Memory (MB): peak = 1794.191 ; gain = 412.332 ; free physical = 146
0 ; free virtual = 152808
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:14 ; ela
psed = 00:00:46 . Memory (MB): peak = 1794.191 ; gain = 412.332 ; free physical =
 1459 ; free virtual = 152808
---------------------------------------------------------------------------------
INFO: [Synth 8-
5546] ROM "output_instruction" won't be mapped to RAM because it is too sparse
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:14 ; elapsed = 00:00:46
 . Memory (MB): peak = 1794.191 ; gain = 412.332 ; free physical = 1451 ; free vi
rtual = 152800
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Muxes :
     2 Input     32 Bit        Muxes := 1
---------------------------------------------------------------------------------
```

```
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module i_cache
Detailed RTL Component Info :
+---Muxes :
     2 Input     32 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
WARNING: [Synth 8-
3917] design i_cache has port output_instruction[30] driven by constant 0
WARNING: [Synth 8-
3917] design i_cache has port output_instruction[25] driven by constant 0
WARNING: [Synth 8-
3917] design i_cache has port output_instruction[24] driven by constant 0
WARNING: [Synth 8-
3917] design i_cache has port output_instruction[20] driven by constant 0
WARNING: [Synth 8-
3917] design i_cache has port output_instruction[19] driven by constant 0
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:14 ; elapse
d = 00:00:46 . Memory (MB): peak = 1833.090 ; gain = 451.230 ; free physical = 14
32 ; free virtual = 152782
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
```

```
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:21 ; elapsed = 0
0:01:00 . Memory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ;
free virtual = 152660
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Timing Optimization
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:01:00 . Me
mory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; free virtual
 = 152660
-------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
Start Technology Mapping
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:21 ; elapsed = 00:01:00 . Mem
ory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; free virtual
= 152660
-------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
Start IO Insertion
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Flattening Before IO Insertion
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
```

```
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00 . Memory (M
B): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; free virtual = 1526
60
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Renaming Generated Instances
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:22 ; elapsed = 00:0
1:00 . Memory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; fre
e virtual = 152660
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:22 ; elapsed = 00:01:0
0 . Memory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; free v
irtual = 152660
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Ports
---------------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00
 . Memory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; free vi
rtual = 152660
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:22 ; elapsed = 00:01:
00 . Memory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; free
virtual = 152660
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00
. Memory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; free vir
tual = 152660
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT4 |     2|
|2     |LUT5 |    15|
|3     |IBUF |     5|
|4     |OBUF |    32|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
```

```
|1     |top      |       |    54|
+------+---------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00
 . Memory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1310 ; free vi
rtual = 152660
--------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 5 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:13 ; elapsed = 00:00:23 .
Memory (MB): peak = 1860.098 ; gain = 197.273 ; free physical = 1365 ; free virtu
al = 152715
Synthesis Optimization Complete : Time (s): cpu = 00:00:22 ; elapsed = 00:01:00 .
 Memory (MB): peak = 1860.098 ; gain = 478.238 ; free physical = 1374 ; free virt
ual = 152725
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 5 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/i_cache.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/i_cache.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
14 Infos, 5 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:23 ; elapsed = 00:01:02 . Memory (MB): peak =
 1908.105 ; gain = 538.973 ; free physical = 1361 ; free virtual = 152712
# opt_design
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-
462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1972.141 ; ga
in = 64.035 ; free physical = 1358 ; free virtual = 152709
```

```
Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 13855cffa

Time (s): cpu = 00:00:07 ; elapsed = 00:00:33 . Memory (MB): peak = 2294.312 ; ga
in = 322.172 ; free physical = 1046 ; free virtual = 152396

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 13855cffa

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2294.31
2 ; gain = 0.000 ; free physical = 1047 ; free virtual = 152398
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 13855cffa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2294.31
2 ; gain = 0.000 ; free physical = 1047 ; free virtual = 152398
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: 13855cffa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2294.31
2 ; gain = 0.000 ; free physical = 1047 ; free virtual = 152398
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 13855cffa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2294.31
2 ; gain = 0.000 ; free physical = 1047 ; free virtual = 152398
INFO: [Opt 31-
662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 c
ells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 13855cffa
```

```
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2294.31
2 ; gain = 0.000 ; free physical = 1047 ; free virtual = 152398
INFO: [Opt 31-
389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 13855cffa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2294.31
2 ; gain = 0.000 ; free physical = 1047 ; free virtual = 152398
INFO: [Opt 31-
389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2294.312 ; ga
in = 0.000 ; free physical = 1047 ; free virtual = 152398
Ending Logic Optimization Task | Checksum: 13855cffa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2294.31
2 ; gain = 0.000 ; free physical = 1047 ; free virtual = 152398

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 13855cffa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2294.31
2 ; gain = 0.000 ; free physical = 1047 ; free virtual = 152398

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 13855cffa

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2294.312 ; ga
in = 0.000 ; free physical = 1047 ; free virtual = 152398
INFO: [Common 17-83] Releasing license: Implementation
16 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:36 . Memory (MB): peak = 2
294.312 ; gain = 386.207 ; free physical = 1047 ; free virtual = 152398
# place_design
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
```

```
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-
611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2358.344 ; gain = 0.000 ; free physical = 1038 ; free virtual = 1523
89
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: e367458f

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2358.34
4 ; gain = 0.000 ; free physical = 1038 ; free virtual = 152389
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2358.344 ; gain = 0.000 ; free physical = 1038 ; free virtual = 1523
89

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 1c581cca
5

Time (s): cpu = 00:00:00.72 ; elapsed = 00:00:00.55 . Memory (MB): peak = 2358.34
4 ; gain = 0.000 ; free physical = 1036 ; free virtual = 152386

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 20c76bc85

Time (s): cpu = 00:00:00.77 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2358.34
4 ; gain = 0.000 ; free physical = 1036 ; free virtual = 152386

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 20c76bc85
```

```
Time (s): cpu = 00:00:00.78 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2358.34
4 ; gain = 0.000 ; free physical = 1036 ; free virtual = 152386
Phase 1 Placer Initialization | Checksum: 20c76bc85

Time (s): cpu = 00:00:00.78 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2358.34
4 ; gain = 0.000 ; free physical = 1036 ; free virtual = 152386

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 20c76bc85

Time (s): cpu = 00:00:00.81 ; elapsed = 00:00:00.61 . Memory (MB): peak = 2358.34
4 ; gain = 0.000 ; free physical = 1035 ; free virtual = 152386
WARNING: [Place 46-
29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: 21e7637d4

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.89 . Memory (MB): peak = 2454.387 ;
 gain = 96.043 ; free physical = 1013 ; free virtual = 152364

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 21e7637d4

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.90 . Memory (MB): peak = 2454.387 ;
 gain = 96.043 ; free physical = 1013 ; free virtual = 152364

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 25462d911

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.92 . Memory (MB): peak = 2454.387 ;
 gain = 96.043 ; free physical = 1014 ; free virtual = 152364

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 1d1b154a9

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.93 . Memory (MB): peak = 2454.387 ;
 gain = 96.043 ; free physical = 1014 ; free virtual = 152364

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 1d1b154a9
```

```
Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.93 . Memory (MB): peak = 2454.387 ;
 gain = 96.043 ; free physical = 1014 ; free virtual = 152364

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361
Phase 3 Detail Placement | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361
```

```
Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 133e44c2e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1010 ; free virtual = 152361
Ending Placer Task | Checksum: 12034df9d

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.387 ; ga
in = 96.043 ; free physical = 1028 ; free virtual = 152378
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
# route_design
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.


Starting Routing Task
INFO: [Route 35-
254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: 3ccd9a0e ConstDB: 0 ShapeSum: e367458f RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: 1e3de342

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2465.016 ; ga
in = 10.629 ; free physical = 877 ; free virtual = 152228
Post Restoration Checksum: NetGraph: 6eaf44d NumContArr: 1752eef5 Constraints: 0
Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-
64] No timing constraints were detected. The router will operate in resource-
optimization mode.
```

```
Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 1e3de342

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2472.004 ; ga
in = 17.617 ; free physical = 845 ; free virtual = 152196

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 1e3de342

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2472.004 ; ga
in = 17.617 ; free physical = 845 ; free virtual = 152196
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: 83dd9da2

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2479.270 ; ga
in = 24.883 ; free physical = 842 ; free virtual = 152192

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: fe0b8574

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2479.270 ; ga
in = 24.883 ; free physical = 840 ; free virtual = 152191

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 2
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: ee487205

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2479.270 ; ga
in = 24.883 ; free physical = 840 ; free virtual = 152190
Phase 4 Rip-up And Reroute | Checksum: ee487205

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2479.270 ; ga
in = 24.883 ; free physical = 840 ; free virtual = 152190

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: ee487205

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2479.270 ; ga
in = 24.883 ; free physical = 840 ; free virtual = 152190

Phase 6 Post Hold Fix
```

```
Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: ee487205

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2479.270 ; ga
in = 24.883 ; free physical = 840 ; free virtual = 152190
Phase 6 Post Hold Fix | Checksum: ee487205

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2479.270 ; ga
in = 24.883 ; free physical = 840 ; free virtual = 152190

Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization    = 0.0106193 %
  Global Horizontal Routing Utilization  = 0.0039784 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets               = 0
  Number of Unrouted Nets             = 0
  Number of Partially Routed Nets     = 0
  Number of Node Overlaps             = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 3.6036%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 29.7297%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 11.7647%, No Congested Regions.

------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
```

```
Direction: West
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: ee487205

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.883 ; free physical = 840 ; free virtual = 152190

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: ee487205

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2483.270 ; ga
in = 28.883 ; free physical = 838 ; free virtual = 152188

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 12754a729

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2483.270 ; ga
in = 28.883 ; free physical = 838 ; free virtual = 152188
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2483.270 ; ga
in = 28.883 ; free physical = 872 ; free virtual = 152223

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
8 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:26 ; elapsed = 00:00:23 . Memory (MB): peak =
 2483.270 ; gain = 28.883 ; free physical = 872 ; free virtual = 152223
# write_bitstream -force i_cache.bit
Command: write_bitstream -force i_cache.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-
2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/
data/ip'.
```

```
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-
1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CO
NFIG_VOLTAGE voltage property is set in the current_design.  Configuration bank v
oltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set
 to the correct configuration voltage, in order to determine the I/O voltage supp
ort for the pins in bank 0.  It is suggested to specify these either using the 'E
dit Device Properties' function in the GUI or directly in the XDC file using the
following syntax:

 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
WARNING: [DRC UCIO-
1] Unconstrained Logical Port: 37 out of 37 logical ports have no user assigned s
pecific location constraint (LOC). This may cause I/O contention or incompatibili
ty with the board power or connectivity affecting performance, signal integrity o
r in extreme cases cause damage to the device or the components to which it is co
nnected. To correct this violation, specify all pin locations. This design will f
ail to generate a bitstream unless all logical ports have a user specified site L
OC constraint defined.  To allow bitstream creation with unspecified pin location
s (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_c
hecks UCIO-
1].  NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl comman
d), add this command to a .tcl file and add that file as a pre-
hook for write_bitstream step for the implementation run.  Problem ports: input_a
ddress[4:0], and output_instruction[31:0].
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 2 Warnings
INFO: [Vivado 12-
3200] Please refer to the DRC report (report_drc) for more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./i_cache.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
```

```
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:12 ; elapsed = 00:00:15 . Memory (MB): pea
k = 2829.090 ; gain = 345.820 ; free physical = 829 ; free virtual = 152183
INFO: [Common 17-206] Exiting Vivado at Thu Jun 24 20:27:15 2021...
```

Vivado synthesis log file: sign_extend.log

```
#-----------------------------------------------------------
# Vivado v2018.2 (64-bit)
# SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
# IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
# Start of session at: Thu Jun 24 17:54:09 2021
# Process ID: 9917
# Current directory: /nfs/home/u/u_mal/COEN316/LAB4
# Command line: vivado -log sign_extend.log -mode batch -source sign_extend.tcl
# Log file: /nfs/home/u/u_mal/COEN316/LAB4/sign_extend.log
# Journal file: /nfs/home/u/u_mal/COEN316/LAB4/vivado.jou
#-----------------------------------------------------------
source sign_extend.tcl
# set_property SEVERITY {Warning} [get_drc_checks UCIO-1]
# read_vhdl  { ./Code/sign_extend.vhd }
# read_xdc  sign_extend.xdc
# synth_design -top sign_extend -part xc7a100tcsg324-1
Command: synth_design -top sign_extend -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 9938
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory
 (MB): peak = 1468.586 ; gain = 86.727 ; free physical = 94327 ; free virtual = 1
54763
---------------------------------------------------------------------------------
INFO: [Synth 8-
638] synthesizing module 'sign_extend' [/nfs/home/u/u_mal/COEN316/LAB4/Code/sign_
extend.vhd:13]
INFO: [Synth 8-
226] default block is never used [/nfs/home/u/u_mal/COEN316/LAB4/Code/sign_extend
.vhd:18]
INFO: [Synth 8-
256] done synthesizing module 'sign_extend' (1#1) [/nfs/home/u/u_mal/COEN316/LAB4
/Code/sign_extend.vhd:13]
---------------------------------------------------------------------------------
```

```
Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory
 (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 94340 ; free virtual =
154776
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:
05 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 94340 ; free
 virtual = 154776
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05
 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 94340 ; free v
irtual = 154776
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/sign_extend.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/sign_extend.xdc]
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01
. Memory (MB): peak = 1795.191 ; gain = 0.000 ; free physical = 94088 ; free virt
ual = 154524
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:13 ; elapsed = 00:00:44 .
Memory (MB): peak = 1795.191 ; gain = 413.332 ; free physical = 94156 ; free virt
ual = 154592
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
```

```
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:13 ; elapsed
 = 00:00:44 . Memory (MB): peak = 1795.191 ; gain = 413.332 ; free physical = 941
56 ; free virtual = 154592
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:13 ; ela
psed = 00:00:44 . Memory (MB): peak = 1795.191 ; gain = 413.332 ; free physical =
 94157 ; free virtual = 154594
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:13 ; elapsed = 00:00:44
 . Memory (MB): peak = 1795.191 ; gain = 413.332 ; free physical = 94146 ; free v
irtual = 154584
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Muxes :
     4 Input     32 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module sign_extend
Detailed RTL Component Info :
+---Muxes :
     4 Input     32 Bit        Muxes := 1
---------------------------------------------------------------------------------
```

```
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:14 ; elapse
d = 00:00:44 . Memory (MB): peak = 1834.090 ; gain = 452.230 ; free physical = 94
129 ; free virtual = 154567
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:20 ; elapsed = 0
0:00:57 . Memory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ;
 free virtual = 154443
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:20 ; elapsed = 00:00:57 . Me
mory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; free virtua
l = 154443
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
```

```
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
Start Technology Mapping
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:20 ; elapsed = 00:00:57 . Mem
ory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; free virtual
 = 154443
-------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
Start IO Insertion
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Flattening Before IO Insertion
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Final Netlist Cleanup
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Final Netlist Cleanup
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:21 ; elapsed = 00:00:58 . Memory (M
B): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; free virtual = 154
443
-------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
-------------------------------------------------------------------------------
```

```
Start Renaming Generated Instances
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:21 ; elapsed = 00:0
0:58 . Memory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; fr
ee virtual = 154443
--------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
--------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:21 ; elapsed = 00:00:5
8 . Memory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; free
virtual = 154443
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Renaming Generated Ports
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:21 ; elapsed = 00:00:58
 . Memory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; free v
irtual = 154443
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Handling Custom Attributes
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:21 ; elapsed = 00:00:
58 . Memory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; free
 virtual = 154443
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Renaming Generated Nets
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:21 ; elapsed = 00:00:58
. Memory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; free vi
rtual = 154443
--------------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |    17|
|2     |LUT4 |    15|
|3     |IBUF |    18|
|4     |OBUF |    32|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    82|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed = 00:00:58
 . Memory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94005 ; free v
irtual = 154443
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:12 ; elapsed = 00:00:22 .
Memory (MB): peak = 1859.098 ; gain = 195.273 ; free physical = 94059 ; free virt
ual = 154497
Synthesis Optimization Complete : Time (s): cpu = 00:00:21 ; elapsed = 00:00:58 .
 Memory (MB): peak = 1859.098 ; gain = 477.238 ; free physical = 94069 ; free vir
tual = 154507
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 18 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/sign_extend.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/sign_extend.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
```

```
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
14 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:22 ; elapsed = 00:00:59 . Memory (MB): peak =
 1907.109 ; gain = 537.977 ; free physical = 94056 ; free virtual = 154494
# opt_design
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-
462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1971.141 ; ga
in = 64.031 ; free physical = 94052 ; free virtual = 154490

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: e3756f72

Time (s): cpu = 00:00:07 ; elapsed = 00:00:32 . Memory (MB): peak = 2302.312 ; ga
in = 331.172 ; free physical = 93742 ; free virtual = 154180

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: e3756f72

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2302.31
2 ; gain = 0.000 ; free physical = 93742 ; free virtual = 154180
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: e3756f72
```

```
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2302.31
2 ; gain = 0.000 ; free physical = 93742 ; free virtual = 154180
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: e3756f72

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2302.31
2 ; gain = 0.000 ; free physical = 93742 ; free virtual = 154180
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: e3756f72

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2302.31
2 ; gain = 0.000 ; free physical = 93742 ; free virtual = 154180
INFO: [Opt 31-
662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 c
ells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: e3756f72

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2302.31
2 ; gain = 0.000 ; free physical = 93742 ; free virtual = 154180
INFO: [Opt 31-
389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: e3756f72

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2302.31
2 ; gain = 0.000 ; free physical = 93742 ; free virtual = 154180
INFO: [Opt 31-
389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2302.312 ; ga
in = 0.000 ; free physical = 93742 ; free virtual = 154180
Ending Logic Optimization Task | Checksum: e3756f72

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2302.31
2 ; gain = 0.000 ; free physical = 93742 ; free virtual = 154180
```

```
Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: e3756f72

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2302.31
2 ; gain = 0.000 ; free physical = 93740 ; free virtual = 154178

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: e3756f72

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2302.312 ; ga
in = 0.000 ; free physical = 93740 ; free virtual = 154178
INFO: [Common 17-83] Releasing license: Implementation
16 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:34 . Memory (MB): peak = 2
302.312 ; gain = 395.203 ; free physical = 93740 ; free virtual = 154178
# place_design
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-
611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2366.344 ; gain = 0.000 ; free physical = 93724 ; free virtual = 154
162
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 125a9e6d
```

```
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2366.34
4 ; gain = 0.000 ; free physical = 93724 ; free virtual = 154162
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2366.344 ; gain = 0.000 ; free physical = 93724 ; free virtual = 154
162

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: ed49fd70

Time (s): cpu = 00:00:00.78 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2366.34
4 ; gain = 0.000 ; free physical = 93719 ; free virtual = 154157

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 13565f66a

Time (s): cpu = 00:00:00.82 ; elapsed = 00:00:00.59 . Memory (MB): peak = 2366.34
4 ; gain = 0.000 ; free physical = 93719 ; free virtual = 154157

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 13565f66a

Time (s): cpu = 00:00:00.82 ; elapsed = 00:00:00.59 . Memory (MB): peak = 2366.34
4 ; gain = 0.000 ; free physical = 93719 ; free virtual = 154157
Phase 1 Placer Initialization | Checksum: 13565f66a

Time (s): cpu = 00:00:00.82 ; elapsed = 00:00:00.60 . Memory (MB): peak = 2366.34
4 ; gain = 0.000 ; free physical = 93719 ; free virtual = 154157

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 13565f66a

Time (s): cpu = 00:00:00.85 ; elapsed = 00:00:00.62 . Memory (MB): peak = 2366.34
4 ; gain = 0.000 ; free physical = 93718 ; free virtual = 154156
WARNING: [Place 46-
29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: 1c6a3d8d5

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.87 . Memory (MB): peak = 2454.383 ;
 gain = 88.039 ; free physical = 93695 ; free virtual = 154134

Phase 3 Detail Placement
```

```
Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 1c6a3d8d5

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.88 . Memory (MB): peak = 2454.383 ;
 gain = 88.039 ; free physical = 93695 ; free virtual = 154134

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 199657ba6

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.90 . Memory (MB): peak = 2454.383 ;
 gain = 88.039 ; free physical = 93695 ; free virtual = 154134

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 1385fd5c0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.90 . Memory (MB): peak = 2454.383 ;
 gain = 88.039 ; free physical = 93695 ; free virtual = 154134

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 1385fd5c0

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.91 . Memory (MB): peak = 2454.383 ;
 gain = 88.039 ; free physical = 93695 ; free virtual = 154134

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93692 ; free virtual = 154130

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93692 ; free virtual = 154130

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93692 ; free virtual = 154130
Phase 3 Detail Placement | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93692 ; free virtual = 154130
```

```
Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93692 ; free virtual = 154130

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93693 ; free virtual = 154131

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93693 ; free virtual = 154131

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93693 ; free virtual = 154131
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 11e4075ad

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93693 ; free virtual = 154131
Ending Placer Task | Checksum: ed4d1137

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2454.383 ; ga
in = 88.039 ; free physical = 93709 ; free virtual = 154148
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
# route_design
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
```

```
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.


Starting Routing Task
INFO: [Route 35-
254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: daf272ca ConstDB: 0 ShapeSum: 125a9e6d RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: 16282c617

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.016 ; ga
in = 11.633 ; free physical = 93561 ; free virtual = 154000
Post Restoration Checksum: NetGraph: b0dcc4f0 NumContArr: b1a60127 Constraints: 0
 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-
64] No timing constraints were detected. The router will operate in resource-
optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 16282c617

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2473.004 ; ga
in = 18.621 ; free physical = 93530 ; free virtual = 153968

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 16282c617

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2473.004 ; ga
in = 18.621 ; free physical = 93530 ; free virtual = 153968
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: 18f52f7d9

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.887 ; free physical = 93527 ; free virtual = 153965

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: 140cf44fb

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.887 ; free physical = 93525 ; free virtual = 153963
```

```
Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 1
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: 83a13789

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.887 ; free physical = 93525 ; free virtual = 153963
Phase 4 Rip-up And Reroute | Checksum: 83a13789

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.887 ; free physical = 93525 ; free virtual = 153963

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: 83a13789

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.887 ; free physical = 93525 ; free virtual = 153963

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: 83a13789

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.887 ; free physical = 93525 ; free virtual = 153963
Phase 6 Post Hold Fix | Checksum: 83a13789

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.887 ; free physical = 93525 ; free virtual = 153963

Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization    = 0.0282456 %
  Global Horizontal Routing Utilization  = 0.00909349 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets                  = 0
  Number of Unrouted Nets                = 0
  Number of Partially Routed Nets        = 0
  Number of Node Overlaps                = 0
```

```
Congestion Report
North Dir 1x1 Area, Max Cong = 1.8018%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 43.2432%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 20.5882%, No Congested Regions.

------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
---------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 83a13789

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2480.270 ; ga
in = 25.887 ; free physical = 93524 ; free virtual = 153962

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: 83a13789

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2482.270 ; ga
in = 27.887 ; free physical = 93524 ; free virtual = 153962

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: f2eb3440

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2482.270 ; ga
in = 27.887 ; free physical = 93524 ; free virtual = 153962
INFO: [Route 35-16] Router Completed Successfully
```

```
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2482.270 ; ga
in = 27.887 ; free physical = 93556 ; free virtual = 153994

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
8 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:27 ; elapsed = 00:00:23 . Memory (MB): peak =
 2482.270 ; gain = 27.887 ; free physical = 93556 ; free virtual = 153994
# write_bitstream -force sign_extend.bit
Command: write_bitstream -force sign_extend.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-
2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/
data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-
1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CO
NFIG_VOLTAGE voltage property is set in the current_design.  Configuration bank v
oltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set
 to the correct configuration voltage, in order to determine the I/O voltage supp
ort for the pins in bank 0.  It is suggested to specify these either using the 'E
dit Device Properties' function in the GUI or directly in the XDC file using the
following syntax:

 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
WARNING: [DRC UCIO-
1] Unconstrained Logical Port: 50 out of 50 logical ports have no user assigned s
pecific location constraint (LOC). This may cause I/O contention or incompatibili
ty with the board power or connectivity affecting performance, signal integrity o
r in extreme cases cause damage to the device or the components to which it is co
nnected. To correct this violation, specify all pin locations. This design will f
ail to generate a bitstream unless all logical ports have a user specified site L
```

```
OC constraint defined.  To allow bitstream creation with unspecified pin location
s (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_c
hecks UCIO-
1].  NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl comman
d), add this command to a .tcl file and add that file as a pre-
hook for write_bitstream step for the implementation run.  Problem ports: func[1:
0], in_16bit[15:0], and out_32bit[31:0].
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 2 Warnings
INFO: [Vivado 12-
3200] Please refer to the DRC report (report_drc) for more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./sign_extend.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:11 ; elapsed = 00:00:15 . Memory (MB): pea
k = 2829.090 ; gain = 346.820 ; free physical = 93514 ; free virtual = 153956
INFO: [Common 17-206] Exiting Vivado at Thu Jun 24 17:56:34 2021...
```

Vivado synthesis log file: d_cache.log

```
#-----------------------------------------------------------
# Vivado v2018.2 (64-bit)
# SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
# IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
# Start of session at: Thu Jun 24 22:09:47 2021
# Process ID: 12434
# Current directory: /nfs/home/u/u_mal/COEN316/LAB4
# Command line: vivado -log d_cache.log -mode batch -source d_cache.tcl
# Log file: /nfs/home/u/u_mal/COEN316/LAB4/d_cache.log
# Journal file: /nfs/home/u/u_mal/COEN316/LAB4/vivado.jou
#-----------------------------------------------------------
source d_cache.tcl
# set_property SEVERITY {Warning} [get_drc_checks UCIO-1]
# read_vhdl  { ./Code/d_cache.vhd }
# read_xdc  d_cache.xdc
# synth_design -top d_cache -part xc7a100tcsg324-1
Command: synth_design -top d_cache -part xc7a100tcsg324-1
```

```
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 12467
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory
 (MB): peak = 1468.586 ; gain = 86.727 ; free physical = 1632 ; free virtual = 15
2995
---------------------------------------------------------------------------------
INFO: [Synth 8-
638] synthesizing module 'd_cache' [/nfs/home/u/u_mal/COEN316/LAB4/Code/d_cache.v
hd:16]
INFO: [Synth 8-
256] done synthesizing module 'd_cache' (1#1) [/nfs/home/u/u_mal/COEN316/LAB4/Cod
e/d_cache.vhd:16]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory
 (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 1641 ; free virtual = 1
53005
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:
05 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 1641 ; free
virtual = 153005
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05
 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 1641 ; free vi
rtual = 153005
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
```

```
Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/d_cache.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/d_cache.xdc]
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01
. Memory (MB): peak = 1882.191 ; gain = 0.000 ; free physical = 1344 ; free virtu
al = 152708
-----------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:14 ; elapsed = 00:01:06 .
Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1458 ; free virtu
al = 152822
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Start Loading Part and Timing Information
-----------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
-----------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:14 ; elapsed
 = 00:01:06 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 145
8 ; free virtual = 152822
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:14 ; ela
psed = 00:01:06 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical =
 1458 ; free virtual = 152822
-----------------------------------------------------------------------------
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[0]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[1]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[2]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[3]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[4]" won't be mapped to RAM because it is too sparse
```

```
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[5]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[6]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[7]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[8]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[9]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[10]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[11]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[12]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[13]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[14]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[15]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[16]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[17]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[18]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[19]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[20]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[21]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[22]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[23]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[24]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[25]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[26]" won't be mapped to RAM because it is too sparse
```

```
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[27]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[28]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[29]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[30]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-
5546] ROM "d_cache_data_reg[31]" won't be mapped to RAM because it is too sparse
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:14 ; elapsed = 00:01:06
 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1450 ; free vi
rtual = 152815
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Registers :
                32 Bit    Registers := 32
+---Muxes :
     2 Input      1 Bit        Muxes := 32
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module d_cache
Detailed RTL Component Info :
+---Registers :
                32 Bit    Registers := 32
+---Muxes :
     2 Input      1 Bit        Muxes := 32
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:15 ; elapse
d = 00:01:08 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 14
23 ; free virtual = 152789
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:22 ; elapsed = 0
0:01:21 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1300 ;
free virtual = 152666
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:22 ; elapsed = 00:01:21 . Me
mory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1300 ; free virtual
 = 152666
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
```

```
+-+--------------+------------+----------+
--------------------------------------------------------------------------------
Start Technology Mapping
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:22 ; elapsed = 00:01:21 . Mem
ory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1300 ; free virtual
= 152666
--------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
--------------------------------------------------------------------------------
Start IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Flattening Before IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Final Netlist Cleanup
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Final Netlist Cleanup
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:23 ; elapsed = 00:01:22 . Memory (M
B): peak = 1882.191 ; gain = 500.332 ; free physical = 1299 ; free virtual = 1526
65
--------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
--------------------------------------------------------------------------------
Start Renaming Generated Instances
--------------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:23 ; elapsed = 00:0
1:22 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1299 ; fre
e virtual = 152665
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:23 ; elapsed = 00:01:2
2 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1299 ; free v
irtual = 152665
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Ports
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:23 ; elapsed = 00:01:22
 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1299 ; free vi
rtual = 152665
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:23 ; elapsed = 00:01:
22 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1299 ; free
virtual = 152665
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:23 ; elapsed = 00:01:22
. Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1299 ; free vir
tual = 152665
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
```

```
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+------+------+
|      |Cell  |Count |
+------+------+------+
|1     |BUFG  |     1|
|2     |LUT6  |   320|
|3     |MUXF7 |   128|
|4     |FDCE  |  1024|
|5     |IBUF  |    40|
|6     |OBUF  |    32|
+------+------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |  1545|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:23 ; elapsed = 00:01:22
 . Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1299 ; free vi
rtual = 152665
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:14 ; elapsed = 00:00:24 .
Memory (MB): peak = 1882.191 ; gain = 131.367 ; free physical = 1354 ; free virtu
al = 152720
Synthesis Optimization Complete : Time (s): cpu = 00:00:23 ; elapsed = 00:01:22 .
 Memory (MB): peak = 1882.191 ; gain = 500.332 ; free physical = 1363 ; free virt
ual = 152729
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 168 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
WARNING: [Netlist 29-
101] Netlist 'd_cache' is not ideal for floorplanning, since the cellview 'd_cach
e' contains a large number of primitives.  Please consider enabling hierarchy in
synthesis if you want to do floorplanning.
```

```
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/d_cache.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/d_cache.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
45 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:25 ; elapsed = 00:01:24 . Memory (MB): peak =
 1885.816 ; gain = 516.684 ; free physical = 1349 ; free virtual = 152715
# opt_design
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-
462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1925.840 ; ga
in = 40.023 ; free physical = 1343 ; free virtual = 152709

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 5f802ef3

Time (s): cpu = 00:00:07 ; elapsed = 00:00:33 . Memory (MB): peak = 2259.012 ; ga
in = 333.172 ; free physical = 1042 ; free virtual = 152408

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 5f802ef3

Time (s): cpu = 00:00:00.13 ; elapsed = 00:00:00.08 . Memory (MB): peak = 2259.01
2 ; gain = 0.000 ; free physical = 1043 ; free virtual = 152409
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells
```

```
Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 5f802ef3

Time (s): cpu = 00:00:00.15 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2259.01
2 ; gain = 0.000 ; free physical = 1043 ; free virtual = 152409
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: 5f802ef3

Time (s): cpu = 00:00:00.17 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2259.01
2 ; gain = 0.000 ; free physical = 1043 ; free virtual = 152409
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 5f802ef3

Time (s): cpu = 00:00:00.20 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2259.01
2 ; gain = 0.000 ; free physical = 1043 ; free virtual = 152409
INFO: [Opt 31-
662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 c
ells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 5f802ef3

Time (s): cpu = 00:00:00.22 ; elapsed = 00:00:00.16 . Memory (MB): peak = 2259.01
2 ; gain = 0.000 ; free physical = 1043 ; free virtual = 152409
INFO: [Opt 31-
389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 5f802ef3

Time (s): cpu = 00:00:00.22 ; elapsed = 00:00:00.17 . Memory (MB): peak = 2259.01
2 ; gain = 0.000 ; free physical = 1043 ; free virtual = 152409
INFO: [Opt 31-
389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00 . Memory (MB): peak = 2259.012 ;
 gain = 0.000 ; free physical = 1043 ; free virtual = 152409
```

```
Ending Logic Optimization Task | Checksum: 5f802ef3

Time (s): cpu = 00:00:00.23 ; elapsed = 00:00:00.18 . Memory (MB): peak = 2259.01
2 ; gain = 0.000 ; free physical = 1043 ; free virtual = 152409

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 5f802ef3

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2259.01
2 ; gain = 0.000 ; free physical = 1043 ; free virtual = 152409

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 5f802ef3

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2259.012 ; ga
in = 0.000 ; free physical = 1043 ; free virtual = 152409
INFO: [Common 17-83] Releasing license: Implementation
16 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:09 ; elapsed = 00:00:36 . Memory (MB): peak = 2
259.012 ; gain = 373.195 ; free physical = 1043 ; free virtual = 152409
# place_design
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-
611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
```

```
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2323.043 ; gain = 0.000 ; free physical = 1035 ; free virtual = 1524
01
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 0253f2a9

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2323.04
3 ; gain = 0.000 ; free physical = 1035 ; free virtual = 152401
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2323.043 ; gain = 0.000 ; free physical = 1035 ; free virtual = 1524
01

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: a33d82f3

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.99 . Memory (MB): peak = 2347.055 ;
 gain = 24.012 ; free physical = 1028 ; free virtual = 152394

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: e8cd18ed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 2347.055 ; ga
in = 24.012 ; free physical = 1028 ; free virtual = 152394

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: e8cd18ed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 2347.055 ; ga
in = 24.012 ; free physical = 1028 ; free virtual = 152394
Phase 1 Placer Initialization | Checksum: e8cd18ed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 2347.055 ; ga
in = 24.012 ; free physical = 1028 ; free virtual = 152394

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: e8cd18ed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 2347.055 ; ga
in = 24.012 ; free physical = 1026 ; free virtual = 152393
WARNING: [Place 46-
29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: ddf5f6ce
```

```
Time (s): cpu = 00:00:07 ; elapsed = 00:00:02 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 1000 ; free virtual = 152366

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: ddf5f6ce

Time (s): cpu = 00:00:07 ; elapsed = 00:00:02 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 1000 ; free virtual = 152366

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 1319c8ced

Time (s): cpu = 00:00:07 ; elapsed = 00:00:02 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 140a96217

Time (s): cpu = 00:00:07 ; elapsed = 00:00:02 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 140a96217

Time (s): cpu = 00:00:07 ; elapsed = 00:00:02 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: c75b6074

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: c75b6074

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: c75b6074
```

```
Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365
Phase 3 Detail Placement | Checksum: c75b6074

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: c75b6074

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: c75b6074

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: c75b6074

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: c75b6074

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365
Phase 4 Post Placement Optimization and Clean-Up | Checksum: c75b6074

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 999 ; free virtual = 152365
Ending Placer Task | Checksum: c6f4b06b

Time (s): cpu = 00:00:08 ; elapsed = 00:00:03 . Memory (MB): peak = 2483.117 ; ga
in = 160.074 ; free physical = 1016 ; free virtual = 152382
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
place_design: Time (s): cpu = 00:00:10 ; elapsed = 00:00:06 . Memory (MB): peak =
 2483.117 ; gain = 224.105 ; free physical = 1016 ; free virtual = 152382
```

```
# route_design
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-
199] Please refer to the DRC report (report_drc) for more information.


Starting Routing Task
INFO: [Route 35-
254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: c4a0bdc2 ConstDB: 0 ShapeSum: 253f2a9 RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: 147245d9c

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2483.117 ; ga
in = 0.000 ; free physical = 866 ; free virtual = 152232
Post Restoration Checksum: NetGraph: f13e1d9e NumContArr: 55e63ffe Constraints: 0
 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-
64] No timing constraints were detected. The router will operate in resource-
optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 147245d9c

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2487.730 ; ga
in = 4.613 ; free physical = 835 ; free virtual = 152201

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 147245d9c

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2487.730 ; ga
in = 4.613 ; free physical = 835 ; free virtual = 152201
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: 19b479f4e
```

```
Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 823 ; free virtual = 152189

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: 12a4f47ce

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 827 ; free virtual = 152193

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 88
 Number of Nodes with overlaps = 1
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: 11fb62b1d

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 828 ; free virtual = 152195
Phase 4 Rip-up And Reroute | Checksum: 11fb62b1d

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 828 ; free virtual = 152195

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: 11fb62b1d

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 828 ; free virtual = 152195

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: 11fb62b1d

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 828 ; free virtual = 152195
Phase 6 Post Hold Fix | Checksum: 11fb62b1d

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 828 ; free virtual = 152195

Phase 7 Route finalize

Router Utilization Summary
```

```
  Global Vertical Routing Utilization    = 0.236019 %
  Global Horizontal Routing Utilization  = 0.23707 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets               = 0
  Number of Unrouted Nets             = 0
  Number of Partially Routed Nets     = 0
  Number of Node Overlaps             = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 34.2342%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 31.5315%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 36.7647%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 29.4118%, No Congested Regions.

------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 11fb62b1d

Time (s): cpu = 00:00:28 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 828 ; free virtual = 152195

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: 11fb62b1d
```

```
Time (s): cpu = 00:00:28 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 827 ; free virtual = 152193

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 11fb62b1d

Time (s): cpu = 00:00:28 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 827 ; free virtual = 152193
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:28 ; elapsed = 00:00:21 . Memory (MB): peak = 2504.996 ; ga
in = 21.879 ; free physical = 862 ; free virtual = 152228

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
8 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:30 ; elapsed = 00:00:35 . Memory (MB): peak =
 2504.996 ; gain = 21.879 ; free physical = 861 ; free virtual = 152228
# write_bitstream -force d_cache.bit
Command: write_bitstream -force d_cache.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-
349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-
2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/
data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-
1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CO
NFIG_VOLTAGE voltage property is set in the current_design.  Configuration bank v
oltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set
 to the correct configuration voltage, in order to determine the I/O voltage supp
ort for the pins in bank 0.  It is suggested to specify these either using the 'E
dit Device Properties' function in the GUI or directly in the XDC file using the
following syntax:

 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
```

```
 #where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
WARNING: [DRC UCIO-
1] Unconstrained Logical Port: 72 out of 72 logical ports have no user assigned s
pecific location constraint (LOC). This may cause I/O contention or incompatibili
ty with the board power or connectivity affecting performance, signal integrity o
r in extreme cases cause damage to the device or the components to which it is co
nnected. To correct this violation, specify all pin locations. This design will f
ail to generate a bitstream unless all logical ports have a user specified site L
OC constraint defined.  To allow bitstream creation with unspecified pin location
s (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_c
hecks UCIO-
1].  NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl comman
d), add this command to a .tcl file and add that file as a pre-
hook for write_bitstream step for the implementation run.  Problem ports: d_in[31
:0], d_out[31:0], data_address[4:0], clk, data_write, and reset.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 2 Warnings
INFO: [Vivado 12-
3200] Please refer to the DRC report (report_drc) for more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./d_cache.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:14 ; elapsed = 00:00:36 . Memory (MB): pea
k = 2844.816 ; gain = 339.820 ; free physical = 817 ; free virtual = 152187
INFO: [Common 17-206] Exiting Vivado at Thu Jun 24 22:13:12 2021...
```

PART: 2 Control Unit and Testing

Objective

This part of the lab requires the implementation of the control unit. The control units the opcode and function fields from the I-Cache and outputs a 14 bit control signal used for the various components in the CPU. The three muxes required to complete the CPU were also implemented in this part.

All the other components were mapped together using port maps and signals in the VHDL code. The control unit was designed as a VHDL process.

Opcode, function field, and controls signals for every instruction.

Inst.	op	func	reg_write	reg_dst	reg_in_src	alu_src	add_sub	data_write	logic_func	func	branch_type	pc_sel
lui	001111		1	0	1	1	0 (X)	0	00 (x)	00	00	00
add	000000	100000	1	1	1	0	0	0	00	10	00	00
sub	000000	100010	1	1	1	0	1	0	00	10	00	00
slt	000000	101010	1	1	1	0	0	0	00	01	00	00
addi	001000		1	0	1	1	0	0	00	10	00	00
slti	001010		1	0	1	1	0	0	00	01	00	00
and	000000	100100	1	1	1	0	1	0	00	11	00	00
or	000000	100101	1	1	1	0	0	0	01	11	00	00
xor	000000	100110	1	1	1	0	0	0	10	11	00	00
nor	000000	100111	1	1	1	0	0	0	11	11	00	00
andi	001100		1	0	1	1	0	0	00	11	00	00
ori	001101		1	0	1	1	0	0	01	11	00	00
xori	001110		1	0	1	1	0	0	10	11	00	00
lw	100011		1	0	0	1	0	0	10 (X)	10	00	00

sw	101011		0	0 (X)	0 (X)	1	0	1	00	10	00	00
j	000010		0 (X)	0	0	0	0	0	00	00	00	01
jr	000000	001000	0 (X)	0	0	0	0	0	00	00	00	10
bltz	000001		0	0	0	0	0	0	00	00	11	00
beq	000100		0	0	0	0	0	0	00	00	01	00
bne	000101		0	0	0	0	0	0	00	00	10	00

CPU ModelSim Result

```
#    Time: 0 ns  Iteration: 7  Instance: /cpu/arithmeticunit
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 7  Instance: /cpu/arithmeticunit
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 7  Instance: /cpu/arithmeticunit
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 7  Instance: /cpu/arithmeticunit
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 7  Instance: /cpu/dcache
# ** Warning: CONV_INTEGER: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, and it has been converted to 0.
#    Time: 0 ns  Iteration: 7  Instance: /cpu/dcache
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 8  Instance: /cpu/arithmeticunit
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 8  Instance: /cpu/arithmeticunit
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 8  Instance: /cpu/arithmeticunit
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 9  Instance: /cpu/arithmeticunit
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#    Time: 0 ns  Iteration: 9  Instance: /cpu/arithmeticunit
# 1 0 00000000 00000000 00000000 0 1
# 0 1 00000001 00000000 00000000 0 1
# 0 1 00000002 00000000 00000000 0 0
# 0 1 00000003 00000000 00000005 0 0
# 0 1 00000004 00000005 00000005 0 0
# 0 1 00000005 00000004 00000000 0 0
# 0 1 00000006 00000000 00000000 0 1
# 0 1 00000003 00000005 00000004 0 0
# 0 1 00000004 00000004 00000004 0 0
# 0 1 00000005 00000003 00000000 0 0
# 0 1 00000006 00000000 00000000 0 1
# 0 1 00000003 00000009 00000003 0 0
# 0 1 00000004 00000003 00000003 0 0
# 0 1 00000005 00000002 00000000 0 0
# 0 1 00000006 00000000 00000000 0 1
# 0 1 00000003 0000000C 00000002 0 0
# 0 1 00000004 00000002 00000002 0 0
# 0 1 00000005 00000001 00000000 0 0
# 0 1 00000006 00000000 00000000 0 1
# 0 1 00000003 0000000E 00000001 0 0
# 0 1 00000004 00000001 00000001 0 1
# 0 1 00000005 00000000 00000000 0 1
# 0 1 00000007 00000000 0000000F 0 1
# 0 1 00000008 00000000 00000000 0 1
# 0 1 00000009 0000000F 0000000F 0 0
# 0 1 0000000A 0000000A 0000000A 0 0
# 0 1 0000000B 0000000B 0000000B 0 0
# 0 1 0000000C 00000000 00000000 0 1
#
#
VSIM 2>
```

Clock Cycle	cpu_reset	cpu_clk	pc_out	rs_out	rt_out	cpu_overflow	cpu_zero
0	1	0	00000000	00000000	00000000	0	1
1	0	1	00000001	00000000	00000000	0	1
2	0	1	00000002	00000000	00000000	0	0
3	0	1	00000003	00000000	00000005	0	0
4	0	1	00000004	00000005	00000005	0	0
5	0	1	00000005	00000004	00000000	0	0
6	0	1	00000006	00000000	00000000	0	1
7	0	1	00000003	00000005	00000004	0	0
8	0	1	00000004	00000004	00000004	0	0
9	0	1	00000005	00000003	00000000	0	0
10	0	1	00000006	00000000	00000000	0	1
11	0	1	00000003	00000009	00000003	0	0
12	0	1	00000004	00000003	00000003	0	0
13	0	1	00000005	00000002	00000000	0	0
14	0	1	00000006	00000000	00000000	0	1
15	0	1	00000003	0000000C	00000002	0	0
16	0	1	00000004	00000002	00000002	0	0
17	0	1	00000005	00000001	00000000	0	0
18	0	1	00000006	00000000	00000000	0	1
19	0	1	00000003	0000000E	00000001	0	0
20	0	1	00000004	00000001	00000001	0	1
21	0	1	00000005	00000000	00000000	0	1
23	0	1	00000007	00000000	0000000F	0	1
24	0	1	00000008	00000000	00000000	0	1
25	0	1	00000009	0000000F	0000000F	0	0
26	0	1	0000000A	0000000A	0000000A	0	0
27	0	1	0000000B	0000000B	0000000B	0	0
28	0	1	0000000C	00000000	00000000	0	1

DO file: cpu.do

```
force cpu_reset 1
force cpu_clk 0
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero
force cpu_clk 1
force cpu_reset 0
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
```

```
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero
```

```
force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
```

```
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero


force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero

force cpu_clk 0
run 20
force cpu_clk 1
run 20
examine -radix X cpu_reset cpu_clk pc_out rs_out rt_out cpu_overflow cpu_zero
```

VHDL file: cpu.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity cpu  is
port(
    cpu_reset                   : in std_logic;
    cpu_clk                     : in std_logic;
    rs_out , rt_out             : out std_logic_vector(31 downto 0);
```

```
    -- output ports from register file

    pc_out                      : out std_logic_vector(31 downto 0); -- pc reg
    cpu_overflow, cpu_zero      : out std_logic
    );
end cpu;


architecture cpu_arch of cpu is

-- next-address component
component next_address
port(
    rt, rs          : in std_logic_vector(31 downto 0); -- two register inputs
    pc              : in std_logic_vector(31 downto 0);
    target_address  : in std_logic_vector(25 downto 0);
    branch_type     : in std_logic_vector(1 downto 0);
    pc_sel          : in std_logic_vector(1 downto 0);
    next_pc         : out std_logic_vector(31 downto 0)
    );
end component;

-- PC register component
component pc_reg
port(
        reset       : in std_logic;
        clk         : in std_logic;
        d           : in std_logic_vector(31 downto 0);
        out_pc      : out std_logic_vector(31 downto 0);
        q           : out std_logic_vector(4 downto 0)
    );
end component;

-- Instruction Cache component
component i_cache
port(
    input_address       : in std_logic_vector(4 downto 0);
    output_instruction  : out std_logic_vector(31 downto 0)
    );
end component;

-- Register File component
component regfile
port(
```

```
    din             : in std_logic_vector(31 downto 0);
    reset           : in std_logic;
    clk             : in std_logic;
    write           : in std_logic;
    read_a          : in std_logic_vector(4 downto 0);
    read_b          : in std_logic_vector(4 downto 0);
    write_address   : in std_logic_vector(4 downto 0);
    out_a           : out std_logic_vector(31 downto 0);
    out_b           : out std_logic_vector(31 downto 0)
);
end component;

-- Arithemetic & Logic Unit Component
component alu
port(
    x, y       : in std_logic_vector(31 downto 0); -- two input operands
    add_sub     : in std_logic; -- 0 = add, 1 = sub
    logic_func  : in std_logic_vector(1 downto 0 ) ; -
- 00 = AND , 01 = OR , 10 = XOR , 11 = NOR
    func        : in std_logic_vector(1 downto 0 ) ; -
- 00 = lui , 01 = setless , 10 = arith , 11 = logic
    output      : out std_logic_vector(31 downto 0) ;
    overflow    : out std_logic;
    zero        : out std_logic
    );
end component;

-- Data Cache component
component d_cache
port(
    reset           : in std_logic;
    clk             : in std_logic;
    data_write      : in std_logic;
    data_address    : in std_logic_vector(4 downto 0);
    d_in            : in std_logic_vector(31 downto 0);
    d_out           : out std_logic_vector(31 downto 0)
    );
end component;

-- Sign Extend component
component sign_extend
port(
        in_16bit    : in std_logic_vector(15 downto 0);
        func        : in std_logic_vector(1 downto 0);
        out_32bit   : out std_logic_vector(31 downto 0)
```

```
    );
end component;

signal next_pc_out, pc_out_32bit, i_cache_out, reg_in, reg_out_a, reg_out_b, alu_
out, alu_in, d_cache_out, sign_extend_out : std_logic_vector(31 downto 0);
signal reg_address_in : std_logic_vector(4 downto 0) := (others => '0');
signal pc_out_5bit : std_logic_vector(4 downto 0);
signal pc_select, branch_select, alu_function, alu_logic_function : std_logic_vec
tor(1 downto 0) := "00";
signal alu_addsub, d_cache_write, reg_write, reg_dst, alu_src, reg_in_src : std_l
ogic := '0';

signal opcode, fnction : std_logic_vector(5 downto 0) := (others => '0');
signal control         : std_logic_vector(13 downto 0);


begin
-- control unit process
    process(i_cache_out, cpu_clk, cpu_reset, opcode, fnction, control)
    begin
        opcode  <= i_cache_out(31 downto 26);
        fnction <= i_cache_out(5 downto 0);
        case opcode is
            when "000000" =>
                if    (fnction = "100000") then -- add
                    control <= "11100000100000";
                elsif (fnction = "100010") then -- sub
                    control <= "11101000100000";
                elsif (fnction = "101010") then -- slt
                    control <= "11100000010000";
                elsif (fnction = "100100") then -- and
                    control <= "11101000110000";
                elsif (fnction = "100101") then -- or
                    control <= "11100001110000";
                elsif (fnction = "100110") then -- xor
                    control <= "11100010110000";
                elsif (fnction = "100111") then -- nor
                    control <= "11100011110000";
                elsif (fnction = "001000") then -- jr
                    control <= "00000000000010";
                else end if;
            when "001111" => control <= "10110000000000"; -- lui
            when "001000" => control <= "10110000100000"; -- addi
            when "001010" => control <= "10110000010000"; -- slti
            when "001100" => control <= "10110000110000"; -- andi
```

```
            when "001101" => control <= "10110001110000"; -- ori
            when "001110" => control <= "10110010110000"; -- xori
            when "100011" => control <= "10010010100000"; -- lw
            when "101011" => control <= "00010100100000"; -- sw
            when "000010" => control <= "00000000000001"; -- j
            when "000001" => control <= "00000000001100"; -- bltz
            when "000100" => control <= "00000000000100"; -- beq
            when "000101" => control <= "00000000001000"; -- bne
            when others =>
        end case;

        reg_write           <= control(13);
        reg_dst             <= control(12);
        reg_in_src          <= control(11);
        alu_src             <= control(10);
        alu_addsub          <= control(9);
        d_cache_write       <= control(8);
        alu_logic_function  <= control(7 downto 6);
        alu_function        <= control(5 downto 4);
        branch_select       <= control(3 downto 2);
        pc_select           <= control(1 downto 0);

    end process;

-- component connection
NextAddress : next_address port map(
        rt => reg_out_b,
        rs => reg_out_a,
        pc => pc_out_32bit,
        target_address => i_cache_out(25 downto 0),
        branch_type => branch_select,
        pc_sel => pc_select,
        next_pc => next_pc_out);

ProgramCounter : pc_reg port map(
        reset => cpu_reset,
        clk => cpu_clk,
        d => next_pc_out,
        out_pc => pc_out_32bit,
        q => pc_out_5bit);

ICache : i_cache port map(
        input_address => pc_out_5bit,
        output_instruction => i_cache_out
        );
```

```
RegisterFile : regfile port map(
        din => reg_in,
        reset => cpu_reset,
        clk => cpu_clk,
        write => reg_write,
        read_a => i_cache_out(25 downto 21),
        read_b => i_cache_out(20 downto 16),
        write_address => reg_address_in,
        out_a => reg_out_a,
        out_b => reg_out_b);

ArithmeticUnit : alu port map(
        x => reg_out_a,
        y => alu_in,
        add_sub => alu_addsub,
        logic_func => alu_logic_function,
        func => alu_function,
        output => alu_out,
        overflow => cpu_overflow,
        zero => cpu_zero
        );

DCache : d_cache port map(
        reset => cpu_reset,
        clk => cpu_clk,
        data_write => d_cache_write,
        data_address => alu_out(4 downto 0),
        d_in => reg_out_b, d_out => d_cache_out
        );

SignExtend : sign_extend port map(
    in_16bit => i_cache_out(15 downto 0),
    func => alu_function,
    out_32bit => sign_extend_out
    );

reg_address_in <= i_cache_out(20 downto 16) when (reg_dst = '0')
                else i_cache_out(15 downto 11) when (reg_dst = '1');

alu_in <= reg_out_b when (alu_src = '0')
        else sign_extend_out when (alu_src = '1');

reg_in <= d_cache_out when (reg_in_src = '0')
        else alu_out when (reg_in_src = '1');
```

```
rs_out <= reg_out_a;
rt_out <= reg_out_b;
pc_out <= pc_out_32bit;


end cpu_arch;
```

XDC: cpu.xdc

```
# Vivado does not support old UCF syntax
# must use XDC syntax

# input ports are left unspecified
# of the Nexys board
# output ports is left unspecified
#
# we use the set_property IOSTANDARD LVCMOS33 to eliminate
# the error during bitgen about unspecified IOSTANDARD
# without bothering to specify any mapping of ports to pins
# since we will not be downloading to the FPGA board

# XDC file for cpu.vhd

set_property  IOSTANDARD LVCMOS33  [ get_ports { cpu_reset }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { cpu_clk }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { rs_out }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { rt_out }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { pc_out }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { cpu_overflow }  ] ;
set_property  IOSTANDARD LVCMOS33  [ get_ports { cpu_zero }  ] ;
```

TCL Vivado synthesis script: cpu.tcl

```
# TCL script for running vivado in batch mode to synthesize cpu.vhd

# To run the script first source the Vivado env file:
# source /CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/settings64_CMC_central_lic
ense.csh
#
#Then issue the following command from the Linux prompt:
# vivado -log cpu.log -mode batch -source cpu.tcl

# read in the VHDL source code files and the xdc constraints file

# to allow for unconstrained ports
# we must set this property, this will
```

```
# generated only Warnings about unconstrained ports, but no errors
# and bitgen will generate the .bit file
# we intentionally did not specify any pin constraints in the
# .xdc file since we are not programming the board


set_property SEVERITY {Warning} [get_drc_checks UCIO-1]


read_vhdl  { ./Code/cpu.vhd }
read_vhdl  { ./Code/alu.vhd }
read_vhdl  { ./Code/d_cache.vhd }
read_vhdl  { ./Code/i_cache.vhd }
read_vhdl  { ./Code/next_address.vhd }
read_vhdl  { ./Code/pc_reg.vhd }
read_vhdl  { ./Code/regfile.vhd }
read_vhdl  { ./Code/sign_extend.vhd }
read_xdc  cpu.xdc

# the -top refers to the top level VHDL entity name
# the -part specfies the target Xilinx FPGA

synth_design -top cpu -part xc7a100tcsg324-1
opt_design
place_design
route_design

# generate the bitsteam file
write_bitstream -force cpu.bit
```

Vivado synthesis log file: cpu.log

```
#-----------------------------------------------------------
# Vivado v2018.2 (64-bit)
# SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
# IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
# Start of session at: Sun Jun 27 16:20:05 2021
# Process ID: 30052
# Current directory: /nfs/home/u/u_mal/COEN316/LAB4
# Command line: vivado -log cpu.log -mode batch -source cpu.tcl
# Log file: /nfs/home/u/u_mal/COEN316/LAB4/cpu.log
# Journal file: /nfs/home/u/u_mal/COEN316/LAB4/vivado.jou
#-----------------------------------------------------------
source cpu.tcl
```

```
# set_property SEVERITY {Warning} [get_drc_checks UCIO-1]
# read_vhdl  { ./Code/cpu.vhd }
# read_vhdl  { ./Code/alu.vhd }
# read_vhdl  { ./Code/d_cache.vhd }
# read_vhdl  { ./Code/i_cache.vhd }
# read_vhdl  { ./Code/next_address.vhd }
# read_vhdl  { ./Code/pc_reg.vhd }
# read_vhdl  { ./Code/regfile.vhd }
# read_vhdl  { ./Code/sign_extend.vhd }
# read_xdc  cpu.xdc
# synth_design -top cpu -part xc7a100tcsg324-1
Command: synth_design -top cpu -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device
'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 30165
---------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory
(MB): peak = 1468.586 ; gain = 86.727 ; free physical = 93026 ; free virtual =
154793
---------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'cpu'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:19]
INFO: [Synth 8-3491] module 'next_address' declared at
'/nfs/home/u/u_mal/COEN316/LAB4/Code/next_address.vhd:5' bound to instance
'NextAddress' of component 'next_address'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:167]
INFO: [Synth 8-638] synthesizing module 'next_address'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/next_address.vhd:22]
INFO: [Synth 8-226] default block is never used
[/nfs/home/u/u_mal/COEN316/LAB4/Code/next_address.vhd:31]
INFO: [Synth 8-256] done synthesizing module 'next_address' (1#1)
[/nfs/home/u/u_mal/COEN316/LAB4/Code/next_address.vhd:22]
INFO: [Synth 8-3491] module 'pc_reg' declared at
'/nfs/home/u/u_mal/COEN316/LAB4/Code/pc_reg.vhd:5' bound to instance
'ProgramCounter' of component 'pc_reg'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:176]
INFO: [Synth 8-638] synthesizing module 'pc_reg'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/pc_reg.vhd:15]
INFO: [Synth 8-256] done synthesizing module 'pc_reg' (2#1)
[/nfs/home/u/u_mal/COEN316/LAB4/Code/pc_reg.vhd:15]
```

```
INFO: [Synth 8-3491] module 'i_cache' declared at
'/nfs/home/u/u_mal/COEN316/LAB4/Code/i_cache.vhd:5' bound to instance 'ICache' of
component 'i_cache' [/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:183]
INFO: [Synth 8-638] synthesizing module 'i_cache'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/i_cache.vhd:12]
INFO: [Synth 8-256] done synthesizing module 'i_cache' (3#1)
[/nfs/home/u/u_mal/COEN316/LAB4/Code/i_cache.vhd:12]
INFO: [Synth 8-3491] module 'regfile' declared at
'/nfs/home/u/u_mal/COEN316/LAB4/Code/regfile.vhd:8' bound to instance
'RegisterFile' of component 'regfile'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:188]
INFO: [Synth 8-638] synthesizing module 'regfile'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/regfile.vhd:22]
INFO: [Synth 8-256] done synthesizing module 'regfile' (4#1)
[/nfs/home/u/u_mal/COEN316/LAB4/Code/regfile.vhd:22]
INFO: [Synth 8-3491] module 'alu' declared at
'/nfs/home/u/u_mal/COEN316/LAB4/Code/alu.vhd:5' bound to instance
'ArithmeticUnit' of component 'alu'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:199]
INFO: [Synth 8-638] synthesizing module 'alu'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/alu.vhd:22]
INFO: [Synth 8-226] default block is never used
[/nfs/home/u/u_mal/COEN316/LAB4/Code/alu.vhd:35]
INFO: [Synth 8-226] default block is never used
[/nfs/home/u/u_mal/COEN316/LAB4/Code/alu.vhd:52]
INFO: [Synth 8-226] default block is never used
[/nfs/home/u/u_mal/COEN316/LAB4/Code/alu.vhd:72]
INFO: [Synth 8-256] done synthesizing module 'alu' (5#1)
[/nfs/home/u/u_mal/COEN316/LAB4/Code/alu.vhd:22]
INFO: [Synth 8-3491] module 'd_cache' declared at
'/nfs/home/u/u_mal/COEN316/LAB4/Code/d_cache.vhd:5' bound to instance 'DCache' of
component 'd_cache' [/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:210]
INFO: [Synth 8-638] synthesizing module 'd_cache'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/d_cache.vhd:16]
INFO: [Synth 8-256] done synthesizing module 'd_cache' (6#1)
[/nfs/home/u/u_mal/COEN316/LAB4/Code/d_cache.vhd:16]
INFO: [Synth 8-3491] module 'sign_extend' declared at
'/nfs/home/u/u_mal/COEN316/LAB4/Code/sign_extend.vhd:5' bound to instance
'SignExtend' of component 'sign_extend'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:218]
INFO: [Synth 8-638] synthesizing module 'sign_extend'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/sign_extend.vhd:13]
INFO: [Synth 8-226] default block is never used
[/nfs/home/u/u_mal/COEN316/LAB4/Code/sign_extend.vhd:18]
```

```
INFO: [Synth 8-256] done synthesizing module 'sign_extend' (7#1)
[/nfs/home/u/u_mal/COEN316/LAB4/Code/sign_extend.vhd:13]
INFO: [Synth 8-256] done synthesizing module 'cpu' (8#1)
[/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:19]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory
(MB): peak = 1513.227 ; gain = 131.367 ; free physical = 93034 ; free virtual =
154802
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed =
00:00:05 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 93036
; free virtual = 154804
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05
. Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 93036 ; free
virtual = 154804
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/cpu.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/cpu.xdc]
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 .
Memory (MB): peak = 1889.191 ; gain = 0.000 ; free physical = 92774 ; free
virtual = 154541
---------------------------------------------------------------------------------
```

```
Finished Constraint Validation : Time (s): cpu = 00:00:14 ; elapsed = 00:00:44 .
Memory (MB): peak = 1889.191 ; gain = 507.332 ; free physical = 92850 ; free
virtual = 154618
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Loading Part and Timing Information
-------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
-------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:14 ; elapsed
= 00:00:44 . Memory (MB): peak = 1889.191 ; gain = 507.332 ; free physical =
92850 ; free virtual = 154618
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:14 ;
elapsed = 00:00:44 . Memory (MB): peak = 1889.191 ; gain = 507.332 ; free
physical = 92849 ; free virtual = 154617
-------------------------------------------------------------------------------
INFO: [Synth 8-5546] ROM "output_instruction" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "registers_reg[0]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[1]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[2]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[3]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[4]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[5]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[6]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[7]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[8]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[9]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[10]" won't be mapped to RAM because it is
too sparse
```

```
INFO: [Synth 8-5546] ROM "registers_reg[11]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[12]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[13]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[14]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[15]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[16]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[17]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[18]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[19]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[20]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[21]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[22]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[23]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[24]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[25]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[26]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[27]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[28]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[29]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[30]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "registers_reg[31]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[0]" won't be mapped to RAM because it
is too sparse
```

```
INFO: [Synth 8-5546] ROM "d_cache_data_reg[1]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[2]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[3]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[4]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[5]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[6]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[7]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[8]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[9]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[10]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[11]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[12]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[13]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[14]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[15]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[16]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[17]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[18]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[19]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[20]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[21]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[22]" won't be mapped to RAM because it
is too sparse
```

```
INFO: [Synth 8-5546] ROM "d_cache_data_reg[23]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[24]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[25]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[26]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[27]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[28]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[29]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[30]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_data_reg[31]" won't be mapped to RAM because it
is too sparse
WARNING: [Synth 8-327] inferring latch for variable 'next_pc_reg'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/next_address.vhd:33]
WARNING: [Synth 8-327] inferring latch for variable 'control_reg'
[/nfs/home/u/u_mal/COEN316/LAB4/Code/cpu.vhd:122]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:14 ; elapsed = 00:00:45
. Memory (MB): peak = 1889.191 ; gain = 507.332 ; free physical = 92841 ; free
virtual = 154609
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
         2 Input     32 Bit       Adders := 3
         3 Input     32 Bit       Adders := 1
+---XORs :
         2 Input     32 Bit         XORs := 1
+---Registers :
                     32 Bit    Registers := 65
                      5 Bit    Registers := 1
```

```
+---Muxes :
         2 Input     32 Bit        Muxes := 7
         4 Input     32 Bit        Muxes := 5
         8 Input     14 Bit        Muxes := 1
        14 Input     14 Bit        Muxes := 1
         2 Input      5 Bit        Muxes := 1
         4 Input      1 Bit        Muxes := 1
         2 Input      1 Bit        Muxes := 72
        14 Input      1 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module cpu
Detailed RTL Component Info :
+---Muxes :
         2 Input     32 Bit        Muxes := 2
         8 Input     14 Bit        Muxes := 1
        14 Input     14 Bit        Muxes := 1
         2 Input      5 Bit        Muxes := 1
         2 Input      1 Bit        Muxes := 7
        14 Input      1 Bit        Muxes := 1
Module next_address
Detailed RTL Component Info :
+---Adders :
         2 Input     32 Bit       Adders := 2
+---Muxes :
         2 Input     32 Bit        Muxes := 3
         4 Input     32 Bit        Muxes := 2
         4 Input      1 Bit        Muxes := 1
Module pc_reg
Detailed RTL Component Info :
+---Registers :
                     32 Bit    Registers := 1
                      5 Bit    Registers := 1
Module i_cache
Detailed RTL Component Info :
+---Muxes :
         2 Input     32 Bit        Muxes := 1
Module regfile
Detailed RTL Component Info :
+---Registers :
```

```
                    32 Bit    Registers := 32
+---Muxes :
         2 Input      1 Bit        Muxes := 32
Module alu
Detailed RTL Component Info :
+---Adders :
         3 Input     32 Bit       Adders := 1
         2 Input     32 Bit       Adders := 1
+---XORs :
         2 Input     32 Bit         XORs := 1
+---Muxes :
         4 Input     32 Bit        Muxes := 2
         2 Input     32 Bit        Muxes := 1
         2 Input      1 Bit        Muxes := 1
Module d_cache
Detailed RTL Component Info :
+---Registers :
                    32 Bit    Registers := 32
+---Muxes :
         2 Input      1 Bit        Muxes := 32
Module sign_extend
Detailed RTL Component Info :
+---Muxes :
         4 Input     32 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
INFO: [Synth 8-3886] merging instance 'ProgramCounter/out_pc_reg[0]' (FDC) to
'ProgramCounter/q_reg[0]'
INFO: [Synth 8-3886] merging instance 'ProgramCounter/out_pc_reg[1]' (FDC) to
'ProgramCounter/q_reg[1]'
```

```
INFO: [Synth 8-3886] merging instance 'ProgramCounter/out_pc_reg[2]' (FDC) to
'ProgramCounter/q_reg[2]'
INFO: [Synth 8-3886] merging instance 'ProgramCounter/out_pc_reg[3]' (FDC) to
'ProgramCounter/q_reg[3]'
INFO: [Synth 8-3886] merging instance 'ProgramCounter/out_pc_reg[4]' (FDC) to
'ProgramCounter/q_reg[4]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][0]' (FDCE)
to 'RegisterFile/registers_reg[13][0]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][0]' (FDCE)
to 'RegisterFile/registers_reg[11][0]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][0] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][1]' (FDCE)
to 'RegisterFile/registers_reg[13][1]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][1]' (FDCE)
to 'RegisterFile/registers_reg[11][1]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][1] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][2]' (FDCE)
to 'RegisterFile/registers_reg[13][2]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][2]' (FDCE)
to 'RegisterFile/registers_reg[11][2]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][2] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][3]' (FDCE)
to 'RegisterFile/registers_reg[13][3]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][3]' (FDCE)
to 'RegisterFile/registers_reg[11][3]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][3] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][4]' (FDCE)
to 'RegisterFile/registers_reg[13][4]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][4]' (FDCE)
to 'RegisterFile/registers_reg[11][4]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][4] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][5]' (FDCE)
to 'RegisterFile/registers_reg[13][5]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][5]' (FDCE)
to 'RegisterFile/registers_reg[11][5]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][5] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][6]' (FDCE)
to 'RegisterFile/registers_reg[13][6]'
```

```
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][6]' (FDCE)
to 'RegisterFile/registers_reg[11][6]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][6] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][7]' (FDCE)
to 'RegisterFile/registers_reg[13][7]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][7]' (FDCE)
to 'RegisterFile/registers_reg[11][7]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][7] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][8]' (FDCE)
to 'RegisterFile/registers_reg[13][8]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][8]' (FDCE)
to 'RegisterFile/registers_reg[11][8]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][8] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][9]' (FDCE)
to 'RegisterFile/registers_reg[13][9]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][9]' (FDCE)
to 'RegisterFile/registers_reg[11][9]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][9] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][10]' (FDCE)
to 'RegisterFile/registers_reg[13][10]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][10]' (FDCE)
to 'RegisterFile/registers_reg[11][10]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][10] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][11]' (FDCE)
to 'RegisterFile/registers_reg[13][11]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][11]' (FDCE)
to 'RegisterFile/registers_reg[11][11]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][11] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][12]' (FDCE)
to 'RegisterFile/registers_reg[13][12]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][12]' (FDCE)
to 'RegisterFile/registers_reg[11][12]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][12] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][13]' (FDCE)
to 'RegisterFile/registers_reg[13][13]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][13]' (FDCE)
to 'RegisterFile/registers_reg[11][13]'
```

```
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][13] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][14]' (FDCE)
to 'RegisterFile/registers_reg[13][14]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][14]' (FDCE)
to 'RegisterFile/registers_reg[11][14]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][14] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][15]' (FDCE)
to 'RegisterFile/registers_reg[13][15]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][15]' (FDCE)
to 'RegisterFile/registers_reg[11][15]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][15] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][16]' (FDCE)
to 'RegisterFile/registers_reg[13][16]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][16]' (FDCE)
to 'RegisterFile/registers_reg[11][16]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][16] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][17]' (FDCE)
to 'RegisterFile/registers_reg[13][17]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][17]' (FDCE)
to 'RegisterFile/registers_reg[11][17]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][17] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][18]' (FDCE)
to 'RegisterFile/registers_reg[13][18]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][18]' (FDCE)
to 'RegisterFile/registers_reg[11][18]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][18] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][19]' (FDCE)
to 'RegisterFile/registers_reg[13][19]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][19]' (FDCE)
to 'RegisterFile/registers_reg[11][19]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][19] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][20]' (FDCE)
to 'RegisterFile/registers_reg[13][20]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][20]' (FDCE)
to 'RegisterFile/registers_reg[11][20]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][20] )
```

```
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][21]' (FDCE)
to 'RegisterFile/registers_reg[13][21]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][21]' (FDCE)
to 'RegisterFile/registers_reg[11][21]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][21] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][22]' (FDCE)
to 'RegisterFile/registers_reg[13][22]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][22]' (FDCE)
to 'RegisterFile/registers_reg[11][22]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][22] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][23]' (FDCE)
to 'RegisterFile/registers_reg[13][23]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][23]' (FDCE)
to 'RegisterFile/registers_reg[11][23]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][23] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][24]' (FDCE)
to 'RegisterFile/registers_reg[13][24]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][24]' (FDCE)
to 'RegisterFile/registers_reg[11][24]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][24] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][25]' (FDCE)
to 'RegisterFile/registers_reg[13][25]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][25]' (FDCE)
to 'RegisterFile/registers_reg[11][25]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][25] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][26]' (FDCE)
to 'RegisterFile/registers_reg[13][26]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][26]' (FDCE)
to 'RegisterFile/registers_reg[11][26]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][26] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][27]' (FDCE)
to 'RegisterFile/registers_reg[13][27]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][27]' (FDCE)
to 'RegisterFile/registers_reg[11][27]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][27] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][28]' (FDCE)
to 'RegisterFile/registers_reg[13][28]'
```

```
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][28]' (FDCE)
to 'RegisterFile/registers_reg[11][28]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][28] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][29]' (FDCE)
to 'RegisterFile/registers_reg[13][29]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][29]' (FDCE)
to 'RegisterFile/registers_reg[11][29]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][29] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][30]' (FDCE)
to 'RegisterFile/registers_reg[13][30]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][30]' (FDCE)
to 'RegisterFile/registers_reg[11][30]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][30] )
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[14][31]' (FDCE)
to 'RegisterFile/registers_reg[13][31]'
INFO: [Synth 8-3886] merging instance 'RegisterFile/registers_reg[13][31]' (FDCE)
to 'RegisterFile/registers_reg[11][31]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\RegisterFile/registers_reg[11][31] )
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][31]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][30]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][29]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][28]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][27]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][26]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][25]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][24]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][23]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][22]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][21]) is
unused and will be removed from module cpu.
```

```
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][20]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][19]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][18]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][17]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][16]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][15]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][14]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][13]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][12]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][11]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][10]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][9]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][8]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][7]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][6]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][5]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][4]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][3]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][2]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][1]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[8][0]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][31]) is
unused and will be removed from module cpu.
```

```
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][30]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][29]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][28]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][27]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][26]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][25]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][24]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][23]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][22]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][21]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][20]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][19]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][18]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][17]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][16]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][15]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][14]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][13]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][12]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][11]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][10]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][9]) is
unused and will be removed from module cpu.
```

```
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][8]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][7]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][6]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][5]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][4]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][3]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][2]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][1]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[9][0]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][31])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][30])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][29])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][28])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][27])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][26])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][25])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][24])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][23])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][22])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][21])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][20])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][19])
is unused and will be removed from module cpu.
```

```
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][18])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][17])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][16])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][15])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][14])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][13])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][12])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][11])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][10])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][9]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][8]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][7]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][6]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][5]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][4]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][3]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][2]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][1]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[10][0]) is
unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[12][31])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[12][30])
is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[12][29])
is unused and will be removed from module cpu.
```

```
WARNING: [Synth 8-3332] Sequential element (RegisterFile/registers_reg[12][28])
is unused and will be removed from module cpu.
INFO: [Common 17-14] Message 'Synth 8-3332' appears 100 times and further
instances of the messages will be disabled. Use the Tcl command set_msg_config to
change the current settings.
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:27 ;
elapsed = 00:00:58 . Memory (MB): peak = 1889.191 ; gain = 507.332 ; free
physical = 92799 ; free virtual = 154570
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:33 ; elapsed =
00:01:11 . Memory (MB): peak = 1889.191 ; gain = 507.332 ; free physical = 92685
; free virtual = 154456
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:35 ; elapsed = 00:01:12 .
Memory (MB): peak = 1889.191 ; gain = 507.332 ; free physical = 92684 ; free
virtual = 154455
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
INFO: [Synth 8-3886] merging instance 'control_reg[3]' (LD) to 'control_reg[9]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\control_reg[9] )
---------------------------------------------------------------------------------
```

```
Finished Technology Mapping : Time (s): cpu = 00:00:36 ; elapsed = 00:01:13 .
Memory (MB): peak = 1929.004 ; gain = 547.145 ; free physical = 92681 ; free
virtual = 154452
--------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
--------------------------------------------------------------------------------
Start IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Flattening Before IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Final Netlist Cleanup
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Final Netlist Cleanup
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:36 ; elapsed = 00:01:14 . Memory
(MB): peak = 1929.008 ; gain = 547.148 ; free physical = 92683 ; free virtual =
154454
--------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
--------------------------------------------------------------------------------
Start Renaming Generated Instances
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:36 ; elapsed =
00:01:14 . Memory (MB): peak = 1929.008 ; gain = 547.148 ; free physical = 92683
; free virtual = 154454
--------------------------------------------------------------------------------
```

```
Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:36 ; elapsed =
00:01:14 . Memory (MB): peak = 1929.008 ; gain = 547.148 ; free physical = 92683
; free virtual = 154454
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Renaming Generated Ports
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:36 ; elapsed = 00:01:14
. Memory (MB): peak = 1929.008 ; gain = 547.148 ; free physical = 92683 ; free
virtual = 154454
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Handling Custom Attributes
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:36 ; elapsed =
00:01:14 . Memory (MB): peak = 1929.008 ; gain = 547.148 ; free physical = 92683
; free virtual = 154454
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Renaming Generated Nets
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:36 ; elapsed = 00:01:14
. Memory (MB): peak = 1929.008 ; gain = 547.148 ; free physical = 92683 ; free
virtual = 154454
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
```

```
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     2|
|2     |CARRY4 |    35|
|3     |LUT1   |     1|
|4     |LUT2   |    29|
|5     |LUT3   |    75|
|6     |LUT4   |    54|
|7     |LUT5   |   141|
|8     |LUT6   |   508|
|9     |MUXF7  |   193|
|10    |MUXF8  |    62|
|11    |FDCE   |  1312|
|12    |LD     |    44|
|13    |IBUF   |     2|
|14    |OBUF   |    98|
+------+-------+------+

Report Instance Areas:
+------+-----------------+-------------+------+
|      |Instance         |Module       |Cells |
+------+-----------------+-------------+------+
|1     |top              |             |  2556|
|2     |  ArithmeticUnit |alu          |   146|
|3     |  DCache         |d_cache      |  1474|
|4     |  NextAddress    |next_address |    93|
|5     |  ProgramCounter |pc_reg       |   127|
|6     |  RegisterFile   |regfile      |   601|
+------+-----------------+-------------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:36 ; elapsed = 00:01:14
. Memory (MB): peak = 1929.008 ; gain = 547.148 ; free physical = 92683 ; free
virtual = 154454
--------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 707 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:28 ; elapsed = 00:00:38 .
Memory (MB): peak = 1929.008 ; gain = 171.184 ; free physical = 92738 ; free
virtual = 154509
```

```
Synthesis Optimization Complete : Time (s): cpu = 00:00:36 ; elapsed = 00:01:14 .
Memory (MB): peak = 1929.012 ; gain = 547.148 ; free physical = 92748 ; free
virtual = 154519
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 336 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/cpu.xdc]
Finished Parsing XDC File [/nfs/home/u/u_mal/COEN316/LAB4/cpu.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 44 instances were transformed.
  LD => LDCE: 44 instances

INFO: [Common 17-83] Releasing license: Synthesis
208 Infos, 102 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:38 ; elapsed = 00:01:16 . Memory (MB): peak =
1961.023 ; gain = 591.891 ; free physical = 92735 ; free virtual = 154506
# opt_design
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more
information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 2025.055 ;
gain = 64.031 ; free physical = 92732 ; free virtual = 154504

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: e39e1d8f

Time (s): cpu = 00:00:07 ; elapsed = 00:00:32 . Memory (MB): peak = 2322.211 ;
gain = 297.156 ; free physical = 92435 ; free virtual = 154199

Starting Logic Optimization Task

Phase 1 Retarget
```

```
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: e39e1d8f

Time (s): cpu = 00:00:00.19 ; elapsed = 00:00:00.11 . Memory (MB): peak =
2322.211 ; gain = 0.000 ; free physical = 92437 ; free virtual = 154201
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: e39e1d8f

Time (s): cpu = 00:00:00.22 ; elapsed = 00:00:00.14 . Memory (MB): peak =
2322.211 ; gain = 0.000 ; free physical = 92437 ; free virtual = 154201
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: 110562511

Time (s): cpu = 00:00:00.29 ; elapsed = 00:00:00.21 . Memory (MB): peak =
2322.211 ; gain = 0.000 ; free physical = 92437 ; free virtual = 154201
INFO: [Opt 31-389] Phase Sweep created 28 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 110562511

Time (s): cpu = 00:00:00.33 ; elapsed = 00:00:00.26 . Memory (MB): peak =
2322.211 ; gain = 0.000 ; free physical = 92437 ; free virtual = 154201
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs
and removed 0 cells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 152e55730

Time (s): cpu = 00:00:00.38 ; elapsed = 00:00:00.31 . Memory (MB): peak =
2322.211 ; gain = 0.000 ; free physical = 92437 ; free virtual = 154201
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed
0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 1313e886b

Time (s): cpu = 00:00:00.39 ; elapsed = 00:00:00.32 . Memory (MB): peak =
2322.211 ; gain = 0.000 ; free physical = 92437 ; free virtual = 154201
```

```
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0
cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2322.211 ;
gain = 0.000 ; free physical = 92437 ; free virtual = 154201
Ending Logic Optimization Task | Checksum: 1313e886b

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.33 . Memory (MB): peak =
2322.211 ; gain = 0.000 ; free physical = 92437 ; free virtual = 154201

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 1313e886b

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak =
2322.211 ; gain = 0.000 ; free physical = 92437 ; free virtual = 154201

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 1313e886b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2322.211 ;
gain = 0.000 ; free physical = 92437 ; free virtual = 154201
INFO: [Common 17-83] Releasing license: Implementation
16 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:09 ; elapsed = 00:00:35 . Memory (MB): peak =
2322.211 ; gain = 361.188 ; free physical = 92437 ; free virtual = 154201
# place_design
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.

Starting Placer Task
```

```
INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8
CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00 .
Memory (MB): peak = 2386.242 ; gain = 0.000 ; free physical = 92421 ; free
virtual = 154185
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: aaa4a45b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak =
2386.242 ; gain = 0.000 ; free physical = 92421 ; free virtual = 154185
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2386.242 ; gain = 0.000 ; free physical = 92421 ; free virtual =
154185

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum:
16ab517a2

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 2386.242 ;
gain = 0.000 ; free physical = 92417 ; free virtual = 154181

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 1a3ca2689

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2386.242 ;
gain = 0.000 ; free physical = 92417 ; free virtual = 154181

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 1a3ca2689

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2386.242 ;
gain = 0.000 ; free physical = 92417 ; free virtual = 154181
Phase 1 Placer Initialization | Checksum: 1a3ca2689

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2386.242 ;
gain = 0.000 ; free physical = 92417 ; free virtual = 154181

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 1a3ca2689
```

```
Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2386.242 ;
gain = 0.000 ; free physical = 92415 ; free virtual = 154179
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical
synthesis in placer
Phase 2 Global Placement | Checksum: 1d98d5e82

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92382 ; free virtual = 154146

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 1d98d5e82

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92382 ; free virtual = 154146

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 286b4aa50

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92382 ; free virtual = 154146

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 1abe12878

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92382 ; free virtual = 154146

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 1abe12878

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92382 ; free virtual = 154146

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 1be0e1b23

Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92381 ; free virtual = 154145

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 1be0e1b23
```

```
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92381 ; free virtual = 154145

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 1be0e1b23

Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92381 ; free virtual = 154145
Phase 3 Detail Placement | Checksum: 1be0e1b23

Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92382 ; free virtual = 154146

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 1be0e1b23

Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92382 ; free virtual = 154146

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 1be0e1b23

Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92383 ; free virtual = 154147

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 1be0e1b23

Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92383 ; free virtual = 154147

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 1be0e1b23

Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92383 ; free virtual = 154147
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1be0e1b23

Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92383 ; free virtual = 154147
Ending Placer Task | Checksum: 18300a5bd
```

```
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2482.285 ;
gain = 96.043 ; free physical = 92399 ; free virtual = 154163
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
place_design: Time (s): cpu = 00:00:12 ; elapsed = 00:00:07 . Memory (MB): peak =
2482.285 ; gain = 160.074 ; free physical = 92399 ; free virtual = 154163
# route_design
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.


Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8
CPUs
Checksum: PlaceDB: d85c0162 ConstDB: 0 ShapeSum: aaa4a45b RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: 11a82b5a4

Time (s): cpu = 00:00:23 ; elapsed = 00:00:20 . Memory (MB): peak = 2485.914 ;
gain = 3.629 ; free physical = 92261 ; free virtual = 154025
Post Restoration Checksum: NetGraph: 625052f4 NumContArr: b83262b0 Constraints: 0
Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will operate
in resource-optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 11a82b5a4

Time (s): cpu = 00:00:23 ; elapsed = 00:00:20 . Memory (MB): peak = 2491.902 ;
gain = 9.617 ; free physical = 92229 ; free virtual = 153993

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 11a82b5a4
```

```
Time (s): cpu = 00:00:23 ; elapsed = 00:00:20 . Memory (MB): peak = 2491.902 ;
gain = 9.617 ; free physical = 92229 ; free virtual = 153993
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: fc7a541c

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2503.168 ;
gain = 20.883 ; free physical = 92220 ; free virtual = 153984

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: 1c739b27a

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2505.168 ;
gain = 22.883 ; free physical = 92220 ; free virtual = 153984

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 207
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: 173b77e37

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2505.168 ;
gain = 22.883 ; free physical = 92220 ; free virtual = 153984
Phase 4 Rip-up And Reroute | Checksum: 173b77e37

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2505.168 ;
gain = 22.883 ; free physical = 92220 ; free virtual = 153984

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: 173b77e37

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2505.168 ;
gain = 22.883 ; free physical = 92220 ; free virtual = 153984

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: 173b77e37

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2505.168 ;
gain = 22.883 ; free physical = 92220 ; free virtual = 153984
Phase 6 Post Hold Fix | Checksum: 173b77e37

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2505.168 ;
gain = 22.883 ; free physical = 92220 ; free virtual = 153984
```

```
Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization    = 0.418418 %
  Global Horizontal Routing Utilization  = 0.527351 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets               = 0
  Number of Unrouted Nets             = 0
  Number of Partially Routed Nets     = 0
  Number of Node Overlaps             = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 33.3333%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 38.7387%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 35.2941%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 45.5882%, No Congested Regions.

------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 173b77e37

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2505.168 ;
gain = 22.883 ; free physical = 92220 ; free virtual = 153984
```

```
Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: 173b77e37

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2506.168 ;
gain = 23.883 ; free physical = 92219 ; free virtual = 153983

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: dfdbc185

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2506.168 ;
gain = 23.883 ; free physical = 92220 ; free virtual = 153984
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:27 ; elapsed = 00:00:21 . Memory (MB): peak = 2506.168 ;
gain = 23.883 ; free physical = 92252 ; free virtual = 154016

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
8 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:29 ; elapsed = 00:00:24 . Memory (MB): peak =
2506.168 ; gain = 23.883 ; free physical = 92252 ; free virtual = 154016
# write_bitstream -force cpu.bit
Command: write_bitstream -force cpu.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties:
Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the
current_design.  Configuration bank voltage select (CFGBVS) must be set to VCCO
or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in
order to determine the I/O voltage support for the pins in bank 0.  It is
suggested to specify these either using the 'Edit Device Properties' function in
the GUI or directly in the XDC file using the following syntax:

 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND
```

```
 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
WARNING: [DRC PDRC-153] Gated clock check: Net
ProgramCounter/registers_reg[0][31][0] is a gated clock net sourced by a
combinational pin ProgramCounter/control_reg[13]_i_2/O, cell
ProgramCounter/control_reg[13]_i_2. This is not good design practice and will
likely impact performance. For SLICE registers, for example, use the CE pin to
control the loading of data.
WARNING: [DRC UCIO-1] Unconstrained Logical Port: 100 out of 100 logical ports
have no user assigned specific location constraint (LOC). This may cause I/O
contention or incompatibility with the board power or connectivity affecting
performance, signal integrity or in extreme cases cause damage to the device or
the components to which it is connected. To correct this violation, specify all
pin locations. This design will fail to generate a bitstream unless all logical
ports have a user specified site LOC constraint defined.  To allow bitstream
creation with unspecified pin locations (not recommended), use this command:
set_property SEVERITY {Warning} [get_drc_checks UCIO-1].  NOTE: When using the
Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a
.tcl file and add that file as a pre-hook for write_bitstream step for the
implementation run.  Problem ports: pc_out[31:0], rs_out[31:0], rt_out[31:0],
cpu_clk, cpu_overflow, cpu_reset, and cpu_zero.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 3 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more
information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./cpu.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:15 ; elapsed = 00:00:15 . Memory (MB):
peak = 2850.988 ; gain = 344.820 ; free physical = 92203 ; free virtual = 153971
INFO: [Common 17-206] Exiting Vivado at Sun Jun 27 16:22:52 2021...
```

Conclusion

The VHDL components sign_extend.vhd, d_cache.vhd, i_cache.vhd, and pc_reg.vhd were successfully synthesized. The CPU required the use of all of these components. During simulation, it is required to compile every other VHDL file before simulating the CPU entity. Similarly for synthesis, the TCL script must also include the command "read_vhdl { ./Code/vhdl_filename.vhd }" for every VHDL file needed for synthesis. The CPU entity uses components as separate files so it is required to include this command for successful bitstream generation.

VHDL files from previous labs:

alu.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity alu is
port(
    x, y       : in std_logic_vector(31 downto 0); -- two input operands

    add_sub     : in std_logic ; -- 0 = add, 1 = sub

    logic_func  : in std_logic_vector(1 downto 0 ) ; -
- 00 = AND , 01 = OR , 10 = XOR , 11 = NOR

    func        : in std_logic_vector(1 downto 0 ) ; -
- 00 = lui , 01 = setless , 10 = arith , 11 = logic

    output      : out std_logic_vector(31 downto 0) ;
    overflow    : out std_logic;
    zero        : out std_logic
    );
end alu ;


architecture alu_arch of alu is

signal result, logic_unit, less: std_logic_vector(31 downto 0);
signal overflow_check : std_logic_vector(2 downto 0);

begin

    process(x, y, func, logic_func, add_sub, result, logic_unit, overflow_check,
less)
    begin
```

```
        overflow_check <= result(result'high) & x(x'high) & y(y'high);


        case add_sub is
            when '0' => result <= x + y;
                    if ((overflow_check = "100") OR (overflow_check = "011")) the
n
                        overflow <= '1';
                    else
                        overflow <= '0';
                    end if;

            when '1' => result <= x - y;
                    if ((overflow_check = "010") OR (overflow_check = "101")) the
n
                        overflow <= '1';
                    else
                        overflow <= '0';
                    end if ;
            when others =>
        end case;

        case logic_func is
            when "00" => logic_unit <= x AND y;

            when "01" => logic_unit <= x OR y;

            when "10" => logic_unit <= x XOR y;

            when "11" => logic_unit <= x NOR y;

            when others =>
        end case;

        if (result = x"00000000") then
            zero <= '1';
        else
            zero <= '0';
        end if;

        less <= x - y;

        case func is
            when "00" => output <= y;
```

```
            when "01" => output <= "00000000000000000000000000000000" & less(less'
high);

            when "10" => output <= result;

            when "11" => output <= logic_unit;

            when others =>
        end case;

    end process;
end alu_arch;
```

next_address.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity next_address  is
port(
    rt, rs          : in std_logic_vector(31 downto 0); -- two register inputs

    pc              : in std_logic_vector(31 downto 0);

    target_address  : in std_logic_vector(25 downto 0);

    branch_type     : in std_logic_vector(1 downto 0);

    pc_sel          : in std_logic_vector(1 downto 0);

    next_pc         : out std_logic_vector(31 downto 0)
    );
end next_address;


architecture pc_arch of next_address is


begin
    process(rt, rs, pc, target_address, branch_type, pc_sel)
    begin
        case pc_sel is
```

```
            -- no unconditional jump
            when "00" =>
                case branch_type is
                    when "00" =>
                        next_pc <= pc + x"00000001"; -- no branch
                    when "01" =>
                        if (rs = rt) then
                            next_pc <= pc + x"00000001" + ((31 downto 16 => targe
t_address(15)) & target_address(15 downto 0));
                        else
                            next_pc <= pc + x"00000001"; -- no branch, rs /= rt
                        end if;

                    when "10" =>
                        if (rs /= rt) then
                            next_pc <= pc + x"00000001" + ((31 downto 16 => targe
t_address(15)) & target_address(15 downto 0));
                        else
                            next_pc <= pc + x"00000001"; -- no branch, rs = rt
                        end if;

                    when "11" =>
                        if (rs < 0) then
                            next_pc <= pc + x"00000001" + ((31 downto 16 => targe
t_address(15)) & target_address(15 downto 0));
                        else
                            next_pc <= pc + x"00000001"; -- no branch, rs >= 0
                        end if;
                    when others =>
                end case;

            -- jump
            when "01" =>
                next_pc <= "000000" & target_address;

            -- jump register
            when "10" =>
                next_pc <= rs;

            when others =>
        end case;
    end process;
end pc_arch;
```

regfile.vhd

```
-- 32 x 32 register file
-- two read ports, one write port with write enable

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity regfile is
port(
    din             : in std_logic_vector(31 downto 0);
    reset           : in std_logic;
    clk             : in std_logic;
    write           : in std_logic;
    read_a          : in std_logic_vector(4 downto 0);
    read_b          : in std_logic_vector(4 downto 0);
    write_address   : in std_logic_vector(4 downto 0);
    out_a           : out std_logic_vector(31 downto 0);
    out_b           : out std_logic_vector(31 downto 0)
);
end regfile;

architecture regfile_arch of regfile is

type register_array is array (0 to 31) of std_logic_vector(31 downto 0);
signal registers: register_array;

begin
    -- read process
    process(read_a, read_b, registers)
    begin
        out_a <= registers(conv_integer(read_a));
        out_b <= registers(conv_integer(read_b));
    end process;

    -- write process
    process(din, reset, clk, write, write_address)
    begin
        if (reset = '1') then
            for i in 0 to 31 loop
                registers(i) <= (others => '0');
```

```
            end loop;

        elsif ((rising_edge(clk)) AND (write = '1')) then
            registers(conv_integer(write_address)) <= din;
        end if;

    end process;

end regfile_arch;
```