National University of Computer & Emerging Sciences, Karachi
Spring 2020 CS-Department
Final Examination
7th July 2019 , 9:00 AM – 12:00 PM

Course Code: EE227	**Course Name: Digital Logic Design**
Instructor Names: Rabia Tabassum, Behraj Khan, Bilal Muhammad Yousuf , Musawar ali,	
Student Roll No:	**Section No:**

Instructions:

- Read each question completely before answering it. There are 5 questions on 4 pages
- The Exam will start on: 9:00 am; and will End at: 12:30 pm, including the submission time(30mints)
- You will attempt this paper offline, in your hand writing, however, for some questions, you may use your PC
- In case of any ambiguity, you may make assumption. But your assumption should not contradict any statement in the question paper
- All the answers must be solved according to the SEQUENCE given in the question paper.
- Show all steps clearly
- You may use cam-scanner, MS lens or any equivalent application to scan and convert your hand-written answer sheets + any screenshot in a single PDF file
- The paper should be submitted using our Google classroom. For this purpose, you are given 30 minutes, already mentioned in the above instructions.
- Put your signature on every page along with YOUR Roll No/ID, Section and page number.

Time: 180 minutes. **Max Marks**: **100 points**

Question 1: (Boolean algebra, and Combinational Logic Analysis) [4+2+4 Points]

(a) Implement the following Boolean function F using the two-level forms: AND-NOR and OR-NAND , F (A, B, C, D) = Σ (0, 6, 8, 10, 11, 12, 15) , The variables should be the first four alphabets of your name. Like if someone has name HASSAN, The variables would be HASN. If an alphabet comes two times discard it and go to next. Don't care terms for the K-MAP would be your roll number. Like If someone has Roll number 19K-2098, the don't care terms would be d (1, 2, 9). Make sure that there are no repetitions in don't care terms and don't care terms must not be same as minterms.

(b) Convert the above problem into standard POS, expression using the truth table and minimize using K-map.

(c) Design a combinational circuit with four inputs and one output. The Algebraic expression must be minimized using K-MAP. The output must be one for the digits which are present in your Roll Number Digits. Any duplications must be avoided.

Question 2: (Functions of Combinational Logic) [5+5+1+5+4 Points]

(a) For function F(x, y, z) = x'y'z + x'yz + x'yz' + xyz' + xy'z We want to design a circuit to implement function F(x,y,z) using two different methods. First design is called design MUX . Function F(x,y,z) is implemented using Multiplexer. Second design is design DEC. F(x,y,z) is designed using Decoder.

(b) Design a magnitude comparator circuit for 2-bit binary numbers A=A1A0 and B=B1B0. The outputs are F, G, and H, where F is 1 if A>B, G is 1 if A=B, and H is 1 if A<B.

(i) Fill in the truth table for the three outputs of the comparator and determine their function as sum of minterms.

(ii) Implement your comparator design using a 4-to-16 line decoder.

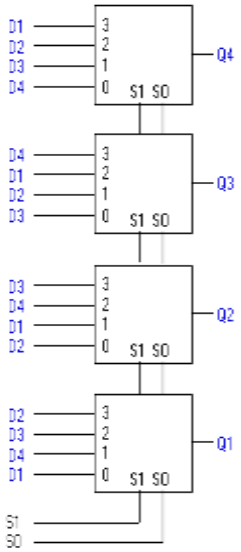
(c) Show the logic required to convert your student id in binary number (for example if your student id is 19K-0982 then this id in binary is 10111010100000110) to Gray code.

(d) Design a 4-to-16-line decoder by using the minimum number of 2-to-4-line decoders. The 2-to-4-line decoders have an enable input ('1'=enabled) and the designed 4-to-16-line decoder does not have an enable. Name the inputs A0...A3 and the outputs D0...D15. Do not draw the internal circuit diagrams for the decoders.

(e) Describe what the following circuit(Fig-1) does in one or two sentences. Begin by filling in the truth-table below. The four components are all 4:1 multiplexers (S1=1 and S0=0 connect input 2 to the single output) with identical select inputs.

S1	S0	Q4	Q3	Q2	Q1
0	0				
0	1				
1	0				
1	1				

Fig-1



Question 3: (Latches and Flip Flop) [7.5+7.5+5 Points]

(a) Your Roll Number is applied as serial data to the flip-flop through the OR gates as indicated in Fig-2. Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH. Rightmost bits are applied first.

Example: If 19K-2098 is your number then serial data would be like:

J1	0	0	0	1
J2	1	0	0	1
J3	0	0	1	0
K1	0	0	0	0
K2	1	0	0	1
K3	1	0	0	0

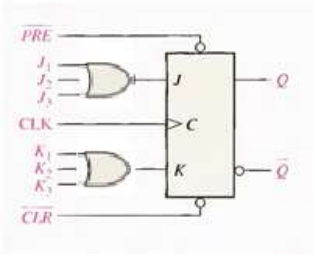


Fig-2

(b) Consider the above question Q3(a) with the same J and K inputs (in form of waveform) but with the PRE and CLR inputs as shown in Fig-3 in relation to the clock. Draw the timing diagram of inputs J1,J2, J3, K1, K2, K3 and the resulting Q output (which is initially LOW).

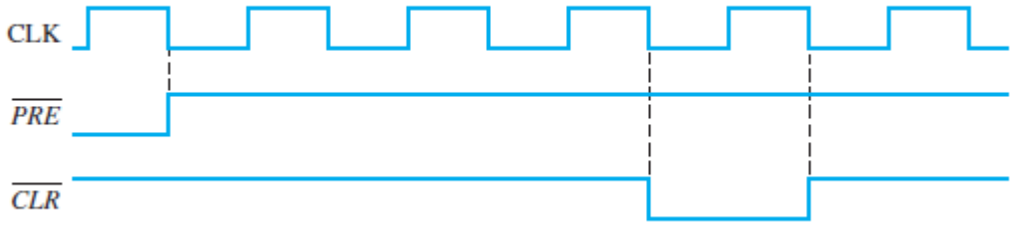


Fig-3

(c) Develop the Q output waves for the active low SR flip-flop with input wave forms from the digits in your roll number. If the roll number is 20K-0985, then SR inputs would be, first two digits for S and last two for R, the numbers before K must not be included.

S	0				9			
S	0	0	0	0	1	0	0	1
R	8				5			
R	1	0	0	0	0	1	0	1

Question 4: (Counter) [10+20+10 Points]

(a) Show how to connect a 74HC93 4-bit asynchronous counter for each of the following moduli: (i) 14 - right most digit of your student id. For example if your student id is 19k-0982 then consider moduli (14 -2 = 12). you must consider the scenario as per your student id (ii) consider the same scenario in part (i) by adding 8 to the right most digit to your student id number for example 8 + 2 = 10.

(b) Design an up/down counter to produce the following binary sequence using D or JK flip flop. The binary sequence should be determined by following way. Take your Roll Number remove K from roll number, add 9999 to your roll number and then determine the counter sequence. If there are duplicates just remove the duplicate digits and randomly place any of your choice. For example the roll number is 20K-0985, you will determine the sequence in following manner

i) Remove K, which makes 200985
ii) Add 9999 to which makes, 200985+9999= 210984
iii) The counter sequence would be 2, 1, 0, 9, 8, 4…

(c) Determine the sequence of the counter in fig-4 till max 8 clock pulses. Begin with the state having the unit digit sum of your roll number digits. Like in 19k-2095 (192095) sum 26 you would take 6 as the start of the counter.

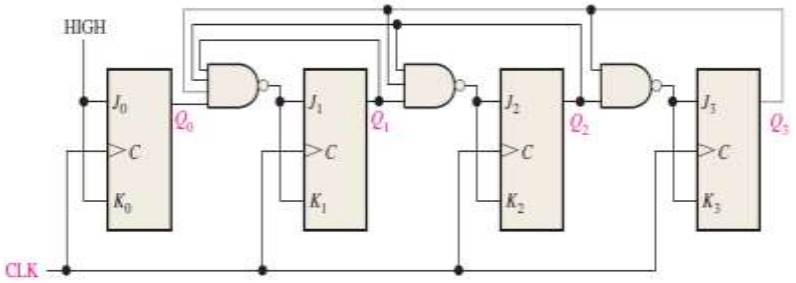


Fig-4

Question 5: (Shift Register) **[4+3+3 Points]**

(a) We would like to design a 4-bit register with the following specifications. The register is supposed to have four modes of operation given by the following table. It has two control inputs s0 and s1

s_0	s_1	Operation
0	0	Unchanged
0	1	Complement of the output
1	0	Clear (set register's contents to 0)
1	1	Load parallel data

(b) Draw the logic diagram for a 5-bit ring counter. If a 5-bit ring counter has an initial state equal to the first five bits from right to left of your student id in binary coded decimal, determine the waveform for each Q output .(For example if your student id is 19K-0982, then mentioned id in BCD is 000110010000100110000010 so in the mentioned case initial sate is 00010). You must consider this scenario as per your student id.

(c) Design a modulus-10 Johnson counter using J K flip flop. Write the sequence in tabular form.

GOOD LUCK