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Reg. No.: 2023-EE-115	Marks Obtained: _____

Lab Manual

Experiment 4

Combinational Circuit Design: RGB LED using K-Maps

DSD Lab Manual Evaluation Rubrics

Assessment	Total Marks	Marks Obtained	0-30%	30-60%	70-100%
Code Organization (CLO1)	3		No Proper Indentation and descriptive naming, no code organization. Zero to Some understanding but not working	Proper Indentation or descriptive naming or code organization. Mild to Complete understanding but not working	Proper Indentation and descriptive naming, code organization. Complete understanding, and proper working
Simulation (CLO2)	5		Simulation not done or incorrect, without any understanding of waveforms	Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms	Working simulation without any errors, etc and complete understanding of waveforms
FPGA (CLO2)	2		Not implemented on FPGA and questions related to synthesis and implementation not answered.	Correctly Implemented on FPGA or questions related to synthesis and implementation answered.	Correctly Implemented on FPGA and questions related to synthesis and implementation answered.

TASKS:

a. Truth Table of the Circuit:

a[1]	*a[0]*	*b[1]*	*b[0]*	*a > b* Purple	*a = b* Yellow	*a < b* Cyan	*Red*	*Green*	*Blue*
0	*0*	*0*	*0*	*0*	*1*	*0*	*1*	*1*	*0*
0	*0*	*0*	*1*	*0*	*0*	*1*	*0*	*1*	*1*
0	*0*	*1*	*0*	*0*	*0*	*1*	*0*	*1*	*1*
0	*0*	*1*	*1*	*0*	*0*	*1*	*0*	*1*	*1*
0	*1*	*0*	*0*	*1*	*0*	*0*	*1*	*0*	*1*
0	*1*	*0*	*1*	*0*	*1*	*0*	*1*	*1*	*0*
0	*1*	*1*	*0*	*0*	*0*	*1*	*0*	*1*	*1*
0	*1*	*1*	*1*	*0*	*0*	*1*	*0*	*1*	*1*
1	*0*	*0*	*0*	*1*	*0*	*0*	*1*	*0*	*1*
1	*0*	*0*	*1*	*1*	*0*	*0*	*1*	*0*	*1*
1	*0*	*1*	*0*	*0*	*1*	*0*	*1*	*1*	*0*
1	*0*	*1*	*1*	*0*	*0*	*1*	*0*	*1*	*1*
1	*1*	*0*	*0*	*1*	*0*	*0*	*1*	*0*	*1*
1	*1*	*0*	*1*	*1*	*0*	*0*	*1*	*0*	*1*
1	*1*	*1*	*0*	*1*	*0*	*0*	*1*	*0*	*1*
1	*1*	*1*	*1*	*0*	*1*	*0*	*1*	*1*	*0*

b. K-map:

1. RED

a[1] a[0] \ b[1] b[0]	*00*	*01*	*11*	*10*
00	***1***	***0***	***0***	***0***
01	***1***	***1***	***0***	***0***
11	***1***	***1***	***1***	***1***
10	***1***	***1***	***0***	***1***

Equation using essential prime implicants:
red = (~b1 & ~bo) | (ao & ~b1) | (a1 & ~b1) | (a1 & ao) | (a1 & ~bo)

2. GREEN

a[1] a[0] \ b[1] b[0]	*00*	*01*	*11*	*10*
00	***1***	***1***	***1***	***1***
01	***0***	***1***	***1***	***1***
11	***0***	***0***	***1***	***0***
10	***0***	***0***	***1***	***1***

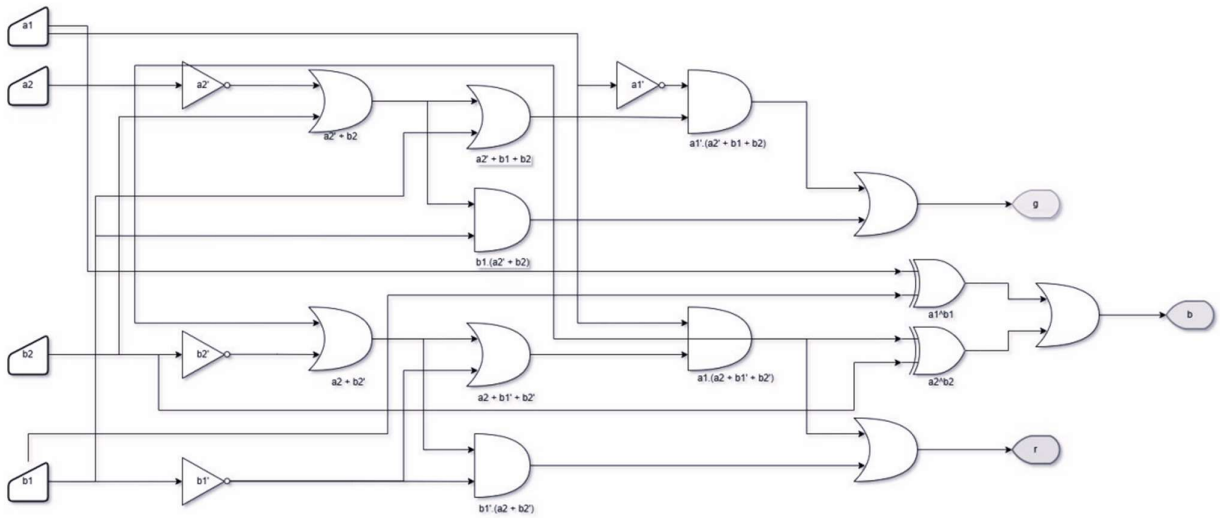
Equation using essential prime implicants:
green = (~a1 & ~ao) | (b1 & bo) | (~a1 & bo) | (~a1 & b1) | (~ao & b1)

3. BLUE

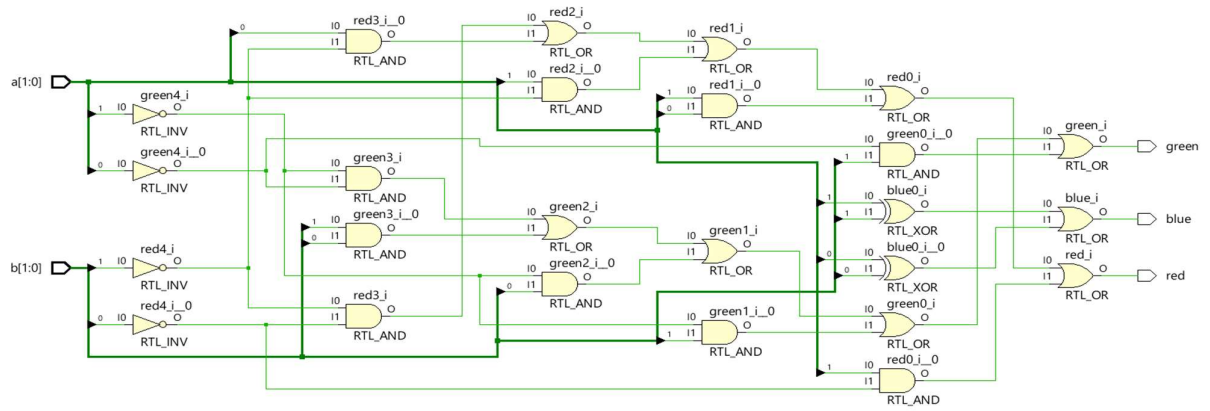
a[1] a[0] \ b[1] b[0]	*00*	*01*	*11*	*10*
00	***0***	***1***	***1***	***1***
01	***1***	***0***	***1***	***1***
11	***1***	***1***	***0***	***1***
10	***1***	***1***	***1***	***0***

Equation using essential prime implicants:
blue = (a1 ^ b1) | (ao ^ bo)

c.



d. Circuit diagram:



e. Combinational Delay:

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a[0]	blue	9.175	SLOW	2.819	FAST
a[0]	green	8.819	SLOW	2.624	FAST
a[0]	red	8.981	SLOW	2.707	FAST
a[1]	blue	8.451	SLOW	2.551	FAST
a[1]	green	8.059	SLOW	2.363	FAST
a[1]	red	8.255	SLOW	2.442	FAST
b[0]	blue	9.001	SLOW	2.746	FAST
b[0]	green	8.653	SLOW	2.564	FAST
b[0]	red	8.817	SLOW	2.649	FAST
b[1]	blue	9.311	SLOW	2.911	FAST
b[1]	green	9.052	SLOW	2.751	FAST
b[1]	red	9.216	SLOW	2.831	FAST

Maximum Combinational delay is from b[1] to blue which is 9.311 ns.

f. Resource Utilization:

The number of **LUTs utilized** is **2**, and the number of **IO ports utilized** is **7**

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	2	0	63400	<0.01
LUT as Logic	2	0	63400	<0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	7	0	210	3.33
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00