Video lecture# 17-29, 32, 35-38, 40, 42, 44-49.

Exercise Questions:

- Chapter 5 (5.14 - 5.28).
- Chapter 6 (6.9-6.12, 6.18, 6.21, 6.22(b), 6.22-6.24(a,c,d)).

Major topics:

1. Decoder
2. Encoder
3. Priority encoder
4. Multiplexer
5. Demultiplexers
6. Magnitude comparator
7. Flip flops JK RS T
8. Flip Flop excitation table
9. Design of sequential circuits
10. Analysis of sequential circuit.

Decoder:

1. Basic design, 2x3 3x8 4x16 decoder
2. With Enable input, 2x3 3x8 4x16 decoder
3. Decoders using NAND gates.
4. Designing 3x8 decoder using 2x4 decoders and some external circuitry
5. Designing 4x16 decoder using 2x4 decoders and some external circuitry
6. Implementation of functions through decoders and some external circuitry
7. Designing half/full adder and half/full subtractor using decoders
8. BCD to decimal decoder
9. Questions related to ***number and size of decoders*** while code converting or designing diff size decoders using smaller size decoder will be asked in exam (e.g bcd to excess-3 and all others).

Encoder:

1. Basic design, 4x2 encoder
2. With valid output, 4x2 encoder
3. With enable input and valid output, 4x2 encoder

Priority Encoder:

1. Design a 4x2 priority encoder using k-map.
2. Design 4x2 8x3 priority encoders using boolean algebra.

Multiplexer:

1. 2x1 4x1 multiplexer (table expression circuit)
2. Design 8x1 multiplexer using two 4x1 multiplexer and one 2x1 multiplexer.
3. Design 8x1 multiplexer using two 4x1 multiplexer and one OR gate.
4. Implementation of functions using MUX
5. Implementation of functions (x,y,z) using 4x1 MUX
6. Implementation of function (w,x,y,z) using 8x1 MUX
7. Implementation of full adder and full subtractor using 4x1 MUX
8. Questions related to ***number and size of multiplexer*** while code converting or designing diff size decoders using smaller size decoder will be asked in exam (e.g bcd to excess-3 and all others).

Demultiplexer:

1. 1x4 1x8 DEMUX
2. 1x4 DEMUX using enable input
3. Design of 1x8 DEMUX with smaller sizes DEMUXs
4. Implementation of functions using DEMUX

Magnitude Comparator:

2-bit 3-bit 4-bit magnitude comparator

- A==B
- A!=B
- A<B
- A>B
- A<=B (using A<B OR A==B)
- A>=B (using A>B OR A==B)

Flip Flops:

1. Basic SR flip flop using NOR and NAND gates and their comparison
2. Gated SR Latch (SR flip flop using Enable input both using NOR and NAND)
3. Edge Triggered(clock pulse) SR flip flop using NOR and NAND gates
4. JK flip flop using NOR and NAND gates.
5. T flip flop using NOR and NAND gates
6. Excitation Table(RS, JK, T)

Sequential Circuits:

1. A statement will be given and we have to derive the state diagram, state table and curcuit.
- Up counter using two JK/ SR flip flops.
- Down counter using two JK/SR flip flops.
- Up and down counter using two JK/ SR flip flops.

2. A circuit diagram will be given and we have to create a state table and state diagram through it.