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<i>Assignment/Lab Number:</i>	<i>Project</i>
<i>Assignment/Lab Title:</i>	<i>Multistage Amplifier Design project</i>

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1. Introduction

The main purpose of this project is to design, simulate, analyze, implement, and test a single-supply, multistage, inverting, transistor amplifier that fulfills a set of specifications.

2. Specifications

- Power supply: **+10V** relative to the ground;
- Quiescent current drawn from the power supply: no larger than **10 mA**;
- No-load voltage gain (at 1 kHz): $|A_{vo}| = 50 (\pm 10\%)$;
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 kHz and with $RL = 1 k\Omega$): no smaller than **90%** of the no-load voltage gain;
- Maximum loaded output voltage swing (at 1 kHz and $RL = 1 k\Omega$): no smaller than 4 V peak to peak;
- Input resistance (at 1 kHz): no smaller than **20 kΩ**;
- Amplifier type: inverting or non-inverting;
- Frequency response: 20 Hz to 50 kHz (**-3dB** response);
- Type of transistors: BJT;
- Number of transistors (stages): no more than 3;
- Resistances permitted: values smaller than **220 kΩ** from the E24 series;
- Capacitors permitted: **0.1 μF, 1.0 μF, 2.2 μF, 4.7 μF, 10 μF, 47 μF, 100 μF, 220 μF**;
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit.

Notes:

- The output voltage must be free from distortions (clipping, etc.) in all test conditions.
- The source resistance R_S must be 600Ω for all tests.

Assumptions taken:

- $V_{BE,ON} = 0.7 \text{ V}$
- $V_{CE, SAT} = 0.3 \text{ V}$
- $\beta \text{ (current gain)} = 150$
- $V_T = 26 \text{ mV}$

3. Design of the Amplifier

For the designed multistage amplifier's setup, the sequence of CC + CE + CC is utilized, where the CC amplifier serves as an effective buffer for the CE stage, owing to its high input impedance, unity gain, and low output impedance. The initial CC stage is tasked with maintaining an input impedance exceeding 20 kΩ. This is achievable due to the capability of the CC stage to determine its input impedance through the following formula:

$$R_{in} = R_1 \parallel R_2 \parallel (g_{m1} + (\beta + 1)R_{E1})$$

The output CC stage is crucial in preserving the CE amplifier's effectiveness. Moreover, It's evident from the voltage gain equation of the CE amplifier that applying a load significantly reduces its gain, compromising its efficiency.

$$A_v = -g_m(R_C \parallel R_L)$$

The CC amplifier's high input impedance means it acts as the load resistance (R_L) in the above computation. Because CC amplifiers have high input impedance, the parallel combination of R_C and R_L closely approximates RC . This keeps the gain almost equivalent to the initial gain of the CE amplifier.

The CE stage is the key component in achieving the desired voltage gain of 50 V/V. The design process began with determining the steady-state voltages and currents. With a 10 V DC power source at our disposal, we opted to experimentally distribute this voltage across the transistor's five elements — R_C , R_E , and V_{CE} —to ensure the required adequate voltage swing is achieved. Consequently, V_{CE} will have a voltage of 4.38 V, which results in V_C and V_E having voltage values of 8.68 and 4.3 volts. Moreover, this distribution allows for the calculation of other parameters, such as g_m and the collector current. Subsequently, the input impedance of the CE stage was calculated and factored into the CC stage's input calculation, in parallel with R_E :

$$R_{in2} = R_3 \parallel R_4 \parallel (g_{m2} + (\beta + 1)(R_{E2} + R_{E3}))$$

4. Circuit configurations and Waveforms

This project involves analyzing and creating a multistage amplifier. The following created circuit in Figure 4.1 is the only tested circuit for this project. It depicts a three-stage amplifier configured in the sequence of CC, CE, and CC stages. The circuit features the amplifier with a switch for the load resistance of $1\text{ K}\Omega$ (allowing for the circuit to be open-circuited when the load resistor is removed, ie. no load resistance). This circuit was designed using the Multisim software platform. For the analysis, a frequency range from 20 Hz to 50 KHz was employed to generate Bode Plots, illustrating the relationship between magnitude and phase. The signal from the function generator used in this setup had a frequency of 1 KHz and a peak-to-peak amplitude of 50 milli-volts, chosen to minimize distortion in the output voltage waveform.

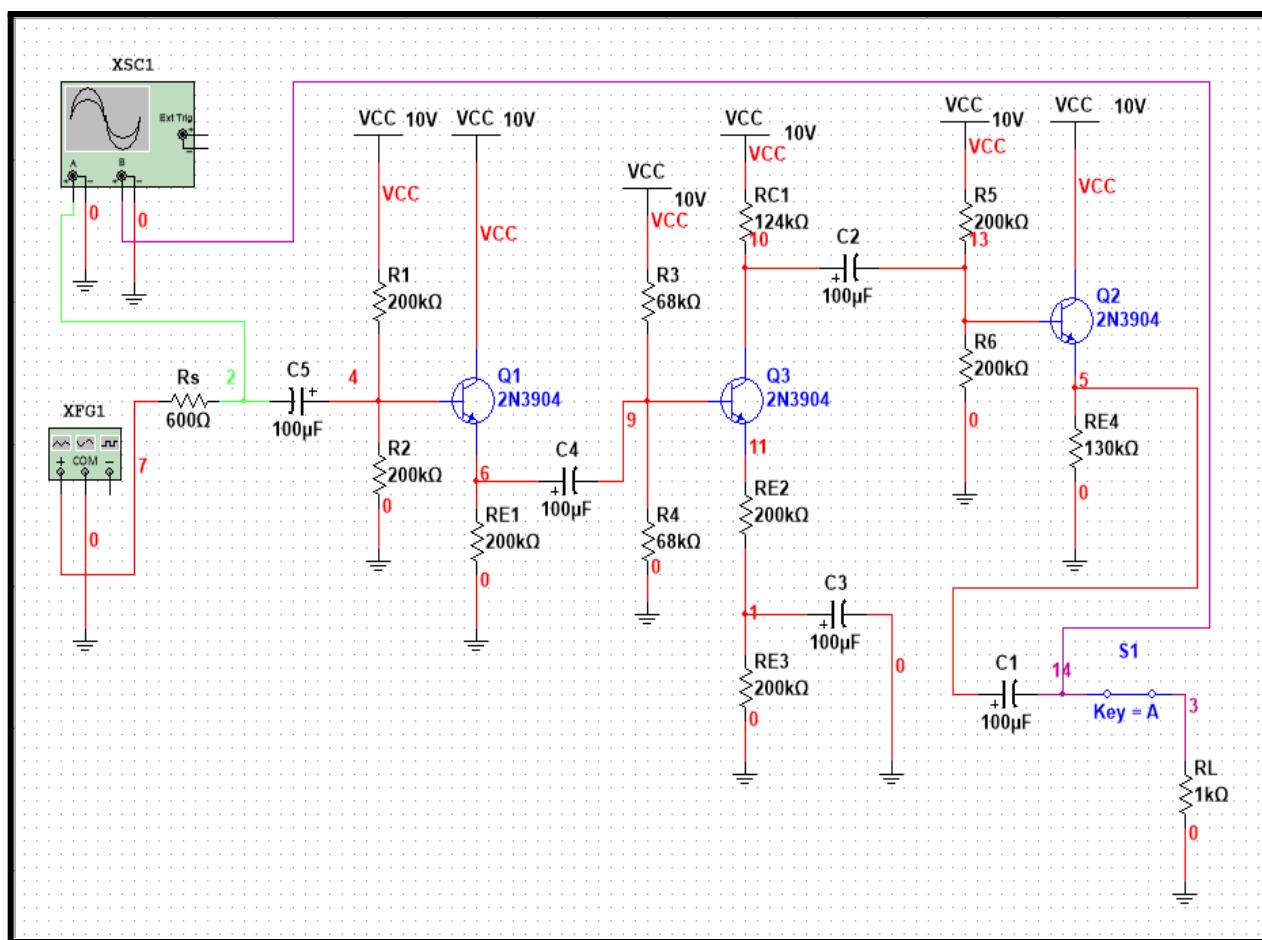
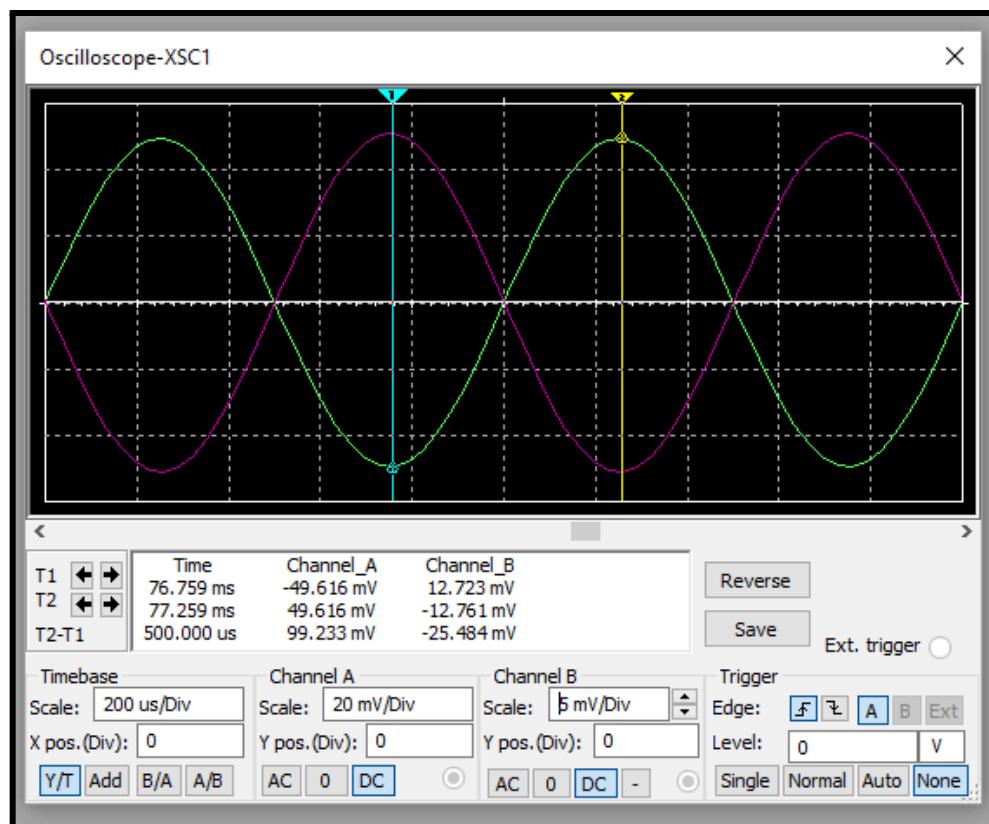
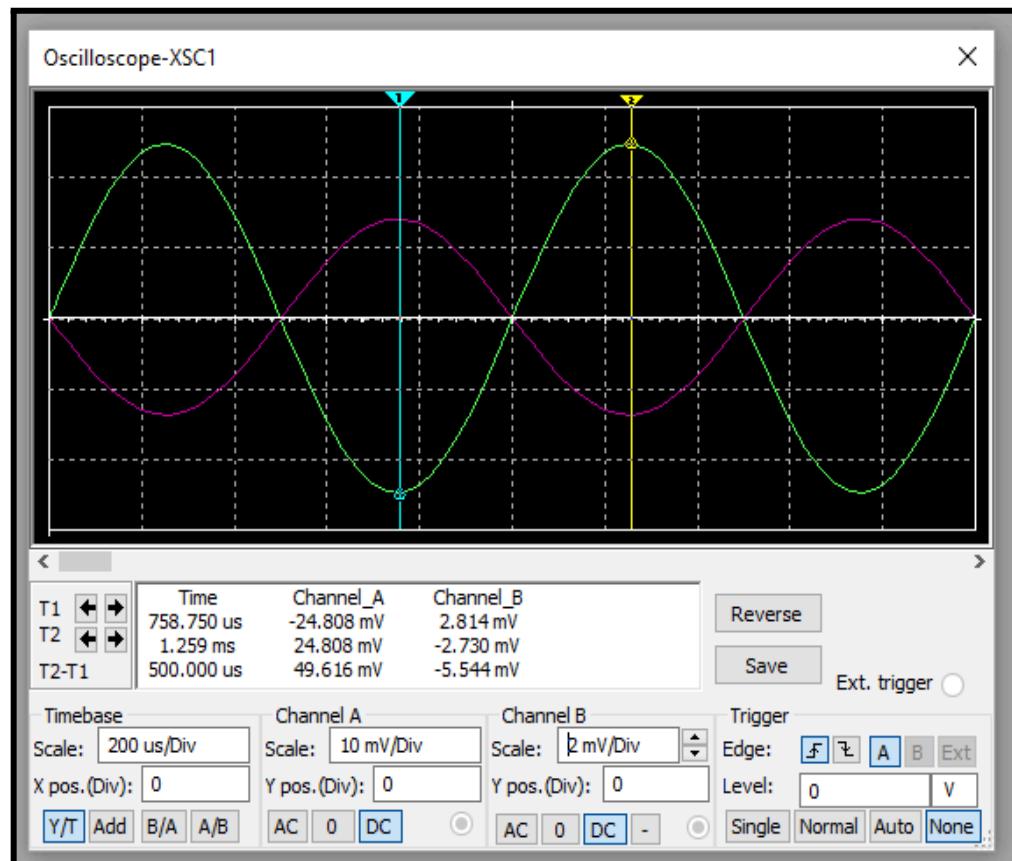


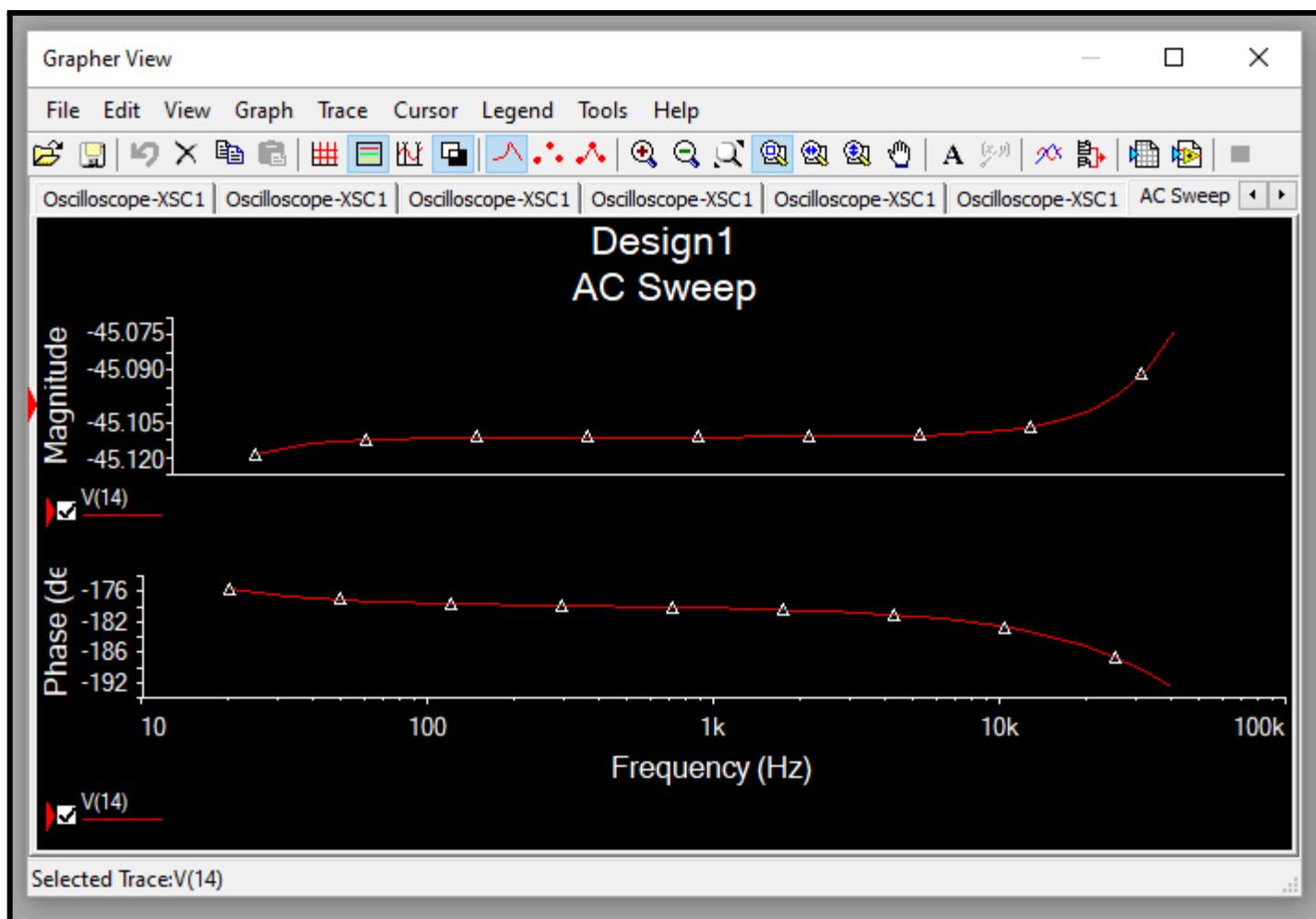
Figure 4.1: Multisim circuit schematic for the three-stage amplifier with a switch for open circuiting the load resistance when removed



Graph 4.1: Input (green) and output (pink) voltages of the circuit when load resistance is disconnected



Graph 4.2: Input (green) and output (pink) voltages of the circuit when load resistance is connected



Graph 4.3: Frequency response waveforms of the circuit of Figure 5 for the output voltage.

Overall, the constructed multistage amplifier successfully fulfilled the specified criteria, achieving the necessary threshold values in the simulation. However, certain inconsistencies were noted within the circuits. Initially, the current gain (β) value was fixed at 150, which impacted both the voltage gain and the steady-state currents. Although the resistors, being ideal within the specified range, and the capacitors, whose internal resistances influenced the BJT's current, showed some variance. Furthermore, the inversion of the input and output waveforms suggests that the CE amplifier is functioning correctly, which might also point to potential miscalculations in the resistances or currents. Despite these issues, the amplifier still met the overall design requirements.

5. Calculations

The calculations for the three-stage amplifier are shown below. For the calculations, the DC and AC analysis parts are separated into sub-sections.

Part I: DC Analysis

Analysis for stage E1
(CC amplifier)

$$V_{B1} = V_{cc} \left(\frac{R_2}{R_1 + R_2} \right) = 10V \left(\frac{200K\Omega}{400K\Omega} \right)$$

$$\therefore V_{B1} = 5V$$

V_{F1}

$$V_{BE} = 0.7V$$

I_{F1}

$$V_{F1} = I_{E1} R_{B1}$$

$$V_{BE} = V_{B1} - V_{E1} \rightarrow I_{E1} = \frac{V_{E1}}{R_{E1}}$$

$$0.7 = 5 - V_{E1}$$

$$\therefore V_{E1} = 4.3V$$

$$I_{E1} = \frac{4.3V}{200K\Omega}$$

$$\therefore I_{E1} = 2.15 \times 10^{-5} A$$

$$= 0.0215mA$$

$$= 21.5\mu A$$

I_{C1}

$$\therefore I_{C1} = \beta I_{B1}$$

$$= 2.136 \times 10^{-5} A$$

$$= 21.36 \mu A$$

I_{B1}

$$I_{E1} = I_{B1} + I_{C1}$$

$$I_{E1} = I_{B1} + \beta I_{B1}$$

$$I_{E1} = I_{B1}(\beta + 1)$$

$$\therefore I_{B1} = \frac{I_{E1}}{\beta + 1}$$

$$= 1.4238 \times 10^{-7} A$$

$$\frac{r_{m1}}{r_m} = \frac{r_{be}}{g_{m1}} = \frac{\beta}{g_{m1}} = 150$$

I_{R1}

$$I_{R1} = \frac{V_{cc} - V_{B1}}{R_1}$$

$$\therefore I_{R1} = \frac{10 - 5}{200K\Omega}$$

$$\therefore I_{R1} = 25\mu A$$

$$\therefore r_{e1} = \frac{r_{m1}}{\beta + 1}$$

r_{e1}

$$= \frac{52000}{43} \Omega$$

$$= 1209.30 \Omega$$

g_{m1}

$$g_{m1} = \frac{I_{C1}}{V_t}$$

$$\therefore g_{m1} = 0.8215 \text{ mS}$$

$$\therefore I_{R1} = 25\mu A$$

$$= \frac{52000}{43} \Omega$$

$$= 1209.30 \Omega$$

Analysis for stage 2 (CE amplified)

$$\frac{V_{B2}}{V_{B2} = V_{CC} \left(\frac{R_4}{R_3 + R_4} \right)} = 10 \left(\frac{68k}{136k} \right)$$

$$\therefore V_{B2} = 5V$$

$$\frac{I_{E2}}{I_{E2} = \frac{V_{E2}}{R_{E2} + R_{E3}}} = \frac{4.3V}{200k\Omega + 200k\Omega}$$

$$\therefore I_{E2} = 1.075 \times 10^{-5} = 10.75 \mu A$$

$$\frac{g_{m2}}{g_{m2} = \frac{I_{C2}}{V_t}} = \frac{10.68 \mu A}{26 \mu A} \therefore g_{m2} = 0.4107 \text{ MS}$$

$$\frac{I_{R3}}{I_{R3} = \frac{V_{CC} - V_{B2}}{R_3}}$$

$$\therefore I_{R3} = \frac{(10-5)V}{68k\Omega}$$

$$\therefore I_{R3} = 73.53 \mu A$$

$$\frac{V_{E2}}{V_{BE} = 0.7} \\ V_{BE} = V_{B2} - V_{E2} \\ 0.7 = 5 - V_{E2} \\ \therefore V_{E2} = 4.3V$$

$$\frac{I_{B2}}{I_{E2} = I_{B2}(\beta+1)} \\ \therefore I_{B2} = 7.12 \times 10^{-8} A$$

$$\frac{I_{C2}}{I_{C2} = \beta I_{B2}} \\ \therefore I_{C2} = 10.68 \mu A$$

$$\frac{r_{M2}}{r_{M2} = r_{BE} = \frac{\beta}{g_{m2}}} = \frac{365209.3023}{\Omega}$$

$$\frac{r_{e2}}{r_{e2} = \frac{r_{M2}}{\beta+1}} \\ \therefore r_{e2} = \frac{104000}{43} = 2418.6 \Omega$$

Analysis for Stage 3 (CC amplifier)

$$V_{B3} = \left(\frac{R_6}{R_5 + R_6} \right) V_{CC}$$

$$= \left(\frac{200k}{400k} \right) (10)$$

$$\therefore \underline{V_{B3} = 5V}$$

$$\underline{V_{BE}} = V_{B3} - V_{E3}$$

$$0.7 = 5V - V_{E3}$$

$$\therefore \underline{\underline{V_{E3} = 4.3V}}$$

$$\underline{I_{B3}}$$

$$I_{E3} = I_{B3} (\beta + 1)$$

$$\underline{I_{RS}}$$

$$I_{R5} = \frac{V_{CC} - V_{B3}}{R_5}$$

$$\frac{I_{E3}}{\beta + 1} = I_{B3}$$

$$\therefore \underline{\underline{I_{R5} = 25\mu A}}$$

$$\therefore \underline{\underline{I_{B3} = 2.190524707 \times 10^{-7} A}}$$

$$\underline{I_{E3}} \\ I_{E3} = \frac{V_{E3}}{R_{E4}} = \frac{4.3V}{130k}$$

$$\therefore I_{E3} = \frac{3.307692308 \times 10^{-5} A}{= 3.31 \times 10^{-5} A} \\ = 33.076 \mu A$$

$$\underline{I_{C3}} \\ I_{C3} = \beta I_{B3}$$

$$\therefore I_{C3} = \frac{3.285787061 \times 10^{-5} A}{= 32.86 \mu A}$$

$$\underline{g_{m3}}$$

$$g_{m3} = \frac{I_{C3}}{V_t} = 1.26376425t \times 10^{-3} S$$

$$\therefore \underline{\underline{g_{m3} = 1.26 mS}}$$

$$\underline{r_{e3}} \\ r_{e3} = r_{be3} = \frac{\beta}{g_{m3}} = 118,693.0233 \Omega$$

$$\underline{r_{e3}}$$

$$r_{e3} = \frac{r_{e3}}{\beta + 1}$$

$$\therefore \underline{\underline{r_{e3} = 786.0465116 \Omega}} \\ = 786.05 \Omega$$

Total Quiescent current drawn from the power supply
Sum of DC currents provided by power supply is:

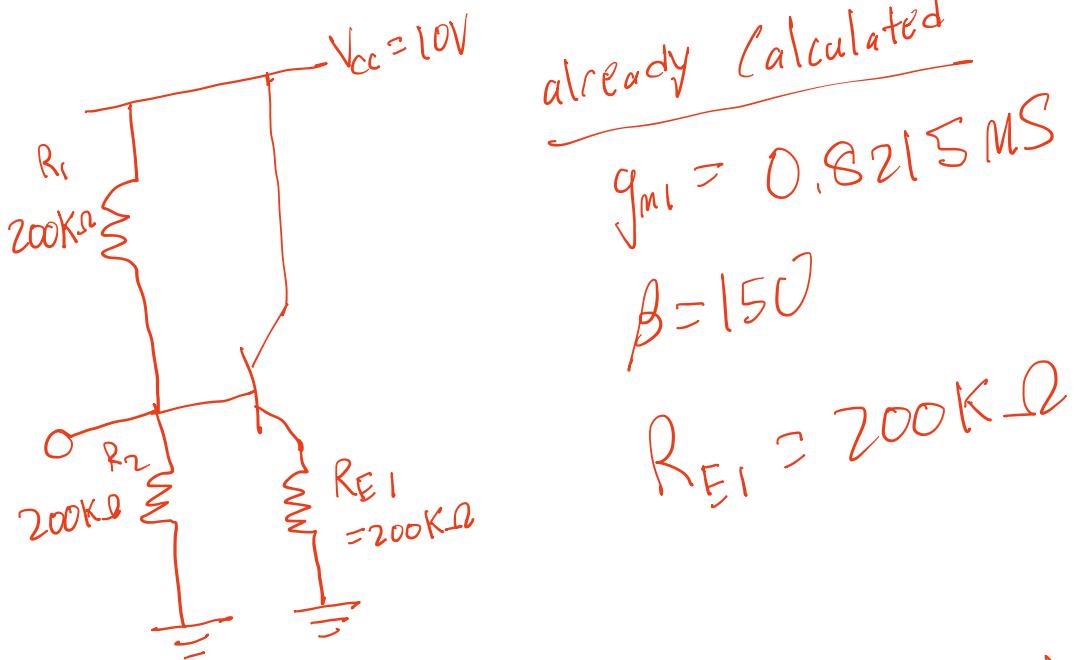
$$\begin{aligned} I &= I_{C1} + I_{C2} + I_{C3} + I_{R1} + I_{R3} + I_{R5} \\ &= 21.36 \mu A + 10.68 \mu A + 32.86 \mu A \\ &\quad + 25 \mu A + 73.53 \mu A + 25 \mu A \\ &= 1.8843 \times 10^{-4} A \\ \therefore I &= 0.18843 \text{ mA} \leq \underline{\underline{10 \text{ mA}}} \end{aligned}$$

meets requirement

The total Quiescent
current requirement
has been met

Part 2 - AC AnalysisInput CC Stage

R_{in} (Input resistance at 1KHz)



$$R_{in} = R_1 \parallel R_2 \parallel (g_m + (\beta + 1) R_{E1})$$

$$\therefore R_{in} = 99669.967\Omega$$

$$= 99.67\text{ K}\Omega > 20\text{ K}\Omega$$

\therefore The R_{in} requirement has been met.

No load Voltage gain

$$R_{in1} = 99669.967 \Omega \\ = 99.67 K\Omega$$

$$R_{in2} = R_3 \parallel R_4 \parallel \left(g_{m2} + (\beta+1)(R_{E2} + R_{E3}) \right)$$

$$\therefore R_{in2} = 33980.87169 \Omega$$

$$\therefore R_{in2} = 33.98 K\Omega$$

$$R_{in3} = R_5 \parallel R_6 \parallel \left(g_{m3} + (\beta+1)(R_{E4}) \right)$$

$$\therefore R_{in3} = 99669.967 \Omega \\ = 99.67 K\Omega$$

Loaded No load Voltage gains
and

$$\frac{V_o}{V_{in}} \geq A_v = A_{v1} \times A_{v2} \times A_{v3} \times A_{vs}$$

$$\frac{V_o}{V_{in}} = A_{vO} = A_{v01} \times A_{v02} \times A_{v03} \times (A_{vos})$$

~~$I_{E1}(R_E1 \parallel R_{in})$~~ = 0.9600299512
 $I_{E1}(R_E1 \parallel R_{in}) + r_{e1}$ = 0.96

$$\frac{V_o}{V_{in}} \geq A_{v01} = A_{v1} \geq$$

$$\frac{V_o}{V_{in}} = A_{v02} = A_{v2} = -\frac{g_{m2} R_C}{50.926} \approx \frac{V}{V}$$

$$R_L = 1K\Omega$$

$$r_{e3} = 120.3\Omega \therefore A_{v02} = A_{v2} = -50.926 \approx \frac{V}{V}$$

$$R_{EA} = 200K\Omega$$

$$\therefore R_{out} \approx \frac{1}{(1.26 \times 10^{-3})}$$

$$R_{out} \approx \frac{1}{g_{m3}}$$

$$g_{m3} = 1.26 \text{ mS}$$

Voltage gain of
CE amplifier with
a resistor load

$$A_v \approx \frac{1}{V}$$

$$R_{out} = 791.29 \Omega$$

$$R_L = 1K\Omega$$

$$\therefore \underline{R_{out} \ll R_L}$$

SO, A_v w/ load = A_v w/o load

$$A_{v03} = A_{v3} = g_{m3} R_{out} = g_{m3} \times \frac{1}{g_{m3}} = 1 \approx$$

No load Voltage gain

$$A_{VOS} = A_{VS} = \frac{R_{in1}}{R_{in1} + R_S} = \frac{1}{1544} = 0.994016$$

$$\frac{V_o}{V_i} = A_{VO} = A_{V1} \times A_{V2} \times A_{V3} \times A_{VOS}$$

stage 1 stage 2 stage 3 Input stage

$$\therefore A_{VO} = (0.9600299512) (-50.9268)(i) \frac{1}{(0.9940161544)}$$

Inverting

$$A_{VO} = -48.59869561 \frac{V}{V}$$

$$\therefore A_{VO} = -48.6 \frac{V}{V}$$

Loaded Voltage gain

$$A_V = A_{V1} \times A_{V2} \times A_{V3} \times A_{VS}$$

$$= (0.96) (-50.93) (i) (0.994)$$

$$\therefore A_V = -48.6 \frac{V}{V}$$

Inverting

requirements check

$$V_{CC} = 10V$$

$$R_S = 600\Omega$$

$$R_L = 1K\Omega$$

A_{V_0} (no load)

$$= -48.6 \frac{V}{V} \text{ which meets } 50 \pm 10\%$$

R_{in} (input resistance)

$$R_{in} = R_{in}$$

$$= 99.67 K\Omega$$

which meets
 $\underline{R_{in} \geq 20 K\Omega}$

A_v (loaded)

$$= -48.6 \text{ (which is not smaller than 90% of the no load gain)}$$

Quiescent Current

$$I = 0.18843mA < 10mA$$

\therefore If meets the requirement that $I \leq 10mA$