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Number Systems

 $N_{10} \to N_R$: Do N/R until 0 then build back using remainder.

 $(0 < N_{10} < 1) \rightarrow N_R$: Do $N \times R$ until number of terms sufficient and build sequentially using the ones digit.

1's complement: add last carry to right $\overline{N}=(2^n-1)-N$ 2's complement: flip bits then add 1 $N^*=2^n-N$

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Boolean Algebra

Identities	
Identities	X + 0 = X
	$X \cdot 0 = 0$
	X + 1 = 1
	$X \cdot 1 = X$
Idempotency	X + X = X
	$X \cdot X = X$

Negation	
Complementarity	X + X' = 1
	$X \cdot X' = 0$
Involution	(X')' = X

Laws	
Commutativity	$A \cdot B = B \cdot A$
	A + B = B + A
Associativity	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$
	A + (B+C) = (A+B) + C
Distributivity	$A \cdot (B+C) = A \cdot B + A \cdot C$
	$A + B \cdot C = (A + B)(A + C)$

De Morgan's Laws	
$(X \cdot Y)' = X' + Y'$	$\left(\prod_{i=1}^{n} X_i\right)' = \sum_{i=1}^{n} X_i'$
$(X+Y)'=X'\cdot Y'$	$\left(\sum_{i=1}^{n} X_i\right)' = \prod_{i=1}^{n} X_i'$

Theorems	
Uniting	XY + XY' = X
	(X+Y)(X+Y') = X
Absorption	X + XY = X
	X(X+Y) = X
Elimination	X + X'Y = X + Y
	X(X'+Y) = XY
Consensus	XY + X'Z + YZ = XY + X'Z
	(X+Y)(X'+Z)(Y+Z) = (X+Y)(X'+Z)
Other	(X+Y)(X'+Z) = XZ + X'Y

Binary Codes

Be careful about multiple ways to form a number!

Dec	BCD	6311	XS-3	2/5	Gray
0	0000	0000	0011	00011	0000
1	0001	0001	0100	00101	0001
2	0010	0011	0101	00110	0011
3	0011	0100	0110	01001	0010
4	0100	0101	0111	01010	0110
5	0101	0111	1000	01100	0111
6	0110	1000	1001	10001	0101
7	0111	1001	1010	10010	0100
8	1000	1011	1011	10100	1100
9	1001	1100	1100	11000	1101

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Look Up Tables

 $n \text{ inputs} \implies 2^n \text{ entries/states} \implies 2^{2^n} \text{ possible fns}$

Caution: Write out the formula (e.g., 2^{2^n}) for full marks

If n = 6, how many fins take 2 or fewer inputs?

- Exactly 0 inputs: $2^{2^0} = 2$ fns
- Exactly 1 input: $2^{2^1} 2^{2^0} = 2$ fns
 Choose 1 of 6 inputs: $N = \binom{6}{1} \times 2 = 6 \times 2 = 12$
- Exactly 2 inputs: $2^{2^2} 2^{2^1} 2^{2^0} = 10$ fms
 Choose 2 of 6 inputs: $N = \binom{6}{2} \times 2 = 15 \times 10 = 150$
- N = 2 + 12 + 150 = 164 fns total

SOP and POS

SOP: multiply out if one term is 1, whole expr is 1 POS: factor if one term is 0, whole expr is 0

 $\Rightarrow x \otimes y = (x \equiv y) = (x \oplus y)' = xy + x'y'$

Logic Gates

XNOR

NOT
$$x - x'$$

AND $x - xy$

OR $x - x + y$

NAND $x - x + y$

NAND $x - x + y'$

NOR $x - x + y' - x + y'$

NOR $x - x + y - x + y' - x + y'$

XOR $x - x + y$

Logic Gate Heuristics

NAND is inverted OR

f = (xy)' = x' + y'

NOR is inverted AND

f = (x+y)' = x'y'

NAND returns $0 \iff \text{all inputs } 1$

NOR returns $1 \iff$ all inputs 0

XOR returns $1 \iff \text{inputs have odd number of } 1s$

XNOR returns $1 \iff$ all inputs equivalent

XOR Properties	
$X \oplus 0 = X$	$X \oplus 1 = X'$
$X \oplus X = 0$	$X \oplus X' = 1$
$X \oplus Y = Y \oplus X$	
$(X \oplus Y) \oplus Z = X \oplus (Y \oplus Z)$	
$X(Y \oplus Z) = XY \oplus XZ$	
$(X \oplus Y)' = X \oplus Y' = X' \oplus Y = XY + X'Y' =$	$=(X\equiv Y)$

XNOR Properties	
$X \otimes 0 = X'$	$X \otimes 1 = X$
$X \otimes X = 1$	$X \otimes X' = 0$
$X \otimes X \otimes \cdots \otimes X = \begin{cases} X, \\ 1, \end{cases}$	n odd
$A \otimes A \otimes \cdots \otimes A = 1,$	n even

XOR and XNOR complements if even no of inputs given

$$A \oplus B \oplus C \oplus D = \overline{A \otimes B \otimes C \otimes D}$$

XOR and XOR same if odd no of inputs given

$$A \oplus B \oplus C = A \otimes B \otimes C$$

Minterms and Maxterms

Row	АВС	Minterms	Maxterms
0	0 0 0	A'B'C'	A + B + C
1	0 0 1	A'B'C	A + B + C'
:	:	:	:
9	111	ABC	A' + B' + C'

Q: Find minterms and maxterms of f(a, b, c, d) = a'b'.

A: Since 4 inputs, $2^4 = 16$ possible outputs.

$$\begin{aligned} \text{minterms} &= a'b' \underbrace{(c+c')(d+d')}_{\text{equals 1}} \\ &= \underbrace{a'b'cd}_{0011} + \underbrace{a'b'cd'}_{0010} + \underbrace{a'b'c'd}_{0001} + \underbrace{a'b'c'd'}_{0000} \\ &= \sum m(0,1,2,3) \\ \text{maxterms} &= \prod M(4,5,\dots,15) \end{aligned}$$

If
$$f = \sum m(3, 4, 5, 6, 7)$$
,

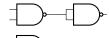
- Maxterm expansion of f is $\prod M(0,1,2)$.
- Minterm expansion of f' is $\sum m(0,1,2)$.
- Maxterm expansion of f' is $\prod M(3,4,5,6,7)$.

NAND as a Universal Gate

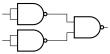
NAND as NOT



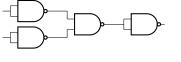
NAND as AND



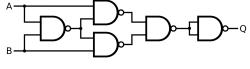
NAND as OR

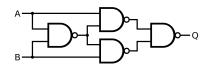


NAND as NOR



NAND as XNOR

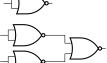




NAND as XOR

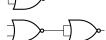
NOR as a Universal Gate

NOR as NOT

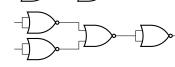


NOR as AND

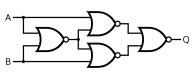
NOR as OR



NOR as NAND



NOR as XNOR





NOR as XOR

Miscellaneous Concepts



Transistor count

- NOT: 2
- NAND, NOR: $2 \times inputs$
- AND = NAND + NOT
- AND, OR: $2 \times \text{inputs} + 2$
- OR = NOR + NOT

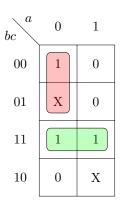
Min transistor count: $2 \times \text{inputs} + 2 \times \text{inverters}$

Karnaugh Maps

Implicant: groups of 1s on map in powers of 2 and is rectangular.

Prime implicant: largest possible implicant.

Essential prime implicant: prime implicant that contains at least 1 term not covered by another prime implicant (can overlap).

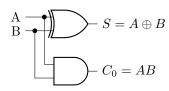


$$f = \sum m(0,3,7) + d(1,6) = a'b' + bc$$

= $\prod M(2,4,5) + d(1,6) = (a'+b)(b'+c)$

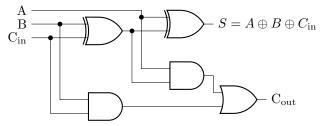
Adders and Subtractors

 $Half\ Adder$



Α	В	S	C_0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

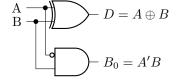
Full Adder



$$C_{\text{out}} = AB + AC_{\text{in}} + BC_{\text{in}} = AB + C_{\text{in}}(A \oplus B)$$

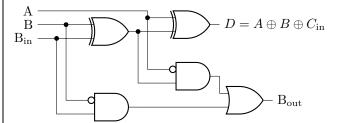
A	В	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

 ${\it Half-Subtractor}$



A	В	D	B_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

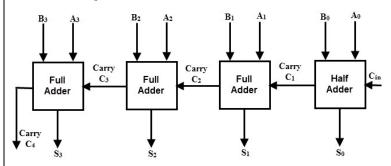
 $Full\ Subtractor$



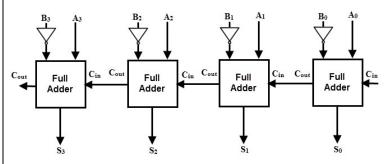
 $B_{\rm out} = A'B + A'B_{\rm in} + BB_{\rm in}$

A	В	$\mathrm{B_{in}}$	D	$\mathrm{B}_{\mathrm{out}}$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Parallel Binary Adder

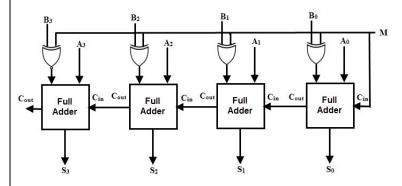


Parallel Binary Subtractor



Adder and Subtractor

M is control bit. If subtracting, M adds 1 and inverts all B bits. If adding, M is 0 (i.e., does nothing).



Design of Multi-Level NAND- and NOR-Gate Circuits

- 1. Design multi-lvl circuit w/ AND and OR gates.
 - Output must be an OR gate.
 - Each lvl must alternate btw AND and OR.
- 2. Number all lvls w/ output as lvl 1. Replace all gates w/ NAND gates.
 - Leave inputs to even lvls unchanged.
 - \bullet Invert literal inputs to odd lvls.

Procedure for NOR same except (i) output is AND and (ii) all gates replaced $\rm w/\ NOR\ gates.$