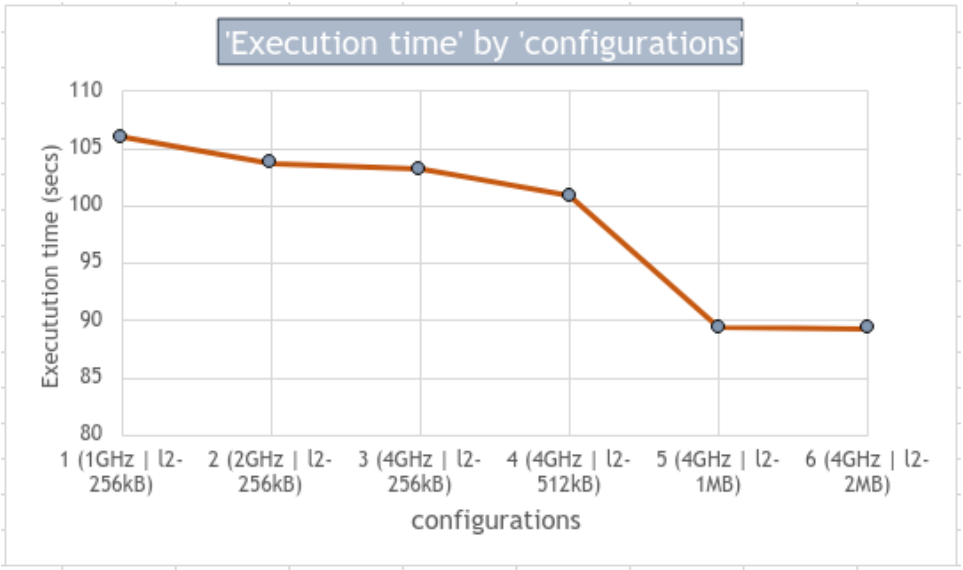
EECS 700 HW 1 SUBMISSION

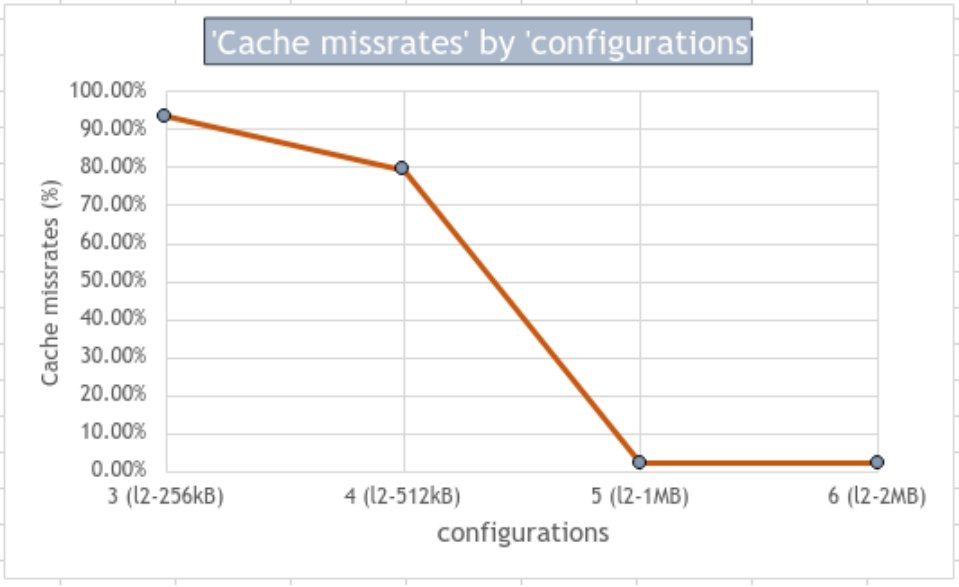
Name: Johnson Umeike

Student ID: 3094849

1. Considering plot 1, we see that execution time is affected by the changing processor clock frequency and l2 cache size. For instance, there is a consistent drop in the execution time from 105.99 secs to 103.23 secs are we move the clock frequency from 1GHz to 4GHz, even with the same l1i, l1d, and l2 configurations. Similarly, execution time changed from 103.23 secs to 89.35 secs as we kept CPU clock frequency constant with decreasing l2 cache size.



2. Considering plot 2, we see a decrease in cache miss rate as we increase the l2 cache size. This is because a larger cache footprint can hold more blocks of data, hence, exploiting the benefits of spatial locality. There is a drastic drop in cache miss rate from config 4 to 5, and not so much change is observed from 5 to 6 meaning temporal locality has kicked in and CPU data movement instructions are accessing the same address space.



3. The working set size of this program is between 512kB and 1MB as we see from the graph. For l2 cache size less than 512kB, miss rate is greater 90% which implies that the processor's data movement instructions still try to access the main memory for unique addresses. However, we see a reduction in the miss rate from config 4 to config 5. At an l2 cache size of 1MB, the miss rate is about 2%, implying that most data elements at unique memory address spaces can fit into the 1MB l2 cache size.