2018-MS-EE-37

Verification Report

AHB Slave

Introduction to the Device-Under-Test (DUT)

Design-Under-Test is the Advanced Microcontroller Bus Architecture (AMBA) Advance High performance Bus (AHB) interface between masters and slaves. Its features like wide data bus and burst transfers allow high performance systems with high clock frequency. AHB Slave (Core-1) receives 32-bit Write Data bus and Read Data bus with 32 bit Address Bus. It supports 4 transfer types decided by HTRANS. This protocol can support single transfer, incremental burst transfer and wrapped burst transfer depending on the control signal HBURST and HSIZE. This DUT can handle multiple slaves, their selection depending on higher order bits of Address using decoder. Output back to Master is controlled via multiplexor. Slave gives output of HREADY and HRESP to show the transfer status.

Verification Plan

No.	Feature	Test Description	Ref.	Type	Result	Comments	Stimulus
1	Reset	Assert reset. During reset all masters must ensure the address and control signals are at valid levels and that HTRANS [1:0] indicates IDLE. During reset all slaves must ensure that HREADYOUT is HIGH	ARM® AMBA® 5 AHB Protocol Specification/ Sec. 7.1.2	T		All signals values are according to the test description	Direct
2	One Write, and then IDLE/ One Read, and then IDLE	Perform one write operation, and then IDLE/ read operation and then IDLE	ARM® AMBA® 5 AHB Protocol Specification/ Sec.3.1	T		Transitions are working fine according to test case	Direct
3	Write and read to a particular memory location	Perform write to any memory location, read from the same memory location, read data should be the same as written data	ARM® AMBA® 5 AHB Protocol Specification/ Sec.3.1	T		Read data is the same as written data on corresponding address locations	Direct
4	Write and read to all memory locations	Perform write and read to all the memory locations. Write to all and then Read from all locations	ARM® AMBA® 5 AHB Protocol Specification/ Sec.3.5	T		Read data is the same as written data on all address locations	Direct

5	Address and Data randomized	Random data would be written on random memory address and randomly write or read back from the same address for comparison.	ARM® AMBA® 5 AHB Protocol Specification/ Sec.3.1/3.5	T		The written data and the read data where same	Random
6	Randomize data only	Random data would be written on particular memory address and read back from the same address for comparison.	ARM® AMBA® 5 AHB Protocol Specification/ Sec.3.1/3.5	T		Random data was written on particular memory location. The same data is read, and the result was same	Random
7	Randomize address only	Data would be written on random memory address and read back from the same address for comparison	ARM® AMBA® 5 AHB Protocol Specification/ Sec.3.1/3.5	T		Data was written on random addresses and then read. The written and read was same.	Random
8	Address out of range	Data would be written on memory location which is out of range of the given design. It should create an Error.	ARM® AMBA® 5 AHB Specification/ Sec.1.3/2.2	T		Address is out of range and an Error end of the execution	Direct

9	Different Size of Data Transfer Depending on HSIZE [2:0] (With in word limit i.e., 32 bits)	Data (Word/Half word/Byte) would be written and read based on HSIZE on different memory locations. The written data and read data should be same	ARM® AMBA® 5 AHB Protocol Specification/ Sec.2.2/3.4	T		Word/Halfword/ Bytes were written and then read. The read data was same as written	Direct
10	Writing Byte and reading Halfword and Word	Writing the Byte on a memory location and then reading Halfword format and Word format.	ARM® AMBA® 5 AHB Protocol Specification/ Sec.2.2/3.4	T		Read data is not of byte format	Direct
11	Different Size of Data Transfer Depending on HSIZE [2:0] (Greater than the word limit i.e. 32 bits)	Data (Double Word/ 4-word line/ 8- word line) would be written and read based on HSIZE on different memory locations. An error should be generated since data is out of range from the given design.	ARM® AMBA® 5 AHB Protocol Specification/ Sec.2.2/3.4	T		Test is failed for the given design because data width is greater than the data width of the given design	Direct

12	Write and read when HSELx is low	When HSELx is low, no write and read operation in the slave core 1.	ARM® AMBA® 5 AHB Protocol Specification/ Sec.2.4/4.2	T		When HSELx is 0 or 1 slave responds back.	Direct
13	Random data generation in a specific range	Random data having specific range will be written on all memory locations and then will be read.	ARM® AMBA® 5 AHB Protocol Specification/ Sec.2.2-2.4/6.1	T		Random data was written and then read. The written data and read data were the same	Random
14	Random Address generation in specific range	Data would be written on random address having value in a specific range	ARM® AMBA® 5 AHB Protocol Specification/ Sec.2.2-2.4/6.1	T		Address is out of range and an Error is generated at the end of the execution	Random
15	BURST operation with HBURST and HSIZE selection	Data in BURST format i.e., INCR4, HSIZE byte, INCR4, HSIZE halfword, to HUBRST INCR16, HSIZE doubleword will be written and then read	ARM® AMBA® 5 AHB Protocol Specification/ Sec.3.5	T		BURST operation is not supported by the design	Direct
16	Randomize all	All fields with rand data type in transaction will be randomized and response of the design will be checked.	ARM® AMBA® 5 AHB Protocol Specification/ sec 3.1/sec 3.5	T		The given fields with rand data type was randomized. Data read was found to be same as written data.	Random

17	Error sequence	Error sequence should comprise of two cycles, HREADY will be low for first cycle and then will be high in second cycle	ARM® AMBA® 5 AHB Protocol Specification/ sec 3.6.2	A		Error sequence remained for two cycles as per design specifications	--
18	Transfer Data size	The values for HSIZE should be between 3'b000 and 3'b010.	ARM® AMBA® 5 AHB Protocol Specification/ sec 3.4	A		HSIZE exceeded the given range	--
19	BURST operation	During the BURST transfer either, INCR or WRAP, HISZE and HBURST should remain same.	ARM® AMBA® 5 AHB Protocol Specification/ sec 3.5	A		During BURST transfer, HSIZE remained same	--
20	Transfer Type Constant	When HREADY signal is low, HTRANS should be kept constant by the master. There is an exception for this one in BUSY or IDLE Transfer	ARM® AMBA® 5 AHB Protocol Specification/ sec 3.6.1	A		When HREADY was low, HTRANS remained constant	--
21	Address Constant when slave is not ready	During the phase when HTRANS transfer type is changed to NONSEQ i.e. 2'b10, the address should remain constant when HREADY is low	ARM® AMBA® 5 AHB Protocol Specification/ sec 3.6.1	A		When HREADY was low, Address remained constant	--

Explanation of Different Fields

No.	The serial number of the test.
Feature	The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.
Test Description	A detailed description of the test case being performed. You can be as verbose as you want.
Ref.	Reference to the section in the related standard document. The section number as well as page numbers should be described here.
Type	Type of the test. Whether the test is an assertion (A) or a transaction (T) type.
Result	Pass (P) or Fail (F).
Comments	Any other comments about the test or its results that you want to mention.
Coverage	Code or Functional
Stimulus	Mention the kind of stimulus give. i.e directed system verilog