2018-MS-EE-37

Verification Report

AHB Slave

Introduction to the Device-Under-Test (DUT)

*Design-Under-Test is the Advanced Microcontroller Bus Architecture (AMBA) Advance High performance Bus (AHB) interface between masters and slaves. Its features like wide data bus and burst transfers allow high performance systems with high clock frequency. AHB Slave (Core-1) receives 32-bit Write Data bus and Read Data bus with 32 bit Address Bus. It supports 4 transfer types decided by HTRANS. This protocol can support single transfer, incremental burst transfer and wrapped burst transfer depending on the control signal HBURST and HSIZE. This DUT can handle multiple slaves, their selection depending on higher order bits of Address using decoder. Output back to Master is controlled via multiplexor. Slave gives output of HREADY and HRESP to show the transfer status.*

3

Verification Plan

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **No.** | **Feature** | **Test Description** | **Ref.** | **Type** | **Result** | **Comments** | **Stimulus** |  |
|  |  |  |  |  |  |  |  |  |
| 1 | Reset | Assert reset. During reset all masters must | ARM® AMBA® 5 AHB |  |  | All signals values |  |  |
|  |  | ensure the address and control signals are at | Protocol |  |  | are according to |  |  |
|  |  | valid levels and that HTRANS [1:0] indicates | Specification/ Sec. | T |  | the test description | Direct |  |
|  |  | IDLE. | 7.1.2 |  |  |
|  |  |  |  |  |  |  |
|  |  | During reset all slaves must ensure that |  |  |  |  |  |  |
|  |  | HREADYOUT is HIGH |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 2 | One Write, and | Perform one write operation, and then IDLE/ | ARM® AMBA® 5 AHB |  |  | Transitions are |  |  |
|  | then IDLE/ One | read operation and then IDLE | Protocol | T |  | working fine | Direct |  |
|  | Read, and then |  | Specification/ Sec.3.1 | according to test |  |
|  |  |  |  |  |  |
|  | IDLE |  |  |  |  | case |  |  |
|  |  |  |  |  |  |  |  |  |
| 3 | Write and read to | Perform write to any memory location, read | ARM® AMBA® 5 AHB |  |  | Read data is the |  |  |
|  | a particular | from the same memory location, read data | Protocol |  |  | same as written |  |  |
|  | memory location | should be the same as written data | Specification/ Sec.3.1 | T |  | data on | Direct |  |
|  |  |  |  |  |  | corresponding |  |  |
|  |  |  |  |  |  | address locations |  |  |
|  |  |  |  |  |  |  |  |  |
| 4 | Write and read to | Perform write and read to all the memory | ARM® AMBA® 5 AHB |  |  | Read data is the |  |  |
|  | all memory | locations. Write to all and then Read from all | Protocol | T |  | same as written | Direct |  |
|  | locations | locations | Specification/ Sec.3.5 | data on all address |  |
|  |  |  |  |  |
|  |  |  |  |  |  | locations |  |  |
|  |  |  |  |  |  |  |  |  |

1

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |
| 5 | Address and Data | Random data would be written on random | ARM® AMBA® 5 AHB |  |  | The written data |  |  |
|  | randomized | memory address and randomly write or read | Protocol | T |  | and the read data | Random |  |
|  |  | back from the same address for comparison. | Specification/ | where same |  |
|  |  |  |  |  |  |
|  |  |  | Sec.3.1/3.5 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 6 | Randomize data | Random data would be written on particular | ARM® AMBA® 5 AHB |  |  | Random data was |  |  |
|  | only | memory address and read back from the | Protocol |  |  | written on |  |  |
|  |  | same address for comparison. | Specification/ |  |  | particular memory |  |  |
|  |  |  | Sec.3.1/3.5 | T |  | location. The same | Random |  |
|  |  |  |  |  |  | data is read, and |  |  |
|  |  |  |  |  |  | the result was |  |  |
|  |  |  |  |  |  | same |  |  |
|  |  |  |  |  |  |  |  |  |
| 7 | Randomize | Data would be written on random memory | ARM® AMBA® 5 AHB |  |  | Data was written |  |  |
|  | address only | address and read back from the same | Protocol |  |  | on random |  |  |
|  |  | address for comparison | Specification/ | T |  | addresses and then | Random |  |
|  |  |  | Sec.3.1/3.5 | read. The written |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  | and read was |  |  |
|  |  |  |  |  |  | same. |  |  |
|  |  |  |  |  |  |  |  |  |
| 8 | Address out of | Data would be written on memory location | ARM® AMBA® 5 AHB |  |  | Address is out of |  |  |
|  | range | which is out of range of the given design. It | Specification/ | T |  | range and an Error | Direct |  |
|  |  | should create an Error. | Sec.1.3/2.2 |  |  | end of the |  |  |
|  |  |  |  |  |  | execution |  |  |

2

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |
| 9 | Different Size of | Data (Word/Half word/Byte) would be | ARM® AMBA® 5 AHB |  |  | Word/Halfword/ |  |  |
|  | Data Transfer | written and read based on HSIZE on different | Protocol |  |  | Bytes were written |  |  |
|  | Depending on | memory locations. The written data and | Specification/ | T |  | and then read. The | Direct |  |
|  | HSIZE [2:0] (With | read data should be same | Sec.2.2/3.4 | read data was |  |
|  |  |  |  |  |
|  | in word limit i.e., |  |  |  |  | same as written |  |  |
|  | 32 bits) |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 10 | Writing Byte and | Writing the Byte on a memory location and | ARM® AMBA® 5 AHB |  |  | Read data is not of |  |  |
|  | reading Halfword | then reading Halfword format and Word | Protocol | T |  | byte format | Direct |  |
|  | and Word | format. | Specification/ |  |  |
|  |  |  |  |  |  |
|  |  |  | Sec.2.2/3.4 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 11 | Different Size of | Data (Double Word/ 4-word line/ 8- word | ARM® AMBA® 5 AHB |  |  | Test is failed for |  |  |
|  | Data Transfer | line) would be written and read based on | Protocol |  |  | the given design |  |  |
|  | Depending on | HSIZE on different memory locations. An | Specification/ |  |  | because data |  |  |
|  | HSIZE [2:0] | error should be generated since data is out | Sec.2.2/3.4 | T |  | width is greater | Direct |  |
|  | (Greater than the | of range from the given design. |  |  |  | than the data |  |  |
|  | word limit i.e. 32 |  |  |  |  | width of the given |  |  |
|  | bits) |  |  |  |  | design |  |  |
|  |  |  |  |  |  |  |  |  |

3



|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 12 | Write and read | When HSELx is low, no write and read | ARM® AMBA® 5 AHB |  |  | When HSELx is 0 or |  |  |
|  | when HSELx is low | operation in the slave core 1. | Protocol | T |  | 1 slave responds | Direct |  |
|  |  |  | Specification/ | back. |  |
|  |  |  |  |  |  |  |
|  |  |  | Sec.2.4/4.2 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 13 | Random data | Random data having specific range will be | ARM® AMBA® 5 AHB |  |  | Random data was |  |  |
|  | generation in a | written on all memory locations and then | Protocol |  |  | written and then |  |  |
|  | specific range | will be read. | Specification/ Sec.2.2- | T |  | read. The written | Random |  |
|  |  |  | 2.4/6.1 |  |  | data and read data |  |  |
|  |  |  |  |  |  | were the same |  |  |
|  |  |  |  |  |  |  |  |  |
| 14 | Random Address | Data would be written on random address | ARM® AMBA® 5 AHB |  |  | Address is out of |  |  |
|  | generation in | having value in a specific range | Protocol |  |  | range and an Error |  |  |
|  | specific range |  | Specification/ Sec.2.2- | T |  | is generated at the | Random |  |
|  |  |  | 2.4/6.1 |  |  | end of the |  |  |
|  |  |  |  |  |  | execution |  |  |
|  |  |  |  |  |  |  |  |  |
| 15 | BURST operation | Data in BURST format i.e., INCR4, HSIZE byte, | ARM® AMBA® 5 AHB |  |  | BURST operation is |  |  |
|  | with HBURST and | INCR4, HSIZE halfword, to HUBRST INCR16, | Protocol | T |  | not supported by | Direct |  |
|  | HSIZE selection | HSIZE doubleword will be written and then | Specification/ Sec.3.5 | the design |  |
|  |  |  |  |  |
|  |  | read |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 16 | Randomize all | All fields with rand data type in transaction | ARM® AMBA® 5 AHB |  |  | The given fields |  |  |
|  |  | will be randomized and response of the | Protocol |  |  | with rand data |  |  |
|  |  | design will be checked. | Specification/ sec |  |  | type was |  |  |
|  |  |  | 3.1/sec 3.5 | T |  | randomized. Data | Random |  |
|  |  |  |  |  |  | read was found to |  |  |
|  |  |  |  |  |  | be same as written |  |  |
|  |  |  |  |  |  | data. |  |  |
|  |  |  |  |  |  |  |  |  |

4

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |
| 17 | Error sequence | Error sequence should comprise of two | ARM® AMBA® 5 AHB |  |  | Error sequence |  |  |
|  |  | cycles, HREADY will be low for first cycle and | Protocol |  |  | remained for two |  |  |
|  |  | then will be high in second cycle | Specification/ sec | A |  | cycles as per | -- |  |
|  |  |  | 3.6.2 |  |  | design |  |  |
|  |  |  |  |  |  | specifications |  |  |
|  |  |  |  |  |  |  |  |  |
| 18 | Transfer Data size | The values for HSIZE should be between | ARM® AMBA® 5 AHB |  |  | HSIZE exceeded |  |  |
|  |  | 3’b000 and 3’b010. | Protocol | A |  | the given range | -- |  |
|  |  |  | Specification/ sec 3.4 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 19 | BURST operation | During the BURST transfer either, INCR or | ARM® AMBA® 5 AHB |  |  | During BURST |  |  |
|  |  | WRAP, HISZE and HBURST should remain | Protocol | A |  | transfer, HSIZE | -- |  |
|  |  | same. | Specification/ sec 3.5 |  |  | remained same |  |  |
|  |  |  |  |  |  |  |  |  |
| 20 | Transfer Type | When HREADY signal is low, HTRANS should | ARM® AMBA® 5 AHB |  |  | When HREADY was |  |  |
|  | Constant | be kept constant by the master. There is an | Protocol | A |  | low, HTRANS | -- |  |
|  |  | exception for this one in BUSY or IDLE Transfer | Specification/ sec | remained constant |  |
|  |  |  |  |  |  |
|  |  |  | 3.6.1 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 21 | Address Constant | During the phase when HTRANS transfer | ARM® AMBA® 5 AHB |  |  | When HREADY was |  |  |
|  | when slave is not | type is changed to NONSEQ i.e. 2’b10, the | Protocol | A |  | low, Address | -- |  |
|  | ready | address should remain constant when | Specification/ sec | remained constant |  |
|  |  |  |  |  |
|  |  | HREADY is low | 3.6.1 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |

5

Explanation of Different Fields

**No.**

**Feature**

**Test Description**

**Ref.**

**Type**

**Result**

**Comments**

**Coverage**

**Stimulus**

The serial number of the test.

The feature which the current test is verifying in full or partially.

The feature is usually on the abstraction level of a user.

A detailed description of the test case being performed.

You can be as verbose as you want.

Reference to the section in the related standard document.

The section number as well as page numbers should be described here.

Type of the test. Whether the test is an assertion (A) or a transaction (T) type.

Pass (P) or Fail (F).

Any other comments about the test or its results that you want to mention.

Code or Functional

Mention the kind of stimulus give. i.e directed system verilog

6