VLSI Physical Design Project

Implementation Documentation

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Tools used:

Synthesis: **Synopsys Design Compiler(DC),**
Place & Route:**Synopsys ICC2**

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1. Block Details

Block Name: Tile
No. of ports:1635

a. Input ports -838
b. Output ports - 797
c. Inout ports –

No. of macros: 18
No. of clocks: 1
Die size: 1396 um x 1076 um
Die Area: 1.50um^2

Initial core utilization: 0.7 (70%)

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2. Design Specifications

2.1 Technology info:

Technology node:28nm

Standard cell height:0.9 um

Standard cell VT types: SVT, HVT, LVT.

2.2 Clock Specifications

Clock name	Clock period	Master/Generated clock	Sinks
clk	**1.7ns**	**Master**	**99071**

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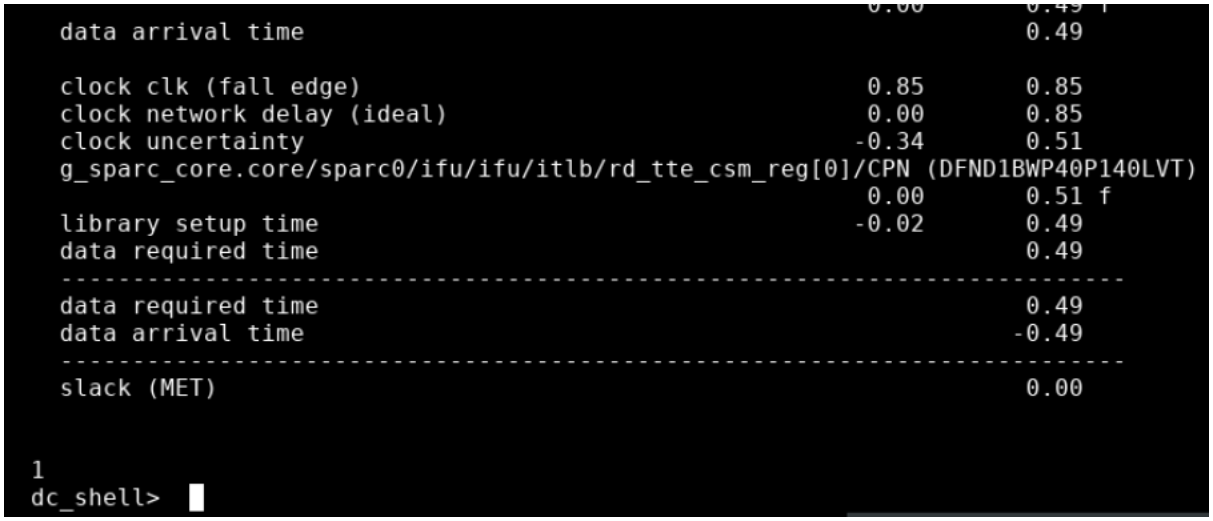
3. Implementation Metrics & Checklist

3.1 Synthesis Stage Metrics

Metric	Value	Unit
RTL files loaded successfully without errors	Successfully read into Design Compiler without any syntax or compilation errors	Pass
Elaborate finished without any errors	RTL hierarchy, module instantiations, and parameter resolutions are correct.	Pass
SDC file applied without any errors	Timing and design constraints defined in the SDC file were applied without any errors.	Pass
No errors in log file	The synthesis log file was reviewed and found to be free of critical errors	Pass
Applied don't use for LVT, CK*, High drive strength cells	Don't-use constraints were applied to LVT, clock-specific, and high drive strength cells	Pass
Gate-level netlist generated	synthesized design mapped to the target standard-cell library.	Pass
Synthesis reports generated	reports including timing, area, and power were generated to analyze design	Pass
Total Cell Area	1.02	μm^2
Combinational Area	0.18	μm^2
Sequential Area	0.19	μm^2
Macro area	0.63	μm^2
Total Cells	413935	count
Sequential Cells	101188	count

Combinational Cells	312709	count
Buf/Inv Cells	3054+46118	count
Worst Setup Slack (WNS)	-0.11(r2o)	ns
Total Negative Slack (TNS)	-81.21(r2o)	ns
No. of Violating paths	2458(r2o)	Count
Total Power	383.06	mW
Check timing issues	Minor setup timing violations are observed on register-to-output (r2o) paths with WNS of –0.11 ns and TNS of –81.21 ns,and Vp=2458	Not clean
Check design issues	No structural or logical design issues reported during synthesis checks	Clean

Report_timing for Reg-Reg path:



Report_timing for In-Reg Path:

```
                                                          0.00       1.41 r
data arrival time                                                    1.41

clock clk (rise edge)                                     1.70       1.70
clock network delay (ideal)                               0.00       1.70
clock uncertainty                                        -0.34       1.36
uncore_config/read_data_s3_reg[8]/CP (DFQD1BWP40P140LVT)
                                                          0.00       1.36 r
library setup time                                       -0.02       1.34
data required time                                                   1.34
---------------------------------------------------------------------------
data required time                                                   1.34
data arrival time                                                   -1.41
---------------------------------------------------------------------------
slack (VIOLATED)                                                    -0.07
```

Report_timing for Reg-Out Path:

```
data arrival time                                                    0.28

clock clk (rise edge)                                     1.70       1.70
clock network delay (ideal)                               0.00       1.70
clock uncertainty                                        -0.34       1.36
output external delay                                    -1.19       0.17
data required time                                                   0.17
---------------------------------------------------------------------------
data required time                                                   0.17
data arrival time                                                   -0.28
---------------------------------------------------------------------------
slack (VIOLATED)                                                    -0.11
```

Report_area:

```
Number of ports:                        39071
Number of nets:                        456267
Number of cells:                       415987
Number of combinational cells:         314743
Number of sequential cells:            101170
Number of macros/black boxes:              18
Number of buf/inv:                      49286
Number of references:                     480

Combinational area:             187506.268682
Buf/Inv area:                    13650.336151
Noncombinational area:          199080.249753
Macro/Black Box area:           635583.927734
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:               1022170.446169
Total area:                 undefined
1
dc_shell>
```

Conclusion:

Synthesis completed successfully with clean r2r timing and no design issues. Minor i2r and r2o setup violations due to ideal synthesis assumptions are acceptable at this stage. Latch-based endpoints in `check_timing` are non-critical, and the design is ready for PNR.

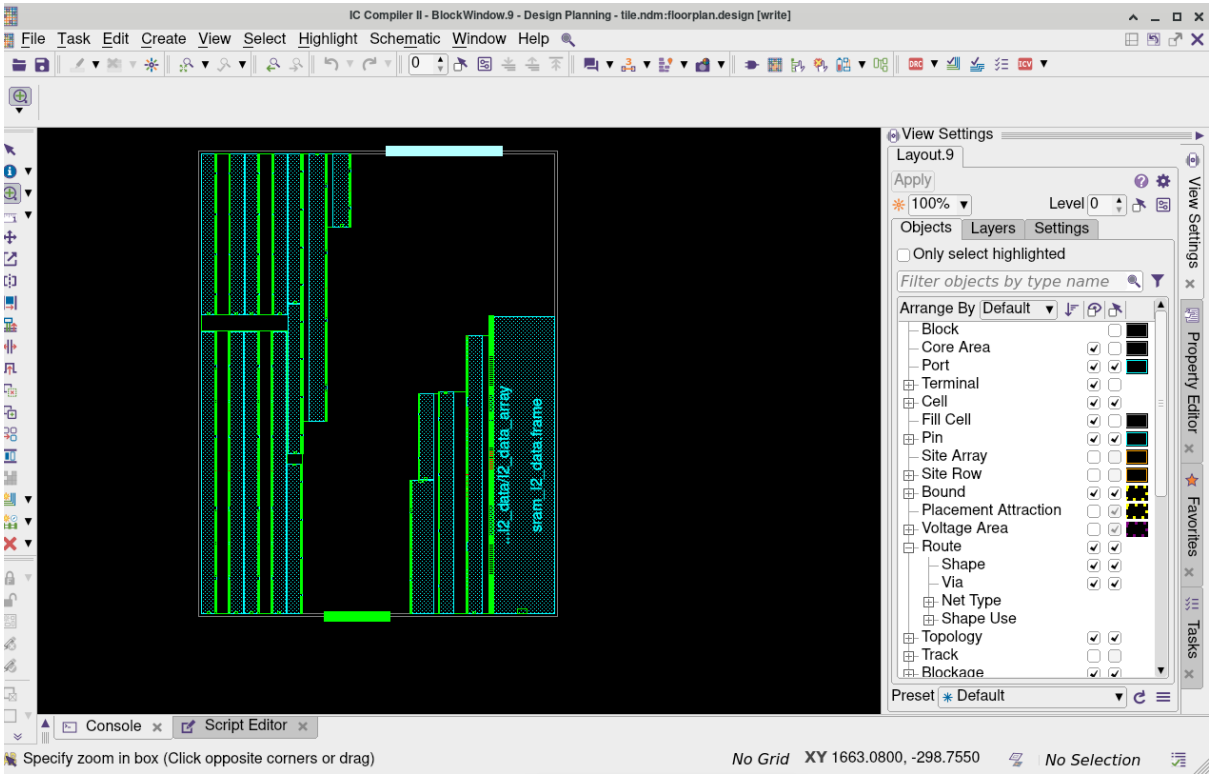
Overall Synthesis Stage: Complete

3.2 Floorplan Stage Metrics

Metric	Value	Unit
Design imported successfully	Netlist, tech LEF, SDC, SRAM NDMs,TLU'S,Pg Script loaded without errors.	Pass
Core area defined with proper utilization (70%)	70 (Chosen to balance routability and timing)	Pass
No linking issues	No unresolved references after design import	Pass
Core Width	1060	µm
Core Height	1380	µm
Core Area	(1,462,800) = 1.4	µm²
Die Width	1076(core width+offsets)	µm
Die Height	1396(core height+offsets)	µm
Die Area	1.50	µm²
Core Utilization	70	%
Core offsets	{8 8 8 8}	µm
Aspect Ratio	1.3(H/W)	
Number of Macros	18	count
Macro Area	635583.93(0.63)	µm²
Ports placed correctly	Ports placed on core boundary without overlaps	Pass
Endcap cell issues	No endcap violations reported	Clean
Tap cell issues	Tap cell insertion clean	Clean
PG opens	0	Count
PG shorts	0	Count
PG connectivity	PG connectivity verified	Clean
PG missing vias	0	Count
Zero interconnect timing (pre place timing)	WNS = -0.03; TNS = -18.81; FEP = 780 report_qor(r20 path getting –ve slack)	Count
Check timing	No timing errors at pre-placement stage	Clean

No errors in logfiles	No errors or fatal warnings in ICC2 logs	Pass
Floorplan Type	Macro-dominant rectangular floorplan	Clean

Figure 1.1: Floorplan View of Tile Block (Post Core Sizing and Macros,ports Placement)



Overall Floorplan Stage: Complete.

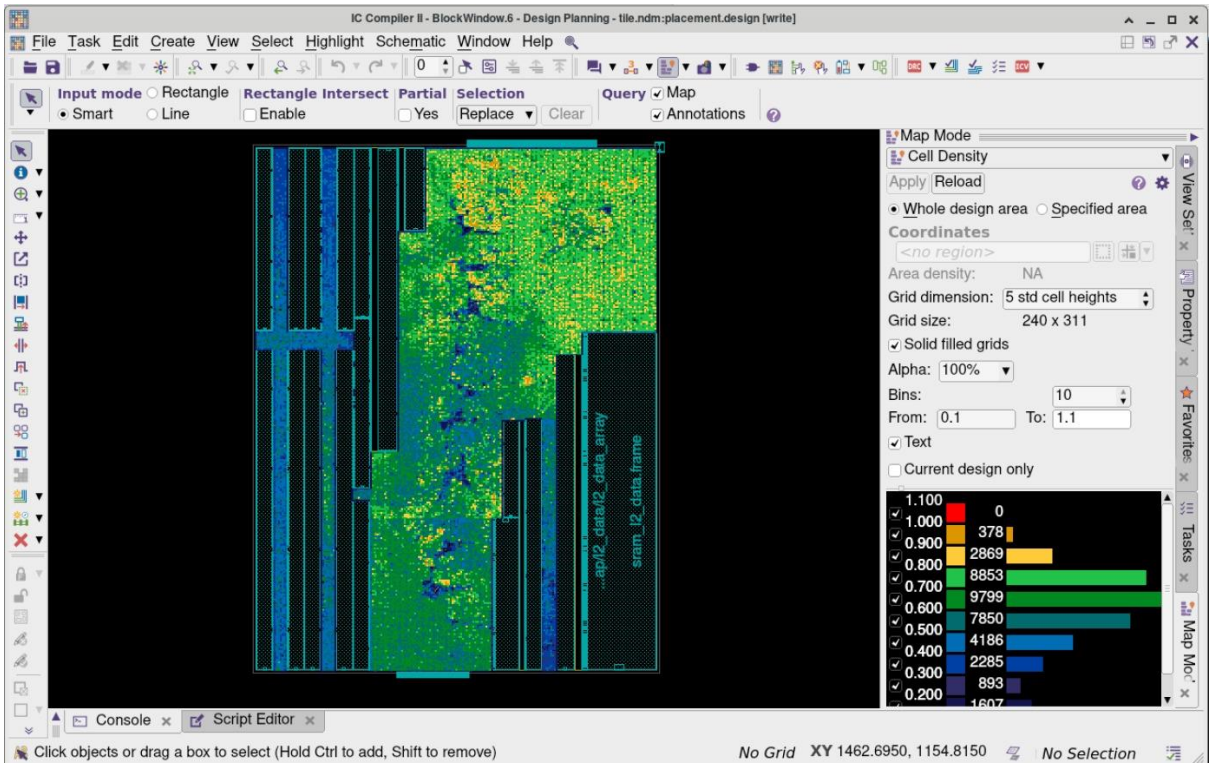
3.3 Placement Stage Metrics

Metric	Value	Unit
core utilization	0.61	%
check_place or check_legality	clean	Clean
Congestion	H(0.18%).., V(1.94%)	H% & V%
Congestion acceptable	yes	Pass
Cell density acceptable	yes	Pass
Setup timing (reg2reg)	-0.24/-10.67/86	WNS/TNS/FEP
Setup timing (in2reg)	-0.32/-175/3847	WNS/TNS/FEP
Setup timing (reg2out)	-0.44/-260.28/784	WNS/TNS/FEP
Setup timing (in2out)	0/0/0	WNS/TNS/FEP

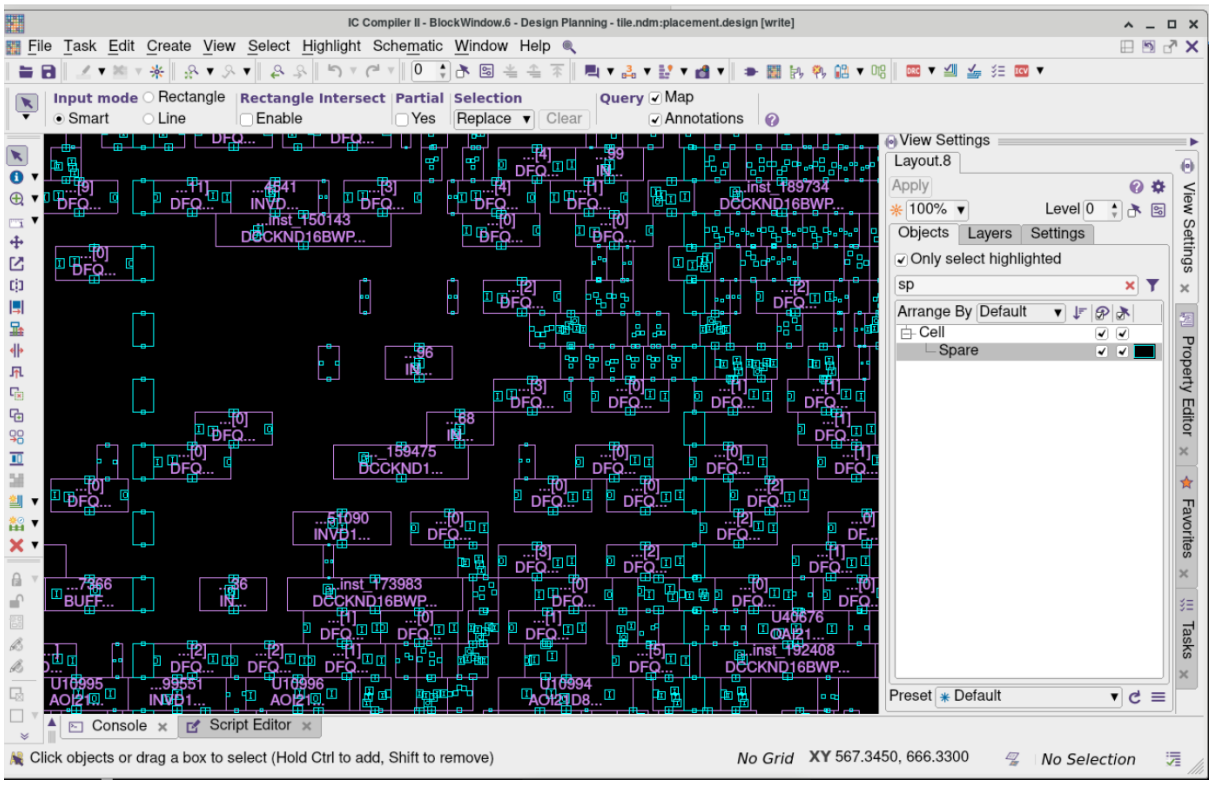
Max transition violations	1	WNS/Count
Max Capacitance violations	7	WNS/Count
Spare cells inserted	yes	Yes
No. of spare cells	1476	Count

Snapshot of cell density, congestion map & spare cell distribution snapshot.

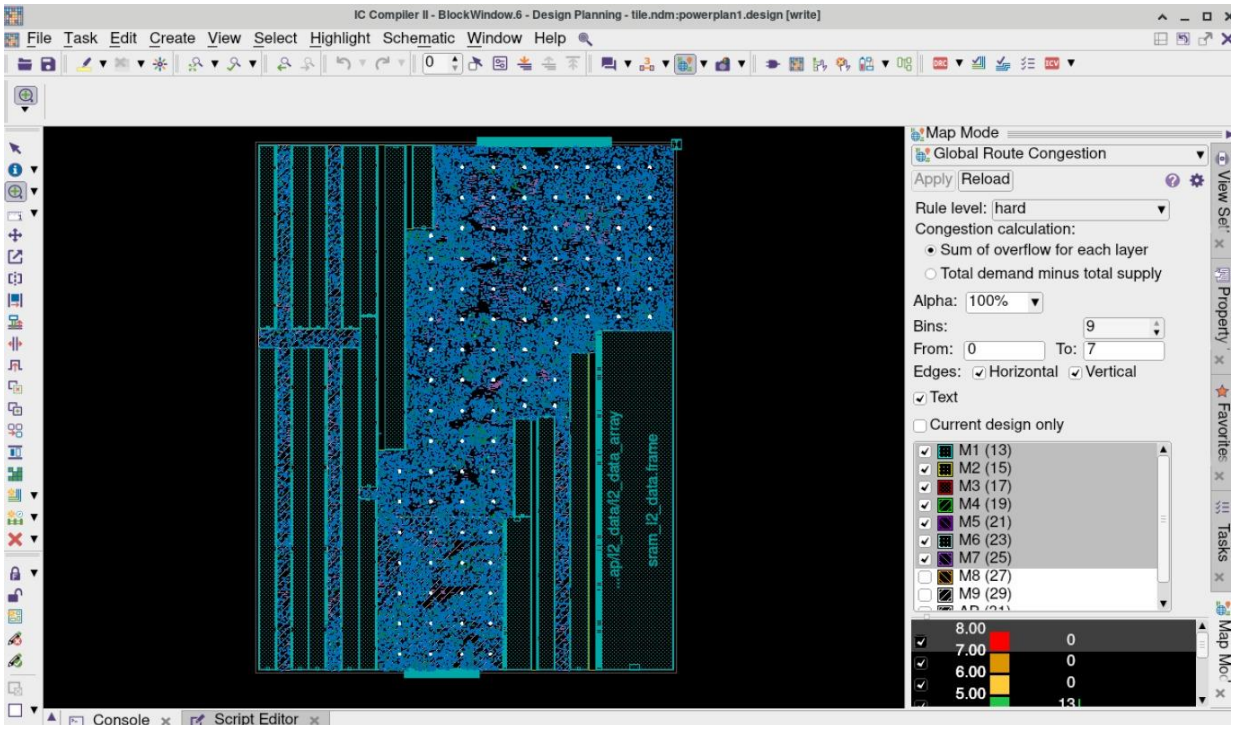
Snapshot of Cell Density:



Snapshot of Spare cell Distubution:



Congestion Map:

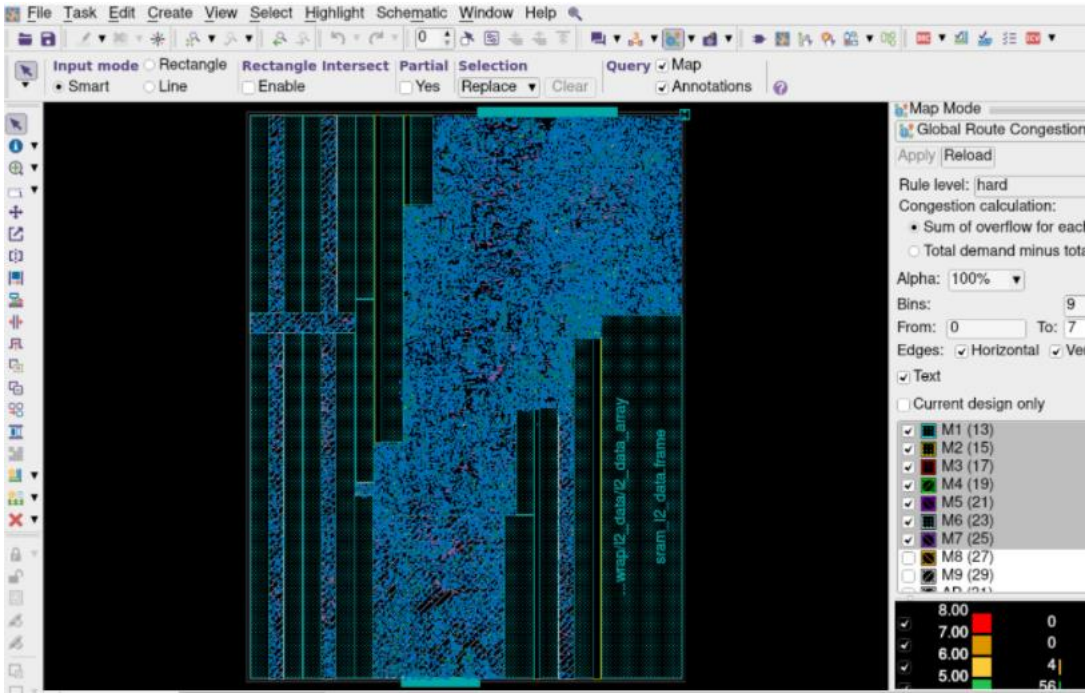


Overall Placement Stage: Complete

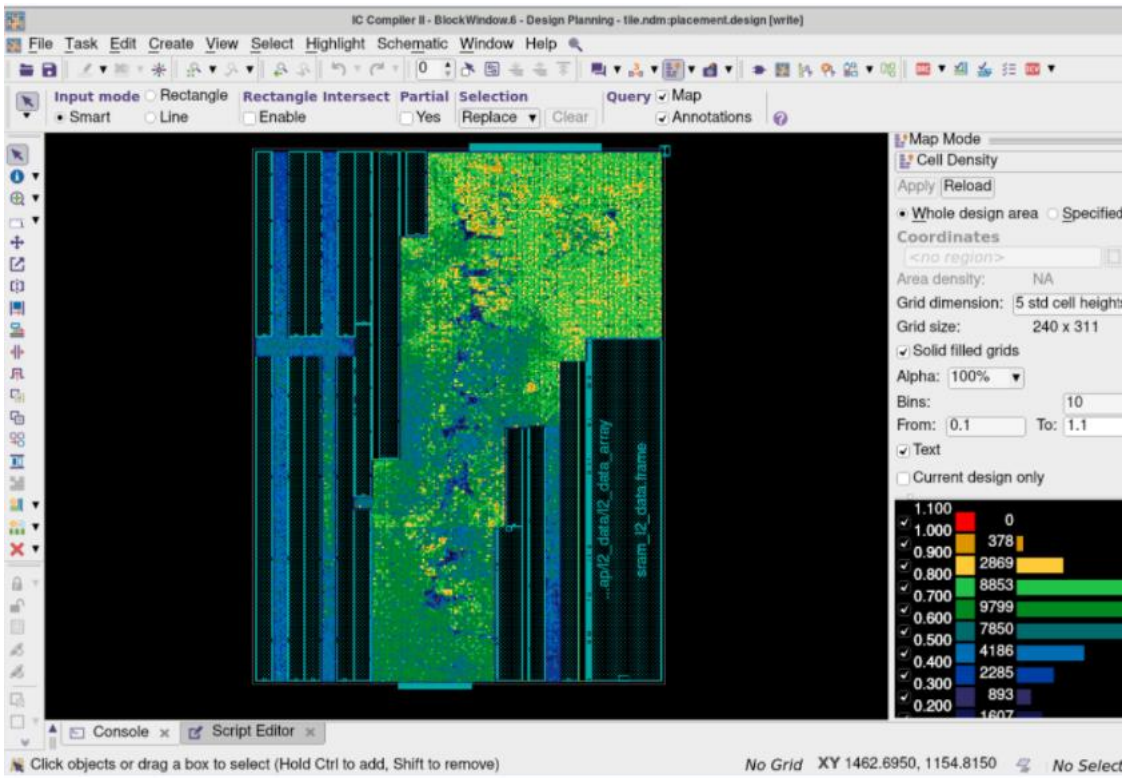
3.4 CTS Stage Metrics (PostCTS)

Metric	Value	Unit
Clock Buffers Inserted	10166	count
Clock Inverters Inserted	163	count
Total Clock Tree Cells	10488	count
Only CK*LVT cells used in clock tree	pass	Pass/Fail
Clock tree reports generated	yes	Yes/No
Clock Tree Area	9886.6	μm^2
Global Skew	0.70	ps
Max Clock Latency	0.93	ps
Clock Transition Limit	2.32	ns
Clock fanout limit	16	count
Setup timing (reg2reg)	-0.32/-46.93/1122	WNS/TNS/FEP
Setup timing (in2reg)	-0.34/-554.73/3834	WNS/TNS/FEP
Setup timing (reg2out)	-0.63/-422.15/797	WNS/TNS/FEP
Setup timing (in2out)	0/0/0	WNS/TNS/FEP
Hold timing (reg2reg)	-0.10/-6.92/328	WNS/TNS/FEP
Max transition violations	26	Count
Max Cap violations	14	Count
Setup uncertainty	0.255	ns
Hold uncertainty	0.05	ns
Clock net DRCs	6	Count
core utilization	0.64(64%)	%
check_place or check_legality	pass	Clean
Congestion	H(0.18%) & V (2.26%)	H% & V% Innovus: Max hotspot score

Snapshot of congestion map.



Snapshot of Cell density:



Overall CTS & PostCTS Stage: Complete

3.5 Routing Stage Metrics

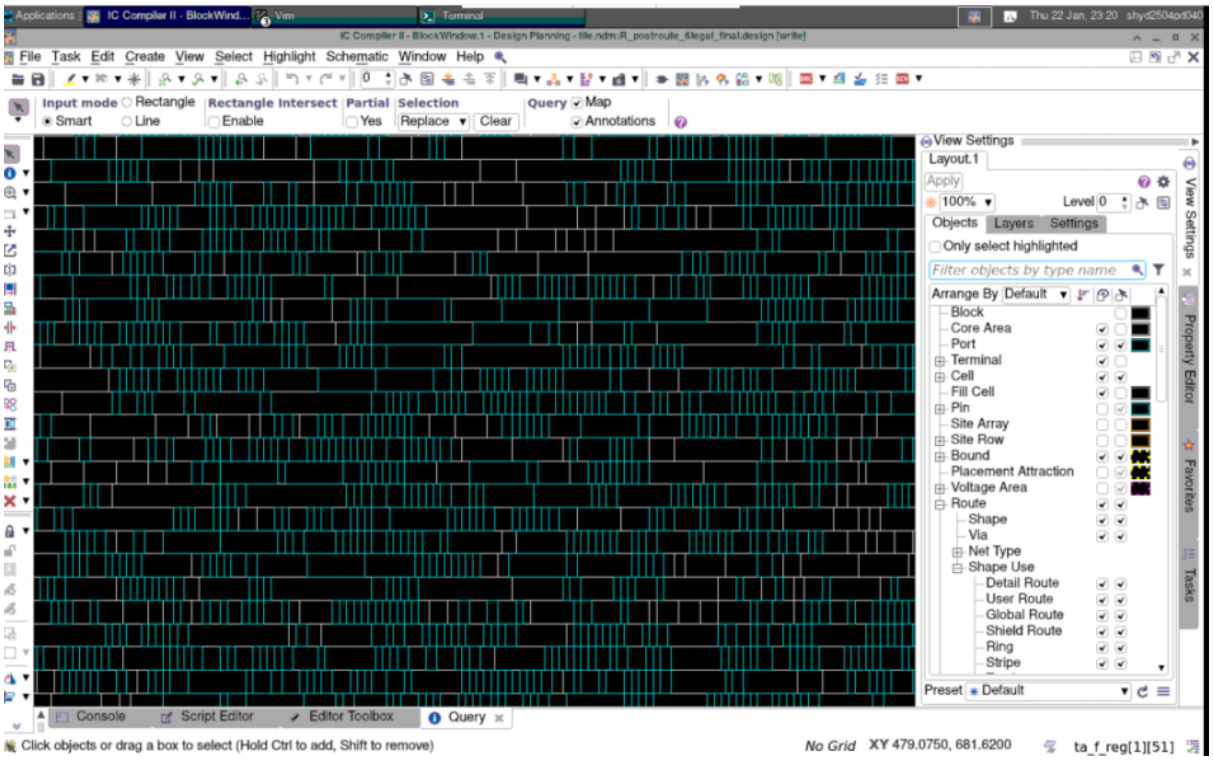
Metric	Value	Unit
Core utilization	80.71	%
DRC violations	0	count
Shorts	0	count
Opens	0	count
Antenna violations	0	count

Overall Route Stage: Complete/Incomplete

3.6 Post-Route Metrics (Final)

Metric	Value	Unit
core utilization	0.80(80.71)	%
check_place or check_legality	clean	Clean/ Not clean
DRC violations	0	count
Shorts	0	count
Opens	0	count
Setup timing (reg2reg)	0/0/0	WNS/TNS/FEP
Setup timing (in2reg)	0/0/0	WNS/TNS/FEP
Setup timing (reg2out)	0.02/0/0	WNS/TNS/FEP
Setup timing (in2out)	NA	WNS/TNS/FEP
Hold timing (reg2reg)	0.28/0/0	WNS/TNS/FEP
Max transition violations	0	WNS/Count
Max Cap violations	0	WNS/Count
Final GDSII generated	Generated (YES)	Yes/No
Final DEF generated	Yes	Yes/No
Final netlist generated	Yes	Yes/No
All signoff reports generated	Yes generated successfully	Yes/No

Snapshot of design with fillers. (Disable all metal layers)



Overall Post-Route Stage: Complete

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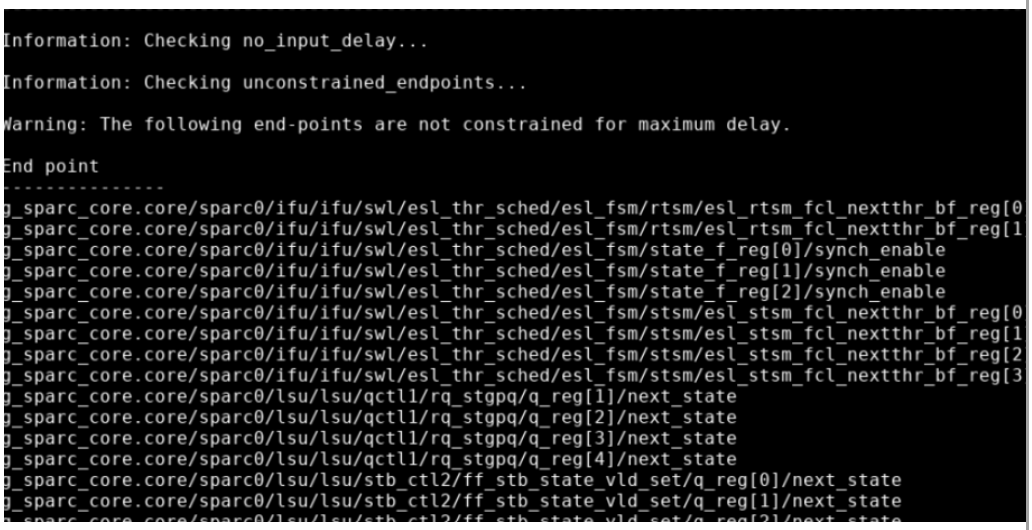
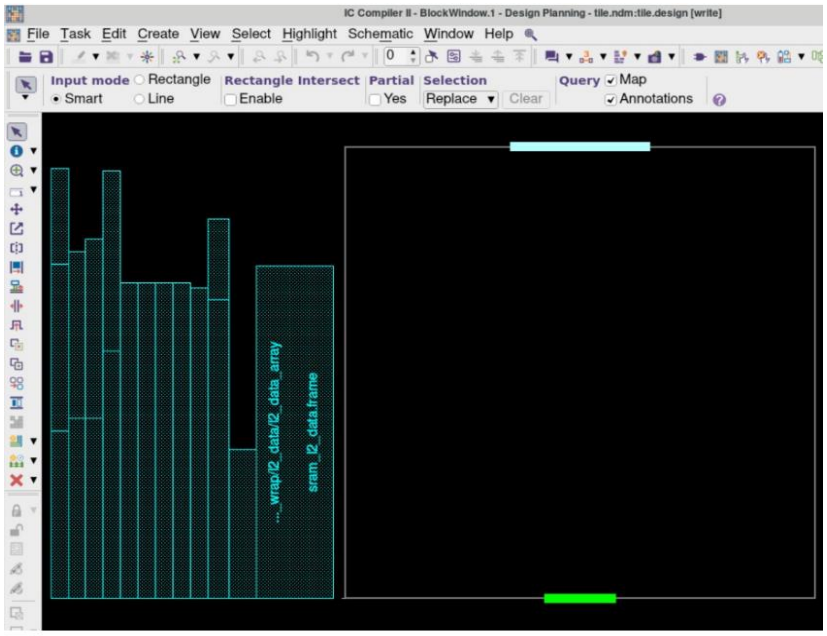
4. Issues and Fixes

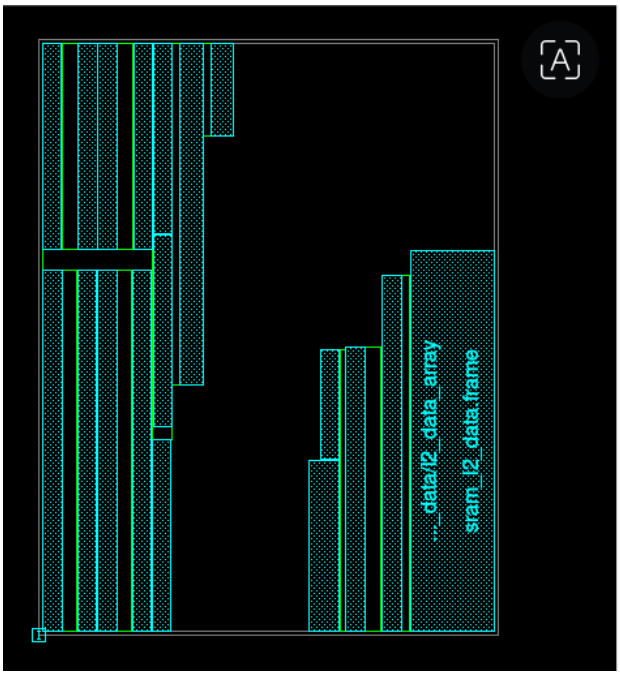
Issue #1

Field	Details
Issue Title	Unconstrained Endpoints
Design Stage	Synthesis
Issue Category	Timing
Tool	DC_tool
Severity	Low

Issue Description	In check_timing there is uncontrained end points (no clock specified to that particular end points)
Error Message/Log	
Root Cause Analysis	After checking reports for one of the end points I came to know that it is a latch based path so we can ignore those end points as there is no need to do timing to those paths.so I decided to proceed to compile stage
Debug Steps Followed	Step1:identified problem(unconstrained end points) Step2:extracted one end point and check whether what type of cell it is using report_cell command Step3:observed it is a latch based end point Step4:decided to move further by ignoring these latch based unconstrained end points.
Solution Applied	Followed above steps and analysed the issue
Result After Fix	After compile these end points are disappeared as they not belong to flob based end points .in check_timing there is no issue now

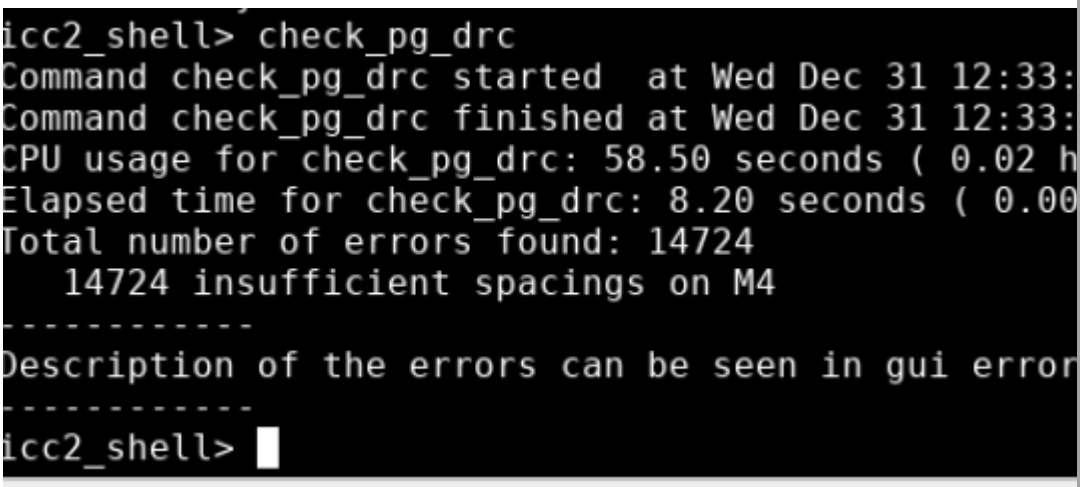
Issue #2

Field	Details
Issue Title	Floorplan core area setting issue
Design Stage	Floorplan
Issue Category	Area
Tool	ICC2_tool
Severity	Medium
Issue Description	During the floorplanning stage, the core area was initially estimated based on standard cell area derived from the synthesis reports and macro area obtained from the library files. After placing the macros, it was observed that the macros were predominantly vertically aligned, resulting in an elongated floorplan structure.
Error Message/Log	
Root Cause Analysis	**Vertical Macro Clustering** The macros from the library were dimensionally taller than wide and were placed in a vertically stacked manner. This created a narrow horizontal routing and concentrated routing demand in limited regions.

	Suboptimal Aspect Ratio Selection The initial core aspect ratio did not consider macro geometry and alignment. As a result, the block shape did not align with the macros
Debug Steps Followed	Step1: I checked for std.cell area & macro area by using report_design Step2:using those areas I calculated core area(total cell area/utilization) Step3:based on that area I selected height and width of the core. Step4:w=1059 : h=1377
Solution Applied	Followed above steps and analysed the issue Changed aspect ratio from default one to fix the macros vertically(to reduce congestion and timing issues)
Result After Fix	After changing core area dimensions : Congestion overflow reduced from 2.5% to 0.2%(H) Red Hotspots count reduced in congestion map Better Placement Spreading, Enhanced Timing Stability
After changing core dimentions	

Issue #3

Field	**Details**

Issue Title	Check_pg_drc,check_pg_missing_vias
Design Stage	Power planning
Issue Category	Power rails,vias
Tool	ICC2_tool
Severity	Medium
Issue Description	During power planning, check_pg_drc and check_pg_missing_vias reported design rule violations and missing via connections in the power grid. These errors indicated incomplete VDD/VSS connectivity.
Error Message/Log	
Root Cause Analysis	The violations were caused by improper power strap spacing and incomplete via stacking between intersecting metal layers during power mesh creation. The PG strategy parameters (strap pitch, width, and via insertion settings) were not fully aligned with technology design rules, leading to DRC and missing via errors.
Debug Steps	Step1: Executed check_pg_drc and check_pg_missing_vias to identify specific violation locations and affected layers.

Followed	Step2: Reviewed violation coordinates in the GUI to analyze strap intersections, spacing, and via stacking between metal layers. Step3:Inserted vias by selecting same metal layer vias and stretched the tool where required Step4:By checking missing vias and pg drcs came to know that errors are cleared after inserting vias manullay using error browser.
Solution Applied	Followed above steps and analysed the issue.
Result After Fix	After correcting the power grid strategy parameters and regenerating the power mesh, all DRC and missing via violations were successfully resolved. Re-running check_pg_drc and check_pg_missing_vias confirmed complete VDD/VSS connectivity and design rule compliance.

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5. Results and Analysis

5.1 Stage-wise Metric Progression

Stage	Area (μm²)	Setup WNS (ns)	Setup TNS (ns)	Setup NVP	Power (mW)
Synthesis	1.02	-0.11	-81.21	2458	383.06
Placement	1.14	-0.24	-10.67	780	3.87e+02
CTS	1.14	-0.32	-46.93	1416	1.25e+02
Routing	1.14	-0.46	-1308.16	28737	1.18e+02
Post-Route	1.41	0.02	0	0	1.21e+02

5.2 Final Power Breakdown:

Component	Power (mW)	Percentage
Sequential	2.67e-02	0

Combinational	6.07e+00	5
Clock Network	1.13e+00	93.2
Leakage	8.13e-02	6.7
Total	1.21e+02	100%

6. Conclusion and Learnings

6.1 Technical Learnings

Synthesis Learnings:

During synthesis, I learned how RTL is optimized into gate-level netlist based on timing, area, and power constraints, and how constraints (SDC) directly impact QoR. I also understood the importance of analyzing reports such as timing, area, and constraint violations to ensure a clean handoff to physical design.

PnR Learnings:

During PnR, I learned how floorplanning, power planning, placement, CTS, and routing collectively impact timing, congestion, and overall design quality. I also understood the importance of resolving physical, electrical, and clock-related issues at each stage to achieve timing closure and signoff-ready design.

Verification Learnings:

During verification, I learned the importance of validating design functionality and physical correctness through checks like DRC, LVS, timing verification, and power integrity analysis. I understood how early detection of logical and physical errors prevents costly rework in later design stages .I came to know that how to verify reports and select appropriate solution for that particular problem.

Tool Usage Learnings:

I gained hands-on experience with industry-standard EDA tools(icc2,dc), understanding how to execute each design stage from RTL_GDSII using appropriate commands and analyze reports for debugging and optimization. I also learned systematic problem-solving by interpreting tool outputs, identifying root causes, and applying corrective actions effectively.

Conclusion:

In this tile-based project, the complete RTL-to-GDSII implementation flow was successfully executed using Synopsys Design Compiler (DC) and ICC2. The design was synthesized in DC with proper timing constraints, generating an optimized gate-level netlist and synthesis reports for area, timing, and constraint analysis. The netlist was then imported into ICC2, where floorplanning, power planning, placement, CTS, and routing were systematically performed.

At each stage, detailed analysis of timing, congestion, and design rule checks was carried out to ensure design correctness and performance optimization. Post-routing, final verification steps were completed, and industry-standard output files such as GDSII, SPEF, and final Verilog (.v) were successfully generated. This project provided hands-on experience in handling real physical design challenges, debugging tool reports, and understanding the impact of each stage on overall design QoR, ultimately achieving a signoff-ready implementation.

***THANK YOU**
