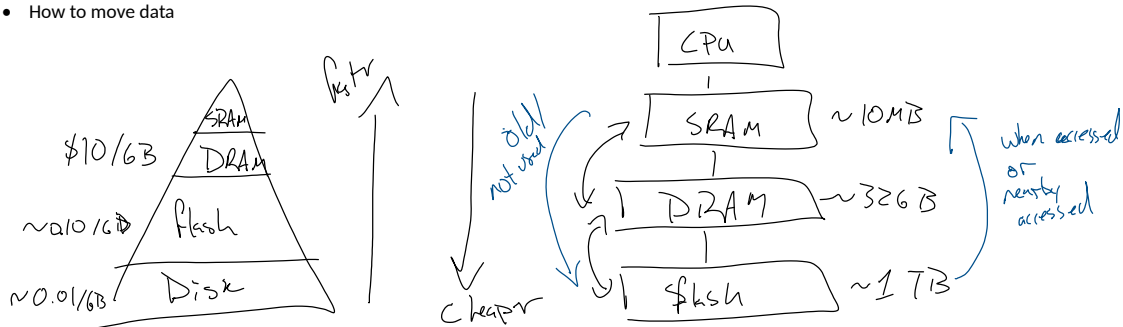


Discussion 7: Hierarchy

Thursday, February 21, 2019 2:34 PM

Outline

- Hierarchy
- Locality
 - Temporal
 - Spatial
- How to move data



how to decide when/what to move?

→ how often accessed
frequent things close

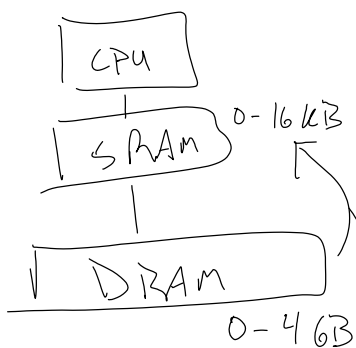
things close to each other (sequentially)
→ pre load / move together

locality

temporal

spatial

→ "prediction"



- 1) try to find data in SRAM
 - 2) go to DRAM
 - 3) put in SRAM
- hash table maps DRAM addr to SRAM addr

hardware cache

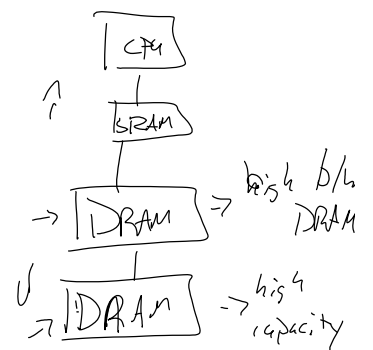
two pools of memory

Let programmer move data from
SRAM/DRAM and back

Scratchpad memory or → CPU
Software cache

tag + valid + state

knight's landing

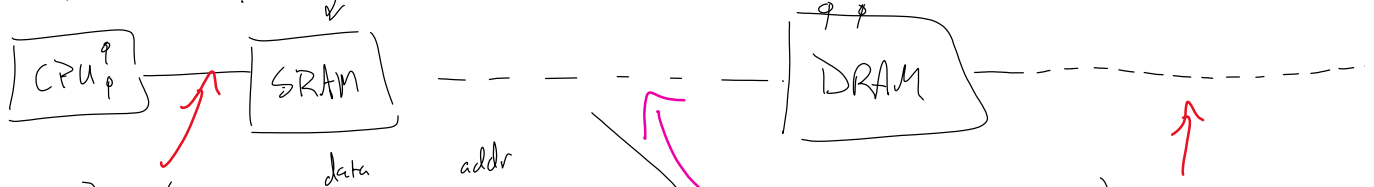


More complex?

hardware cache

→ lots of metadata
to track addresses present
& where address's data is

how to move data?



bus/wires $\sim 64 \text{ bit} + 32 \text{ bit}$
 parallel $\rightarrow 512 \text{ bit}$
 short \rightarrow very fast \rightarrow @ clock speed
 on chip \rightarrow wide
 low power \rightarrow small wires

Off chip limit
 \rightarrow through pins
 onto fiberless board
 thick + long wires
 \rightarrow higher power
 clock is slower

on motherboard
 \rightarrow thick
 serial bus
 \rightarrow more lat
 more package pin
 low bandwidth

narrower bus \rightarrow pretty wide
 64 bits \rightarrow

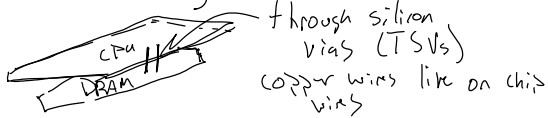
Radio/microwave interconnect

\rightarrow low latency @ speed of light
 \rightarrow interference \rightarrow convert to
 \rightarrow expensive \rightarrow power \rightarrow e/m waves

Optical interconnect

\rightarrow thicker waveguide
 \rightarrow low latency
 \rightarrow high bandwidth per "pin"
 \rightarrow incompatible w/ logic
 \rightarrow convert electric signals to light
 \rightarrow expensive

3D die stacking



wide busses low power \rightarrow very expensive
 high bandwidth \rightarrow heat
 low latency \rightarrow design packages
 \rightarrow new VLSI tools