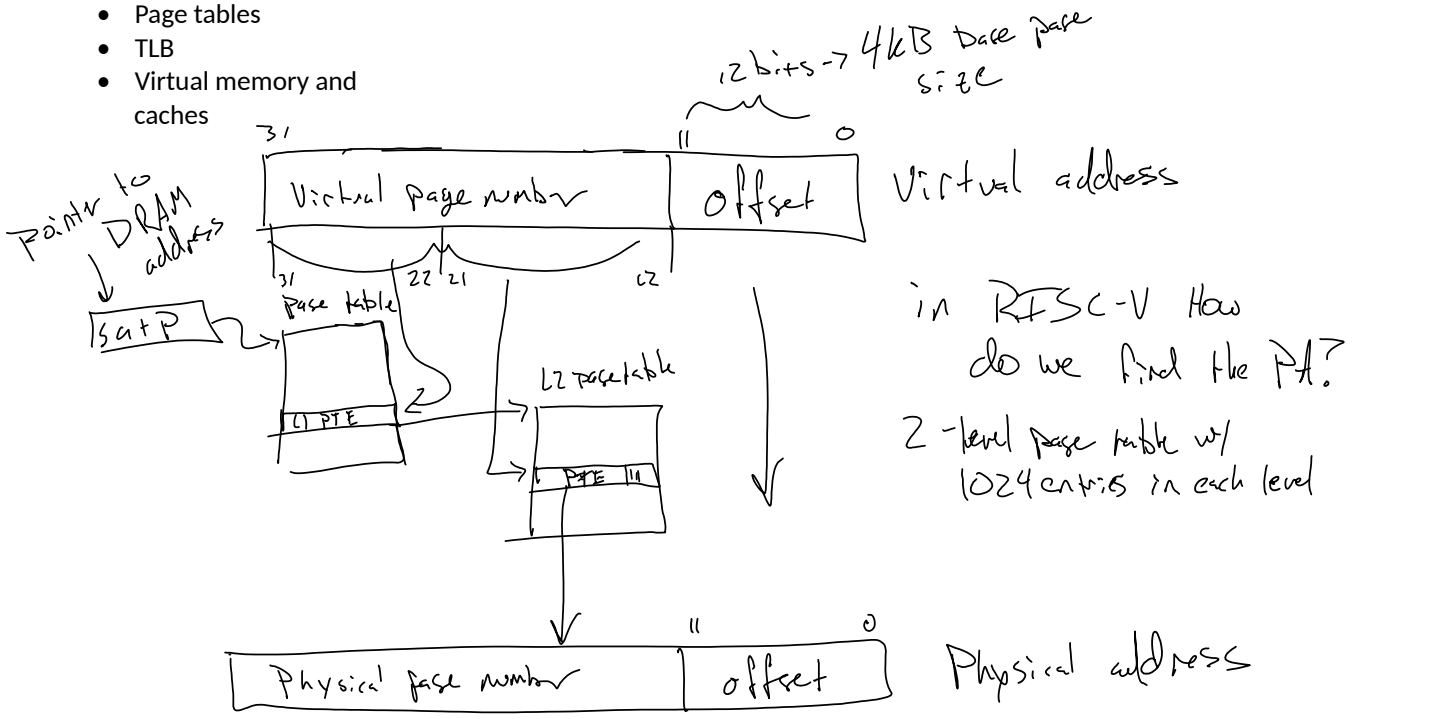
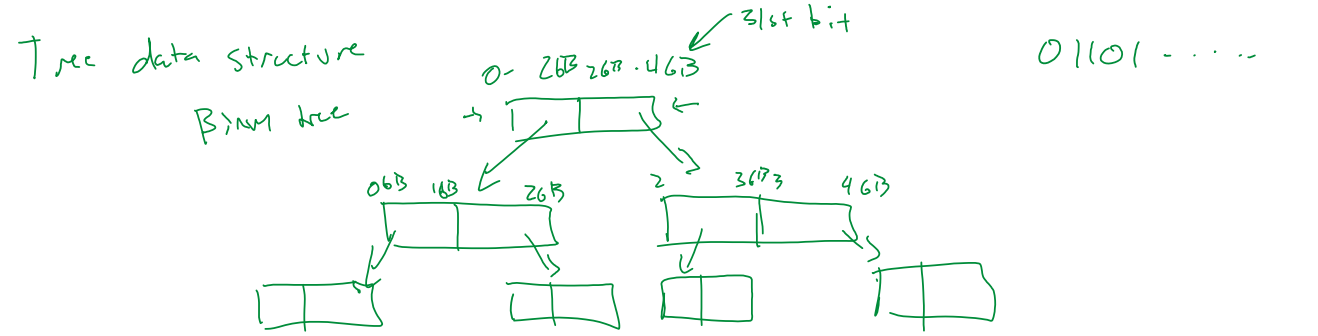
Lecture 23: Virtual Memory 2

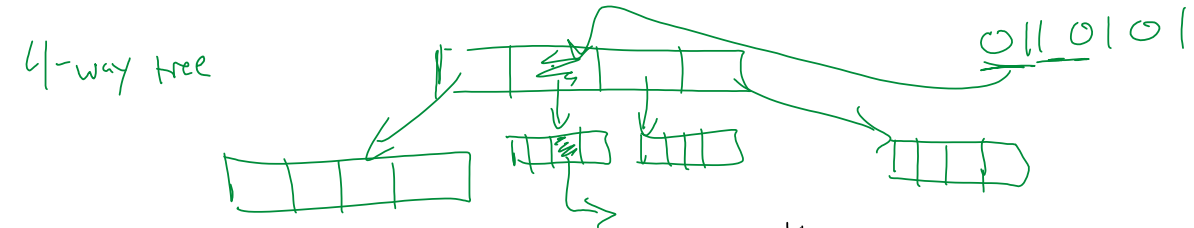
Monday, March 4, 2019 10:56 AM

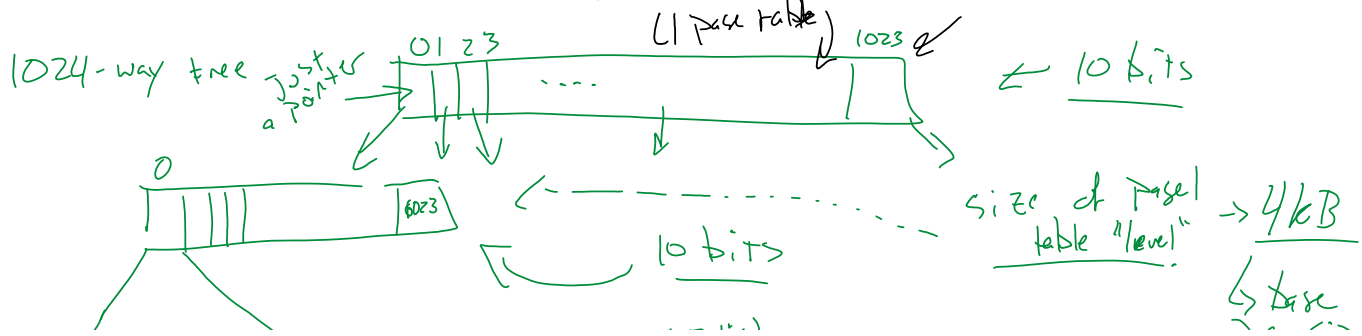
Outline

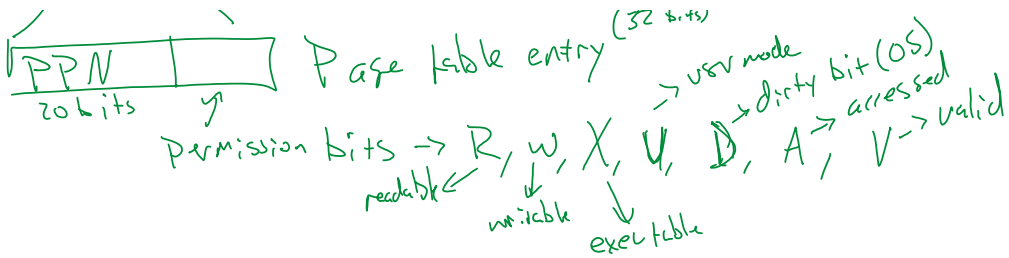
- Page tables
- TLB
- Virtual memory and caches









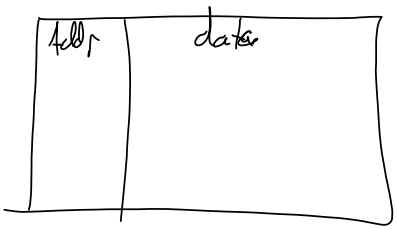


With virtual addressing -> 3 memory accesses per ld/st

↳ 64 bit Virtual address spaces have 3-5 levels

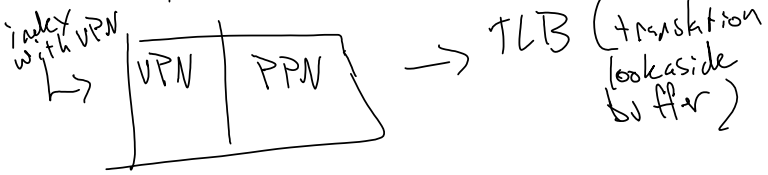
How to improve performance?

↳ CACHE!



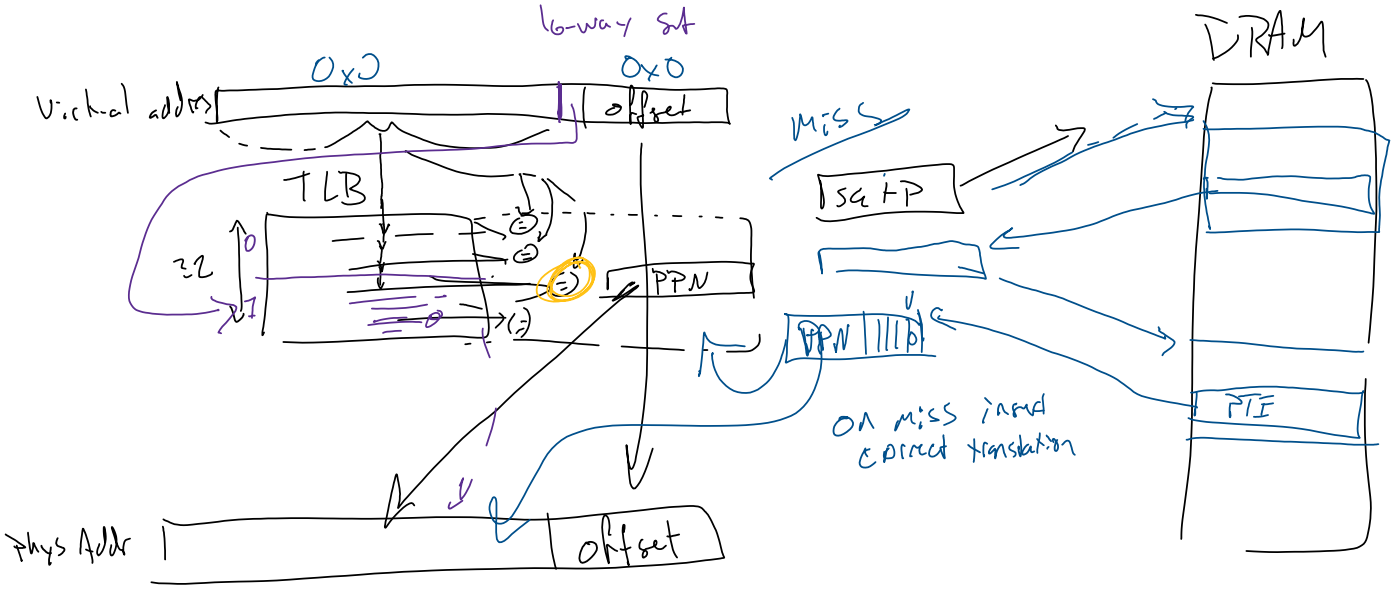
Address translation cache

very small and fast



↳ 16-32 entries

Want to minimize misses -> highly associative often fully associative



if PTE is invalid or permission doesn't match -> page fault exception