Lecture 15: Instruction level parallelism

Monday, February 11, 2019   8:14 AM

Outline

- Increasing performance with ILP
- Finding ILP
- Multi-issue pipeline
- VLIW

add
lw
sw
sub
j

Pipelining is one form of ILP
↳ Execute different parts of different instructions
↳ stages

Task-level parallelism →
↳ multi-threaded
Independent tasks
control? → no change

parallel

add	sub
lw	sw
sw	j
sub	add
j	br

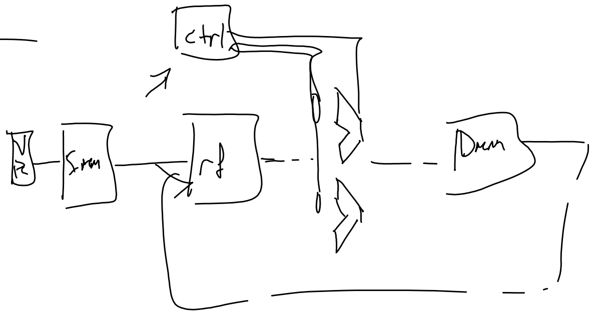
add → w/ independent instructions
lw
sw
sub
j

↳ add more execution units
another adder, branch unit, etc.

↳ different clocks? → difficult

more power
worry?

↳ group independent instructions statically in compiler → hard to do because many dependencies are only known dynamically
↳ Dynamically search for indepenent instructions w/ h/w



Finding ILP

SAXPY

```
for (int i=0; i<100; i++)
  z[i] = a*x[i] + y[i]
```

```
      Li x1, 100
      Add x2, zero, zero
                Addi x7, zero, 1
Top:
  →   Add x3, x3, x2     add x8, x8, x7
  →   Lw t0, 0(x3)       lw t2, 0(x8)
      Mul t0, x6, t0
  →   Add x4, x4, x2
  →   Lw t1, 0(x4)
      Add t1, t0, t1
  →   Add x5, x5, x2
      Sw t1, 0(x5)  <  addi  x2, x2, 2
      Blt x2, x1, Top addi  x7, x7, 2
```

independent

fewer control instructions
fewer control dependencies

loop unrolling

rather than one iteration at a time, if iterations are independent can do 2 or more at once

```
for (i=0; i<100; i+=2) {
  → z[i] = a·x[i] + y[i]       → independent
  → z[i+1] = a·x[i+1] + y[i+1]
}
```

RISC-V R

opcode	rs1	rs2	funct

j

opcode	imm

VLIW ISA
↳ very long instruction word

VLIW

op rs1 rs2	rs1 addr	rs1 offs	op rs1 rs2	rs1 rs2 off
ALU	Load	Store	ALU	Branch

EPIC
↳ explicitly Parallel Instruction computer

encode what each functional unit is doing in the very long instruction

SIMD → single instruction multiple data

ctr

1	1	1	0

predicate

regs

0	1	2	–
32	32	32	32

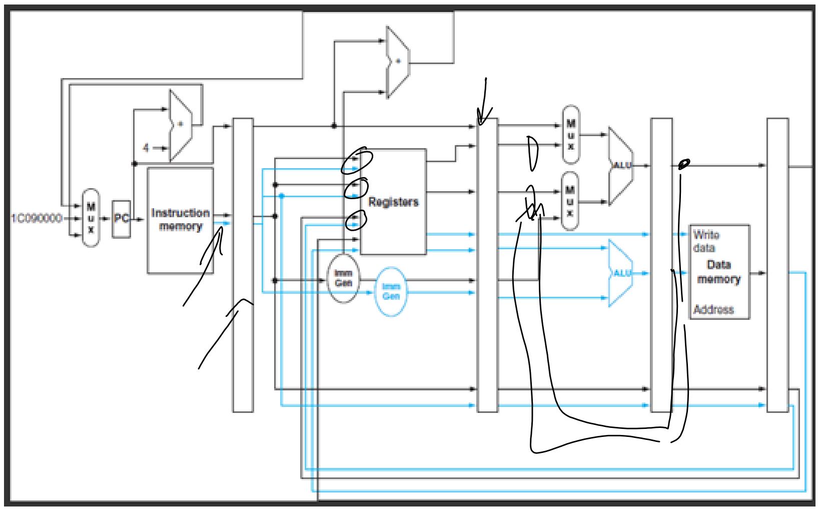
3	4	5	–

3	8	7	–

addsse w1, w2, w3

Static ILP

Dual-issue pipeline



1C090000
M u x
PC
4
Instruction memory
Registers
Imm Gen
Imm Gen
M u x
M u x
ALU
ALU
Write data
Data memory
Address