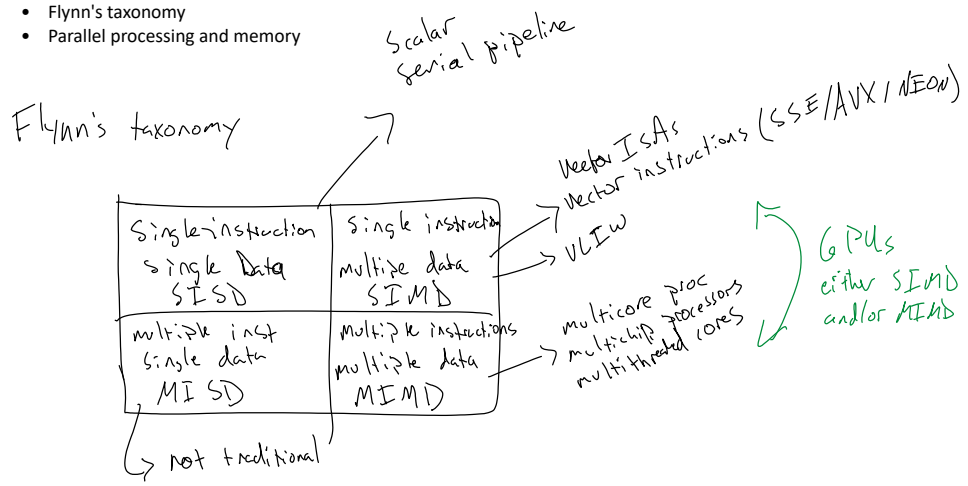
Lecture 26: Parallel 2

Monday, March 11, 2019 10:04 AM

Outline

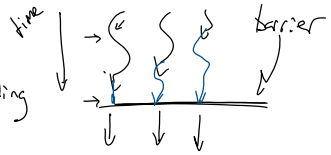
- Flynn's taxonomy
- Parallel processing and memory



Modern systems combine SISD, SIMD, MIMD

Barrier operation

↳ all threads wait for others to arrive before proceeding



int * arrived; = 0x10000 initialize arrived = 0

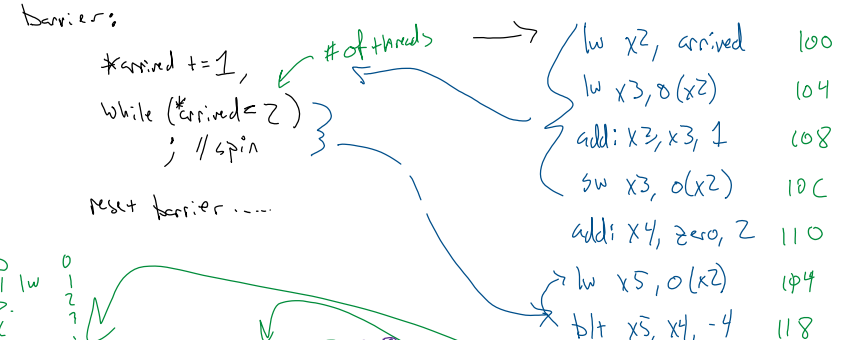
Barrier:

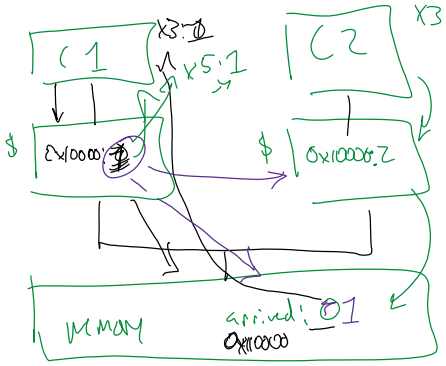
*arrived += 1,

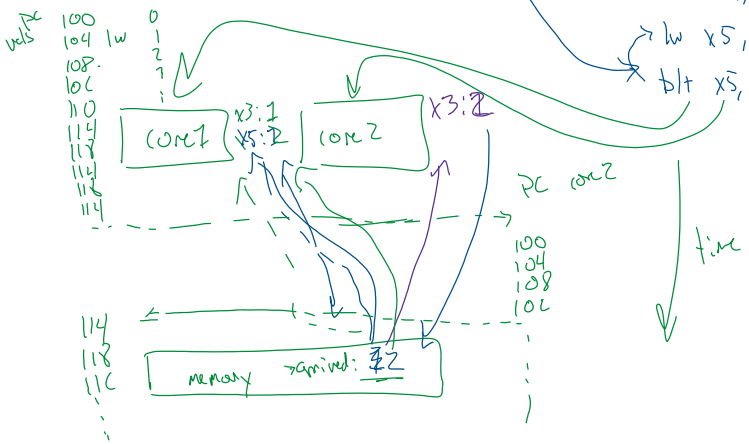
while (*arrived < 2)

; // spin

reset barrier ....







Cache coherence

↳ Rule: Single write -> Multiple reader

every read/write → broadcast all actions
↳ check all caches ↳ small systems w/ shared bus

notify central directory of → directory which is more
state of each block scalable than broadcast

need to add more cache block states
Valid, dirty, invalid ← "normal" states

for coherence add <u>shared</u> state

MSI protocol → modified, <u>shared</u>, Invalid