ECS 154B WQ 2019 **Practice Midterm 1**

Topics covered

Book: chapters 1, 2, and 4 (mostly 1 and 4).

Not every topic here is covered in the practice midterm, though most are.
Also check the written homeworks for more problems.

- Security
  - Meltdown and Spectre
  - Security as a design constraint
- History of computing
  - Moore's law
  - Dennard scaling
- CMOS devices
  - Energy
  - Power
- Trends in computing
- Instruction set architectures (ISAs)
  - RISC versus CISC
- RISC-V
  - Instruction types
  - Extensions
- From code to execution
  - Going from higher-level languages to machine code
  - Executing an instruction
- Single-cycle CPU
  - Datapath
  - Adding new instructions
- Performance
  - Measuring performance
  - Iron law
  - Amdahl's law
  - Latency and throughput
- Introduction to pipelining

1. _____ claims that the number of transistors per chip will double every 18-24 months.

2. Increasing the frequency of a processor leads to increased performance and increased _____.

3. What are three ways to compare two systems to determine which is the "better" system?

4. A _____ predicts the performance of a real-world application, but often has a shorter runtime and is standardized to allow comparisons across systems.

5. There is a processor with three stages: (fetch & decode), (execute), and (memory & writeback). The stages require 350 ps, 250 ps, and 400 ps, respectively.

    a. What is the cycle time if you implemented this as a single cycle processor (not pipelined)?

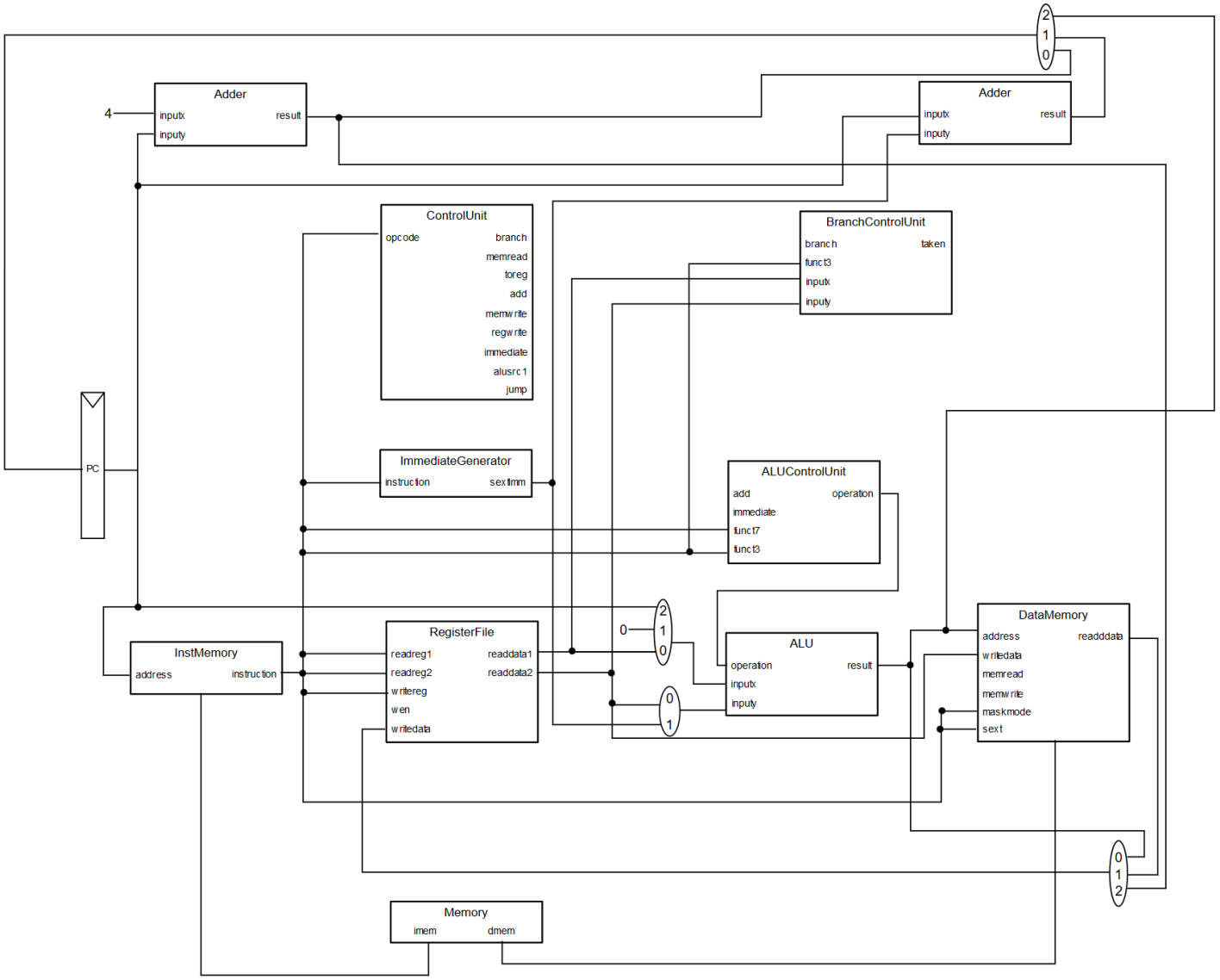
    b. What is the CPI of this processor?

    c. Say we decided to implement this as a pipelined processor instead. How many instructions can this pipeline potentially execute at once?

6. The ISA defines the interface between _____ and _____.

7. Processor A can run 1 billion instructions in 0.5 seconds at a frequency of 500 MHz. You are proposing a pipelined design for a new processor, design B. Your processor has a CPI of 4. The company you work for will not release a new design unless it has at least a 1.5x speedup compared to processor A. What is your target frequency?

For the rest of the problems on this page, use the single cycle DINO CPU diagram from Lab 2 below.



8. What does the *ControlUnit* block do?

9. Explain the *funct7* and *funct3* wires going into the ALU control unit, and what they do.

10. Shade the wires and structures used for a jump instruction on the diagram above.

11. What are the five canonical stages to executing an instruction, and what occurs in each stage?

12. Which instructions cause the PC to be written to?

13. A processor that executes more than one instruction per cycle is leveraging _____ for increased performance.

14. Amdahl's law is a mathematical representation of what common computer design principle?

15. Given the following systems, which will have a higher performance for a constant number of instructions? Why? Show your work.

	System A	System B
Pipeline Depth (stages)	5	10
Cycle time	2 GHz	2.5 GHz
Average CPI	3	5

16. Why should security be considered as a first-order design constraint when designing a new chip or architecture?

17. We are designing a processor for use in an embedded environment, where we will only ever be running one single-threaded application at a time. Would adding additional cores to this processor improve latency, throughput, neither, or both? Explain your answer.

18. _____ power in a CMOS device increases as the size of the transistors decrease, while _____ power increases as the number of transistors in the device that are switched increase.

19. Name two ways that we can decrease the amount of power/energy utilized in a CMOS device. You may want to write out the CMOS device power equation to help you answer this question.

20. According to Dennard's law, power density of a transistor _____ as we decrease the size of the transistor.

21. The reliability of a transistor _____ as we decrease the size of the transistor.

22. Examine the following seven-stage pipeline. Is it balanced? If not, suggest a change to balance the pipeline.
    a. *Fetch:* 170 ps
    b. *Decode:* 180 ps
    c. *Read Register*: 160 ps
    d. *Execute 1*: 175 ps
    e. *Execute 2*: 175 ps
    f. *Memory*: 165 ps
    g. *Writeback*: 155 ps

23. What value does register 0 take in RISC-V? Can we change that value by writing to it?

24. Why have we been unable to significantly increase the average frequency that cores on our processors run at over the past 10 years? What is the limiting factor?

25. RISC instructions tend to be less "powerful" than CISC instructions, thus it takes more RISC instructions to write a program compared to the same program written for a CISC architecture. How are RISC architectures faster than CISC architectures despite this problem?