

Lecture 18: Memory Hierarchy

Wednesday, February 20, 2019 10:59 AM

Outline

- more memory tech
- hierarchy
- locality
- Data movement

nop? → assembler pseudo op
in RISC-V → `addi zero, zero, 0` (0x00000000)

// "avipc 0"
→ 0: `avipc x5, 0`
"avipc 1"
→ 0: `nop`
4: `avipc x5, 0`

0: `addi zero, zero, 0` 0: `nop` 1
4: `addi` ← 4: `nop` 2
8: `addi` ← 8: `nop` 3
12: `addi` 12: `nop` 4
→ 16: `avipc x5, 0`

	SRAM	DRAM	Magnetic disks	Flash	new tech
Latency	low (1 cycle) ~1ns	medium 15-45ns	~10ms high latency	~10µs high	~10ns for reads ~1µs for writes
Density area per bit cost	low 10's MB	high 100's GB	very high 10's TBs	very high 10's TBs	very high 1-2 TBs
Volatility	Volatile	Volatile	non volatile (store)	non volatile	non volatile

Magnetic disks

Storage technology

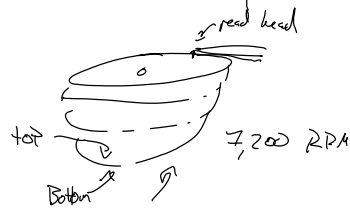
↳ Very high density

↳ store information @ near atomic level

↳ many platters

Latency

↳ high (very) → moving parts



10,000 RPM

↳ 167 RPS

$\frac{1}{167} = 0.00599s$

5 ms

Solid state "disks"

Flash → floating gate transistor

↳ 1 transistor store data → store multiple bits per transistor

high density

↳ per volume → higher than magnetic disk

↳ cost per bit higher than magnetic disks

Latency

↳ lower than spinning disk

↳ higher than DRAM/SRAM (Read)

↳ write latency is higher than read

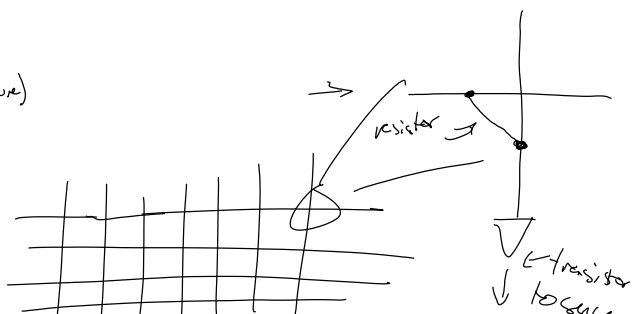
write endurance is low (10's-100's of writes before failure)

Other persistent memory technologies

"3D X point" → optane

PCM → phase change memory →

normal memory array



latencies very high density/
↳ ~ flash

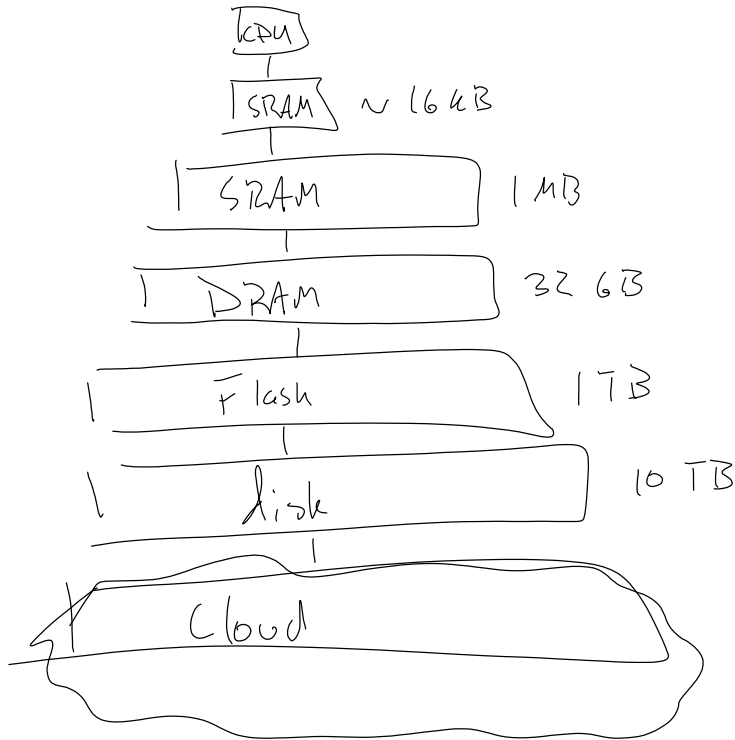
↳ write → high latency (~1ms) } asymmetric read/write latency
read → faster than DRAM

DINO CPU assumes < 1 cycle memory

↳ SRAM → ~100KB

What can we do to have TBs of data but access it in us

Build system w/ combination of many technologies



hierarchy
of diff. tech

PB → EB 100ms