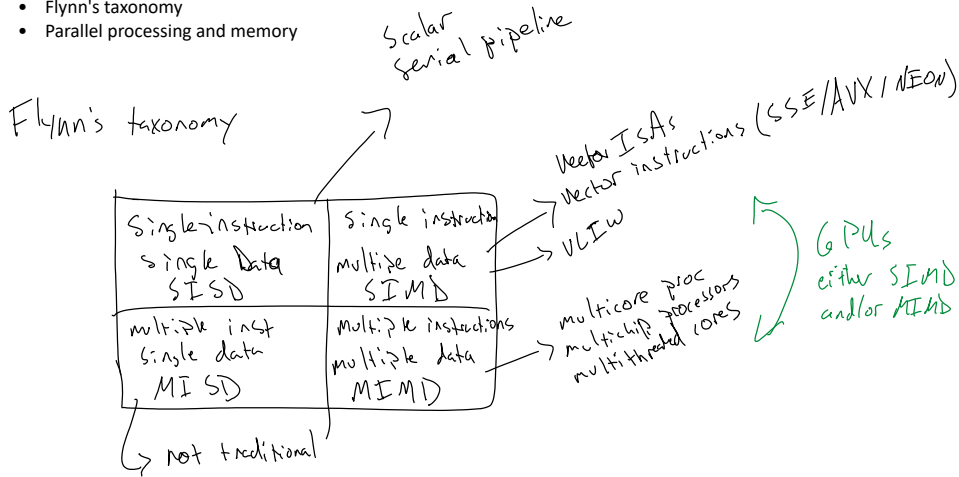


# Lecture 26: Parallel 2

Monday, March 11, 2019 10:04 AM

## Outline

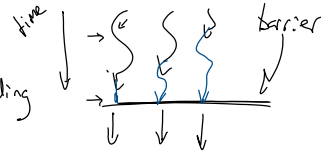
- Flynn's taxonomy
- Parallel processing and memory



Modern systems combine SISD, SIMD, MIMD

## Barrier operation

↳ all threads wait for others to arrive before proceeding



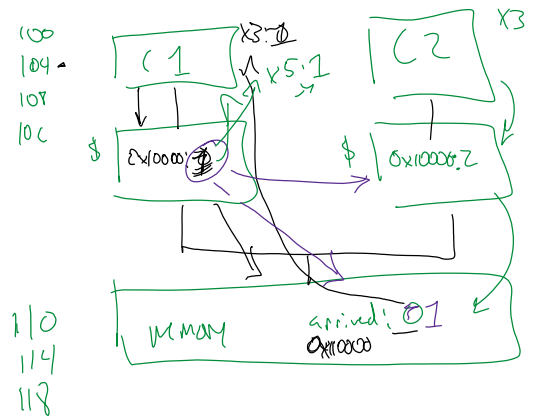
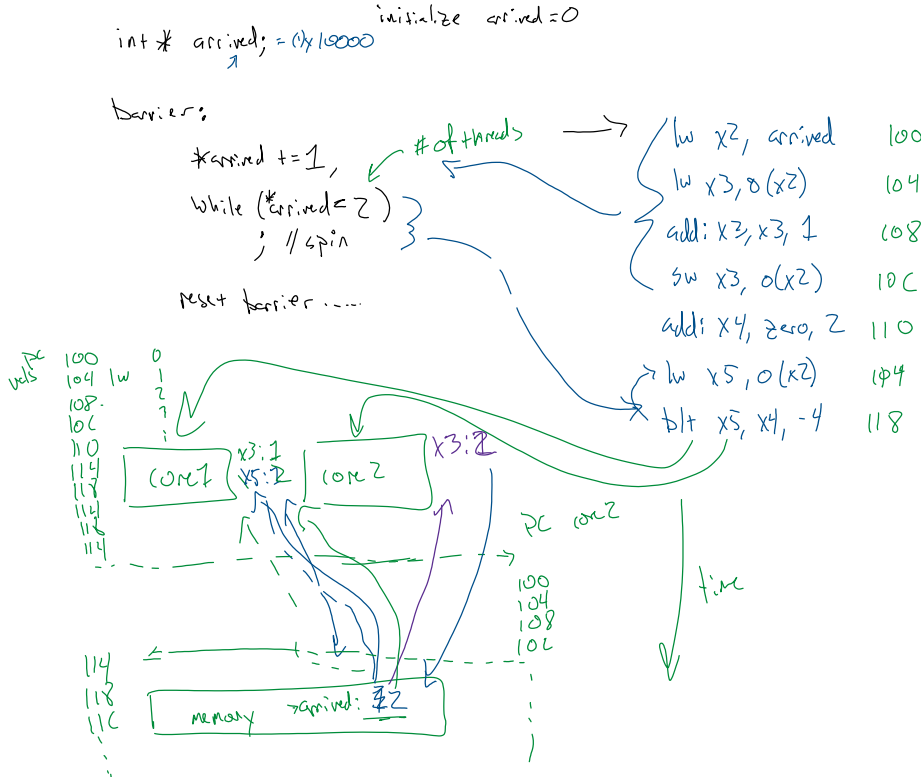
initialize arrived = 0

int \* arrived; = 0x10000

barriers:

```
*arrived += 1,
while (*arrived < 2)
; // spin
```

reset barrier .....



## Cache coherence

↳ Rule: Single write  
→ multiple reader

every read/write → broadcast all actions  
↳ check all caches ↳ small systems w/ shared bus

notify central directory of state of each block → directory which is more scalable than broadcast

need to add more cache block states

Valid, dirty, invalid ← "normal" states

for coherence add shared state

MSI protocol → modified, shared, Invalid