COMP 300

FORMAN CHRISTIAN COLLEGE

(A CHARTERED UNIVERSITY)

COMPUTER ORGANIZATION WITH ASSEMBLY LANGUAGE

MID EXAM-1

Maximum Marks: 100 **Time Window: 96 Hours**

Weightage towards total marks: 15% **(4 days)**

This homework alone carries 15% weightage of the total grade for this course. Marks obtained in this instrument will be contributed towards MID exam.

This home work MUST be completed in complete isolation on individual basis.

It's an open books and open notes task. Use of Internet is allowed, but you must provide references to web sites and /or tutorials from where you got help for this home work. You MUST NOT share your work with any of your class fellow. Any such attempt will result in a ZERO grade.

Both LOGISIM file/s and report need to be submitted within the given time window

Rubric

Correct simulation	**70%**
Proper labelling of simulation diagrams	**05%**
Well formatted report	**25%**

MidExam-1 Task

In this task you need to design a data path with following components:

- Register file
  - Count of registers in the register file should be 4.
  - Each register can store a 4 bit unsigned numeric value.
  - The design of register file is same as we have done in a previous lab.
  - Note that you need not to design registers, decoder, and MUX from scratch.
  - You are allowed to get register, decoder and MUX from the LOGISIM tool box.

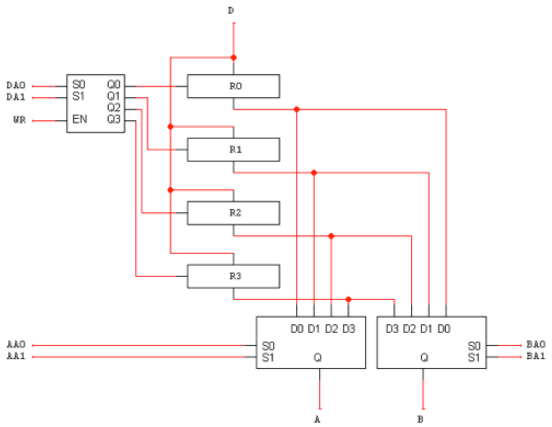

Figure 1: Register File

- ALU
  - ALU in our case is a simple 4-bit ALU with 4 bit operation code.
  - Note that it is the same ALU that we have discussed in our prior lectures.
  - You need to design the ALU (if you have not designed it already in some prior lab session) on LOGISIM.
  - For the time being forget about the V, C, N and Z signals.
  - Further, the S signal lines are equivalent to FS signal lines in the data path.
  - The final shape after converting it into a sub-circuit is as shown:

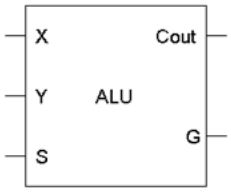

Figure 2: ALU

- Main memory
  - We will assume that the memory is 4 bits in width and has 16 distinct locations. This means we need a 4-bit value to completely address this memory.
  - You need to design the memory on LOGISIM from scratch (or may use the one you have designed earlier) and create its sub-circuit for further use.

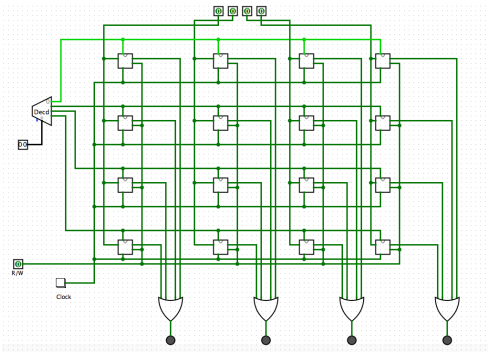

Figure 3: Memory

- Final shape of your design is shown below. It is same you have seen in your past lectures.

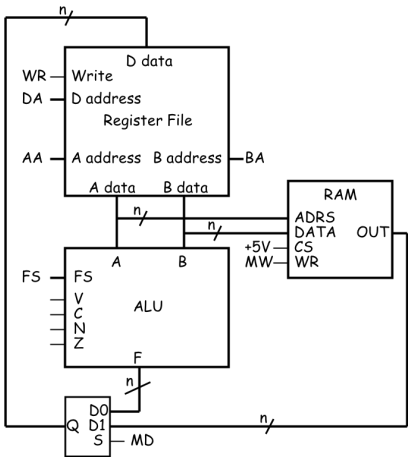

Figure 4: The Data Path

- Note the set of MUXs that transfer data either from ALU or from memory to the register file. You need to design this as well. Use MUX from the tool box of LOGISIM.
- Once you have successfully designed a data path, you need to run it with at least two simple programs written in RTL. Your programs should include some basic operations on registers and memory data. You should also show how data is stored and retrieved to and from the memory.
- Please note that you need to provide correct control signals in order to run the program correctly.
- Make sure that you have connected four LEDs to the output of MUX (right after Q output shown in the figure above). This way we will be able to debug your design.
- The detailed description for each run of your RTL program along with the control signals should be provided in your report.
- It is highly recommended to attach screen shots of your simulation with necessary control signals shown clearly in the report.

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Deliverables

Following files are required in your zip folder:

- A sub-circuit for register file.
- A sub-circuit for ALU.
- A sub-circuit for memory.
- A sub-circuit for set of MUXs.
- Finally, a sub-circuit of complete data path with all components integrated correctly.
- Report file in pdf format having
    - detailed description how you have designed each component in the data path.
    - It is preferable to use figures and diagrams to illustrate your understanding.
    - Simulation run of at least two RTL programs with at least three lines including transfer of data between registers, usage of different operations, transfer of data between register file and memory and vice versa.
    - Use screen shots of your final design to augment the simulation run.

Submission Format

You are required to submit following before the time window expires.

- Logisim design file/s
- Report

Logisim file/s and report should be submitted in zip format with your roll number as its name. Follow this naming convention:

<your roll number>_COMP300<your section>21_MID-EXAM-1

Make sure that the report should follow the template already shared with the class.