COMP 300 Section B

FORMAN CHRISTIAN COLLEGE

(A CHARTERED UNIVERSITY)

COMPUTER ORGANIZATION & ASSEMBLY LANGUAGE

LAB 2

ROLL No. **Time Allowed: 100 min**

SUBMIT THE LAB ON GOOGLE CLASSROOM

Google Classroom Code: cgdprua

This lab should be done in complete isolation. No group formation is allowed.

It's an open books and open notes lab session. You CANNOT share your code/work with each other. Any such attempt will result in a straight ZERO grade in this lab.

Use of Internet is allowed for this lab.

Rubric

Correct simulation	**60%**
Proper labelling of simulation diagram	**10%**
Well formatted report	**30%**

Lab Task [100 Marks]

In this lab you need to design an 8x4 RAM. You should perform the following steps:

- Design a binary cell using RS flipflop and couple of AND gates on LOGISIM.
- Create a sub circuit of this binary cell. Refer to my video lectures to get information about how to construct a sub circuit.
- Using these sub circuits, now design an 8x4 RAM.
- Make sure you add appropriate size OR gates in your design.
- You will also need to design a decoder with enable input using AND OR gates for your memory. Do not use the in-built decoder from LOGISIM tool box.
- Once you have designed all the required components, and integrated these, test your circuit and create a sub circuit of the entire RAM.
- Your final circuit should be a block that has
  - N lines to select one out of 8 rows of the RAM. (the address bus lines)
  - M input data lines where you can place data to be written into a particular row of the memory. (the data bus lines)
  - M data output lines where you can read data from a particular location in the memory. (the data bus lines)
  - Control signal lines
    - One to decide whether to read or write data.
    - Other one to enable / disable the decoder.
- Your simulation should consist of the following steps:
  - Write some 4-bit data in your RAM.

        - For this you will do the following, repeat it couple of times so that your memory is populated with data:
            - Place 4-bit data on the input side of the RAM (the 4 data lines)
            - Next choose some random address where to write your data.
            - Activate the control signals.
    - Now read the data written in the memory
        - For this you will perform following steps:
            - Place a valid address on the address lines(input of decoder)
            - Activate the control signals
            - Data should be available on the output lines.

You should submit all the files created in your design.

The simulation results (screen shots of your LOGISIM editor) should be included in the report.

Submission Format

You are required to submit following before the time of lab elapses.

- Logisim design file,
- the paper work that you have done before working on Logisim. (you can take image of the paper/s)

Make sure you submit your files in a zip format. Follow this naming convention for your zip file:

<your roll number>_COMP300B21_<lab number>

You also need to submit lab report. Lab report must be according to the template already communicated to all students. Lab submission is separate from the Logisim file/s submission. You will be given 24 hrs to write a decent report of the lab. Submit the lab report on google classroom