FORMAN CHRISTIAN COLLEGE
(A CHARTERED UNIVERSITY)

Computer Organization and Assembly Language – COMP 300 B

Spring 21

Lab - 02

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You should attach the lab / assignment handout as second page of this report.

From third page onwards following headings should be included:

- **Introduction**
  - **Should carry information of all major library functions.**
- **Your logic / algorithm in simple English. Bullet points are appreciated.**
- **Your code**
- **Screen shots of at least three outputs of your code with appropriate inputs.**
- **References**

INTRODUCTION

To make the binary cell, I used 3 AND gates, 2 NOT gates, a SR flip flop and several input/output pins. They are the basic building block to make a RAM. They can Write and Read a 1-bit value.

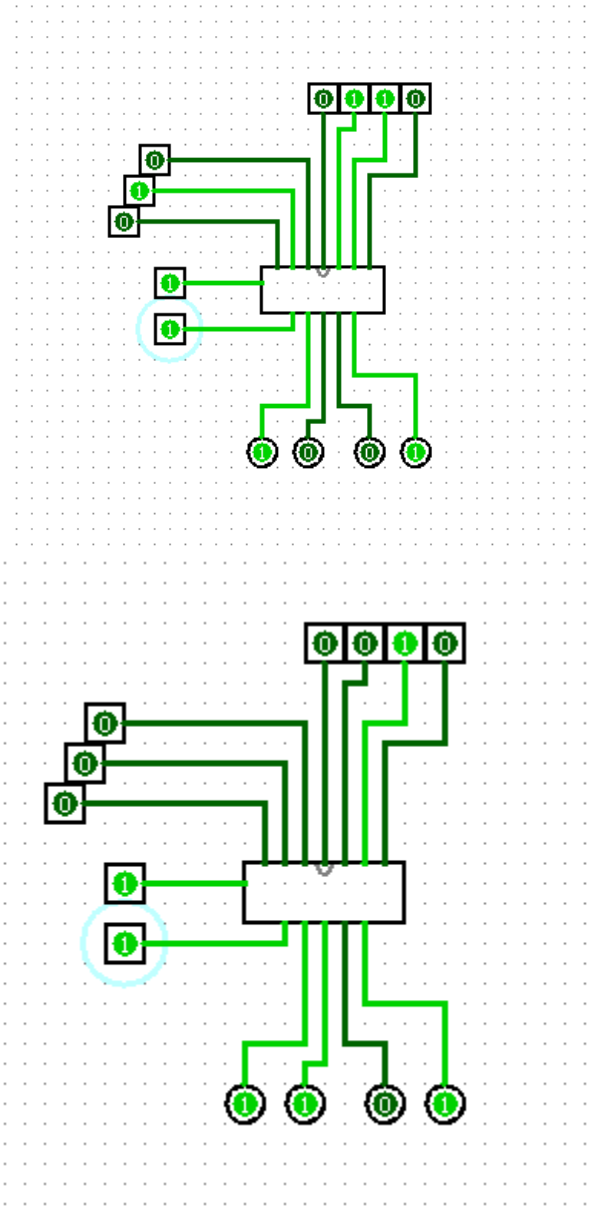
To make the 3x8 Decoder, I used 8 AND gates, 3 NOT gates and several input/output pins. A decoder selects only 1 of its outputs, depending on its inputs. In this case, depending on the 3-bit input it would select 1 of outs 8 outputs.

To make the 8x4 RAM I used, 32 Binary cells and a 3x8 Decoder (both made previously), 4 OR gates and several input/output gates. This RAM could Read and Write a 4-bit value.

LOGIC

- I first made a binary cell, following what we learnt from a previous lecture. Then I made a sub-circuit of it.
- Then I made a 3x8 Decoder. By first making a truth table for it and then using it to make the circuit. Then I made a sub-circuit of it.
- Then for the RAM, it would have 8 rows and 4 columns, in total consisting of 32 binary cells.
- I laid out the sub-circuits of the binary cells in that format and the decoder too.
- Each row of binary cells would have a common select input line, connecting to one of the decoders outputs. 8 rows of binary cells, connecting to each of the 8 decoders outputs.
- The decoder has 3 input pins connecting for input of a 3-bit value. And an enable input.
- Each column of binary cells would have a common input line. In total 4 input lines, connecting to 4 separate input pins.
- All of the binary cells have the same Read/Write input.
- Each column of Binary cells, have their output lines connecting to an OR gate. 4 columns, each connecting to their own OR gate, creating a 4-bit output.
- This completed the 8x4 ram. Which can Read/Write 4-bit values.

OUTPUTS



NOTE:

- I forgot to add the sub-circuit for the whole RAM in the logism file. I've only made the sub-circuit here for the output simulation, for ease of displaying the inputs and outputs.
- The RAM was complementing the ouput. Which could have been fixed by adding NOT gates at the inputs.
  I believe this issue is caused by a mistake in the construction of the binary cell. However, I'm not completely sure.