COMP 300 Section B

FORMAN CHRISTIAN COLLEGE

(A CHARTERED UNIVERSITY)

COMPUTER ORGANIZATION & ASSEMBLY LANGUAGE

LAB 3

ROLL No. **Time Allowed: 24 Hrs**

This lab should be done in complete isolation. No group formation is allowed.

It's an open books and open notes lab session. You CANNOT share your code/work with each other. Any such attempt will result in a straight ZERO grade in this lab.

Use of Internet is allowed for this lab.

Both LOGISIM file/s and report need to be submitted within the given time window

Rubric

Correct simulation	**60%**
Proper labelling of simulation diagram	**10%**
Well formatted report	**30%**

Lab Task

In this lab you need to design a register file discussed in the video lecture uploaded last week.

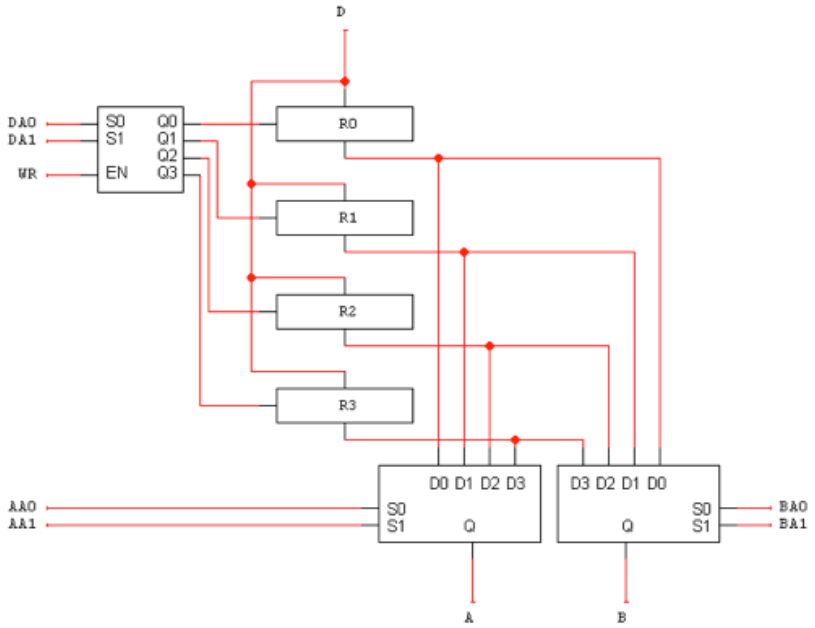
The register file size should be 4 x 8. This means the registers should be 4-bit in width and there are a total of 8 registers in the file. Registers may be named as R0, R1, …, R7.

Note that you need NOT to design any subcomponent from scratch. This means, you can get registers, decoder, and multiplexers from the tool box of LOGISIM.

You may need to use splitter to split the output from a single line to multiple lines.

A button may be helpful to apply clock.

You may follow the diagram provided in the lectures. Here number of registers are four and we are assuming n-bit data.



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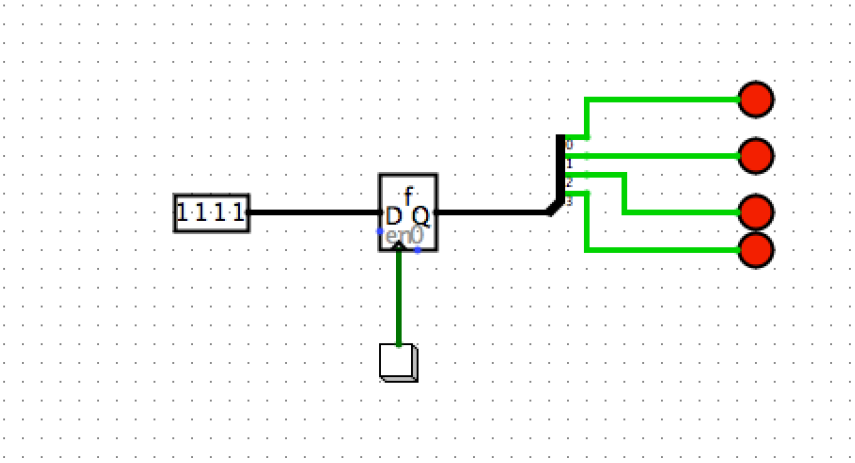
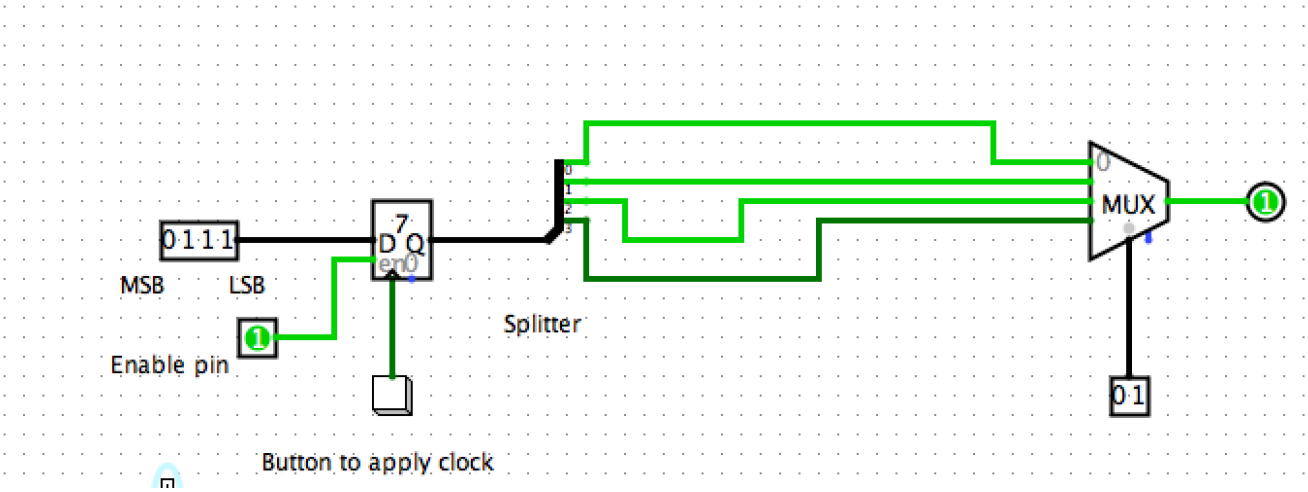
For your convenience a LOGISIM diagram is shown in which a 4 bit register is connected to input and output through a splitter. The output of the register is displayed with the help of four LEDs. Also note there is a button connected to the clock input of the register. It is used to apply controlled clock to the register. The register will change its state only when clock is applied.



Similarly a register interfaced with a MUX is shown:



Make sure you feel comfortable with these circuits before you move ahead

Once you have designed the register file, create a sub circuit of your design and run it using appropriate data as shown:

Test Run 1

- Select the register R3 by applying appropriate values on the register address lines.
- Place some 4- bit data on the input data lines.
- Make sure that the data should be stored in R3 during next clock pulse.

Test Run 2

- Select the register R5.

- Place some 4-bit data on the input data lines.
- Make sure that the data should be stored in R5 during next clock pulse.

Test Run 3

- Now make appropriate arrangements to read both the registers R3 and R5 on the output side of the register file.

Note that in your report you need to explain in some detail each component that you use in your design from the LOGISIM tool box. It is strongly suggested that your report should be neatly decorated with the sample images which show your efforts while understanding the behavior of different components (registers, multiplexer, decoder, splitter etc)

Submission Format

You are required to submit following before the lab time expires.

- Logisim design file/s
- Lab Report

Logisim file/s and report should be submitted in zip format with your roll number as its name. Follow this naming convention:

<your roll number>_COMP300B21_<lab number>

Make sure that the report should follow the template already shared with the class.