Department of Computer Science
Forman Christian College
(A Chartered University)
Lahore

Digital Logic Design
COMP 206

DIGITAL LOGIC DESIGN
COMP 206
LAB 01- RUBRIX

DESCRIPTION	MARKS ALLOCATED
Attendance	5%
Proper handling of components and measuring instruments. Especially current and voltage measurements	20%
Hardware wired completely(for all circuits)	30%
Data table 1	10%
Data Table 2	10%
Data Table 3	5%
Data Table 4	10%
Self debugging	10%

Marks will be deducted in case if students have not completely and correctly filled the data tables.
Note that these marks are max in each category. We may assign less than the given percentage of marks in case students have not successfully completed all the requirements.
This lab is time constrained. Please note that you must finish your work and submitted duly filled handout to the lab engineer within given time.

LAB 01

FAMILIARIZATION WITH LOGIC TRAINER AND VERIFICATION OF TRUTH TABLE OF BASIC LOGIC GATES.

Name:

Roll Number:

Date:

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1. **Objectives:**

   Having completed this experiment, you will be able to:

   i. Understand the different options, facilities and provisions provided on the logic trainer.
   ii. Recognize the different logic gates.
   iii. Verify the truth table of basic logic gates:

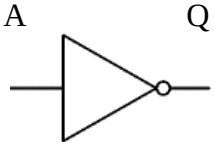
1.	AND	7408
2.	OR	7432
3.	NOT	7404
4.	NAND	7400
5.	NOR	7402
6.	X-OR	7486

2. **Basic Information:**

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions l*ow/false* (0) or *high/true* (1), represented by different voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V).There are seven logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.

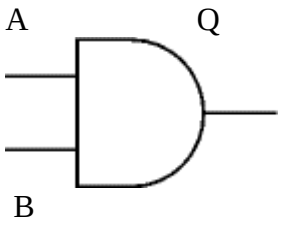
Logic Gates & their Symbols:

- **NOT gate (inverter):** The output Q is true when the input A is NOT true, the output is the inverse of the input: Q = NOT A. A NOT gate can only have one input. A NOT gate is also called an inverter.



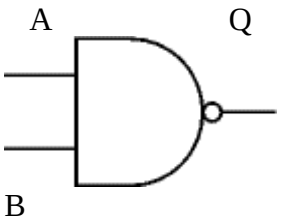
- **AND gate**

The output Q is true if input A AND input B are both true: **Q = A AND B** An AND gate can have two or more inputs, its output is true if all inputs are true.



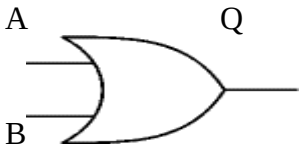
- **NAND gate (NAND = Not AND)**

This is an AND gate with the output inverted, as shown by the 'o' on the output. The output is true if input A AND input B are NOT both true: **Q = NOT (A AND B).** A NAND gate can have two or more inputs, its output is true if NOT all inputs are true.



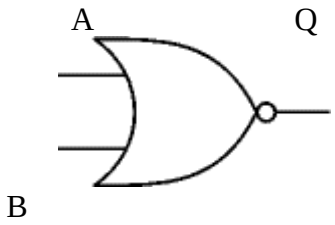
- **OR gate**

The output Q is true if input A OR input B is true (or both of them are true): **Q = A OR B**. An OR gate can have two or more inputs, its output is true if at least one input is true.



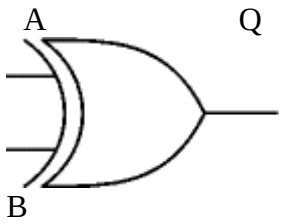
- **NOR gate (NOR = Not OR)**

This is an OR gate with the output inverted, as shown by the 'o' on the output. The output Q is true if NOT inputs A OR B are true: **Q = NOT (A OR B)**. A NOR gate can have two or more inputs, its output is true if no inputs are true.



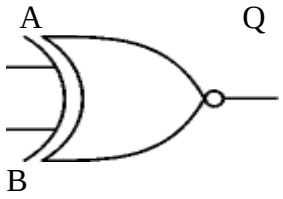
- **EX-OR (Exclusive-OR) gate**

The output Q is true if either input A is true OR input B is true, **but not when both of them are true**: **Q = (A AND NOT B) OR (B AND NOT A)**.This is like an OR gate but excluding both inputs being true.
The output is true if inputs A and B are **DIFFERENT**. EX-OR gates can only have 2 inputs.



- **EX-NOR (Exclusive-NOR) gate**

This is an EX-OR gate with the output inverted, as shown by the 'o' on the output. The output Q is true if inputs A and B are the **SAME** (both true or both false): **Q = (A AND B) OR (NOT A AND NOT B)**. EX-NOR gates can only have 2 inputs.



Experimental Work:

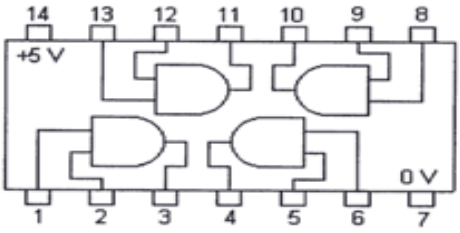
a. Material Required:

- Logic Trainer
- Connecting Wires
- Components (IC's)

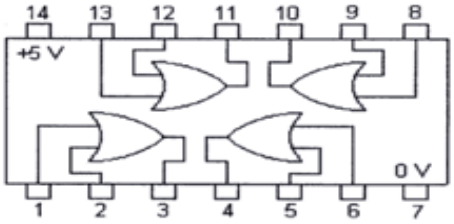
b. Procedure:

- Connect the logic Trainer to 220V Ac power supply.
- Turn the Trainer On and verify the voltage of power supply by using voltmeter.
- Install the IC chip under experiment on the trainer breadboard.
- Wire the circuit according to the diagram provided; supply the +5V and ground to pin number 14 and 7 respectively.
- Use logic switches to provide "0" and "1" for input of each gate one at a time as A and B.
- For the output indication use LED Lout.
- Verify the output according to the truth tables of each gate.
- Fill the truth table in at step 3.4 according to the results obtained.
- Write down your observation & comments

c. Experimental Results.



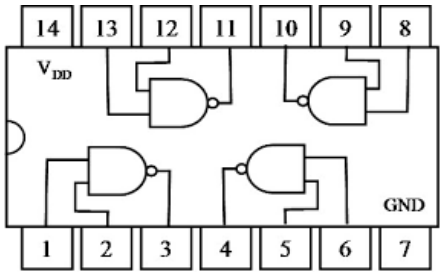
AND GATE (7408)



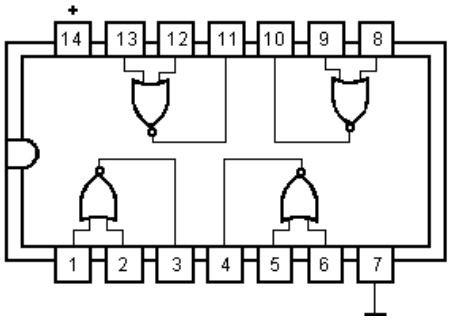
OR GATE(7432)

Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	

Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	



NAND GATE (7400)

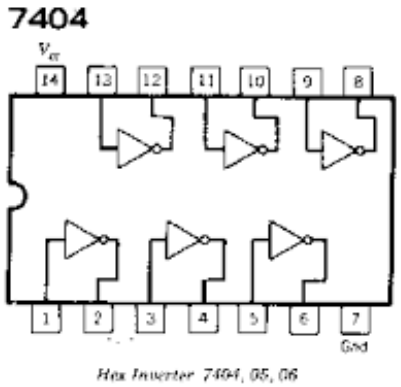


NOR GATE (7402)

Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	

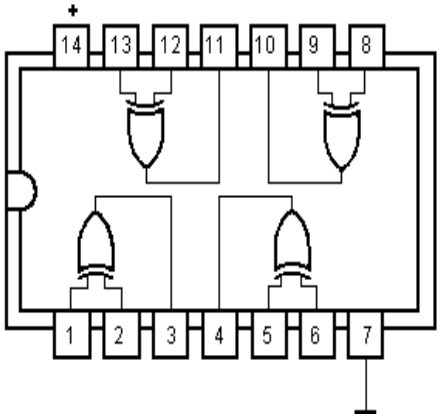
Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	

NOT GATE (7404)



Input A	Output A’
0	
1	

XOR GATE (7486)



Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	

IN CASE OF TROUBLE:

- Check the power supply.
- Check the Vcc and GND at pin number 14 and 7 of the IC under test.
- Check all the wire connections and remove the breaks.
- Check the IC under test using truth table.