Department of Computer Science
Forman Christian College
(A Chartered University)
Lahore

Lab 05

Digital Logic Design
COMP 206

DIGITAL LOGIC DESIGN
COMP 206
LAB 05- RUBRIX

DESCRIPTION	MARKS ALLOCATED
Attendance	5%
Proper handling of components, ICs and wiring	20%
Hardware wired completely(for all circuits)	30%
Data table 1	10%
Data Table 2	10%
Data Table 3	5%
Data Table 4	10%
End questions	10%

Marks will be deducted in case if students have not completely and correctly filled the data tables.
Note that these marks are max in each category. We may assign less than the given percentage of marks in case students have not successfully completed all the requirements.
This lab is time constrained. Please note that you must finish your work and submitted duly filled handout to the lab engineer within given time.

LAB 05

IMPLEMENTATION OF XOR AND XNOR FUNCTIONS USING NAND GATES

Name:

Roll Number:

Date:

1. Objectives:

Having completed this experiment you will be able to:

- Implement XOR gates using NAND gates
- Implement XNOR gates using NAND gates

PART 1

2. Basic Information:

Digital circuits are more frequently constructed with NAND and NOR gates than with AND and OR gates. NAND and NOR gates are easier to fabricate with electronic components and are the basic gates used in all IC digital logic families. The graphic symbols for NAND, XOR, and XNOR gates together with their algebraic functions are given below:

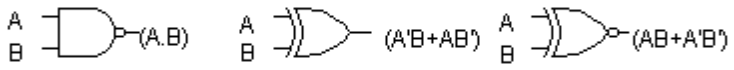


Figure 4.1: *Logic gates*

Truth Table for XOR gate:

Input A	Input B	Output F
0	0	0
0	1	1
1	0	1
1	1	0

The NAND logic diagram for XOR is obtained from Boolean function in the following way:

1. The implementation of a XOR function with NAND gates requires that the function be simplified in the sum of products form.
   $$F = A'B + AB' \qquad \text{equation. 2.1}$$
2. Draw a NAND gate for each product term of the function that has at least two literals. This constitutes a group of first level gates.

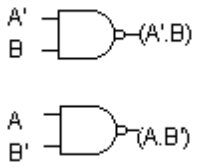


Figure 4.2: *First level gates*

3. Draw a single NAND gate within the second level, with inputs coming from the outputs of first-level gates.

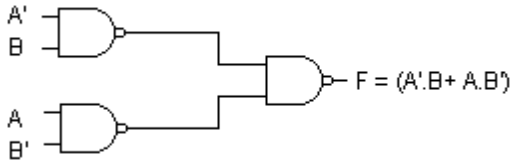


Figure 4.3: *Second level gates*

4. A two input NAND gate can be used as an inverter by applying logic 1 at one of the inputs.

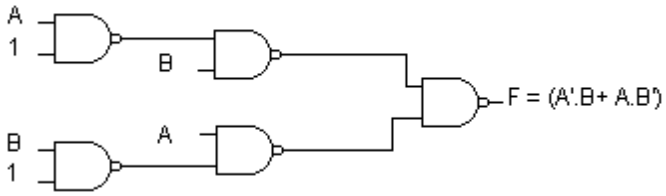


Figure 4.4: *NAND implementation of XOR gate*

3. Experimental Work:

3.1. Material Required:

- Logic Trainer
- Connecting Wires
- Components(IC's): 7400

3.2. Procedure:

It is clear from the logic diagram that the NAND gate implementation of XOR gate requires five NAND gates. You will need two quad- 2 in NAND gate ICs to perform this experiment. Gets the required number of ICs containing NAND gates and other apparatus from the lab attendant. Plug in the ICs in the breadboard of the Logic Trainer. Connect 5Vdc power supply and ground on pins 14 and 7 respectively. For other pin configuration consult the data sheet (we have already used NAND gates in the first lab so it should not be a problem). Wire your circuit according to the logic diagram for XOR gate as given above. Once you have wired the circuit, check it with your instructor and, if approved, power up your circuit. The outputs should be connected to the LEDs on the Logic Trainer for monitoring purpose. Apply different input combinations at the input and note down the outputs and fill in the following truth table. This truth table should confirm to the one given in theory.

4. EXPERIMENTAL RESULT

Fill in the following truth table in the presence of the lab instructor.

4.1. Truth Table for XOR Gate: (Details above)

Input A	Input B	Output F
0	0	
0	1	
1	0	
1	1	

4.2. Write Boolean function for XOR gate:

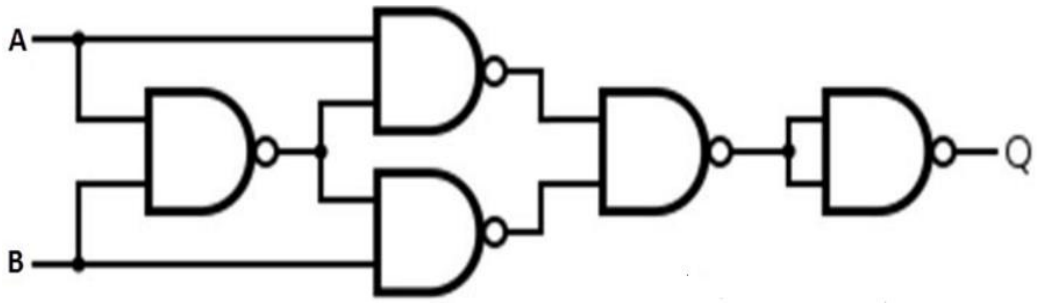
F = ----------

PART 2

1. Basic Information

Digital circuits are more frequently constructed with NAND and NOR gates than with AND and OR gates. NAND and NOR gates are easier to fabricate with electronic components and are the basic gates used in all IC digital logic families. The graphic symbols for NAND and XNOR gates together with their algebraic functions are given below:

If we observe the operation of XNOR gate, we can say that the XNOR gate output will be HIGH when both the inputs are not same and will become LOW for different combination of input. This we can see in truth table.



NAND implementation of XNOR gate

2. <u>Experimental Work:</u>

3.1. Material Required:

- Logic Trainer
- Connecting Wires

- Components(IC's): 7400

3.2. Procedure:

It is clear from the logic diagram that the NAND gate implementation of XNOR gate requires five NAND gates. You will need two quad- 2 in NAND gate ICs to perform this experiment. Gets the required number of ICs containing NAND gates and other apparatus from the lab attendant. Plug in the ICs in the breadboard of the Logic Trainer. Connect 5Vdc power supply and ground on pins 14 and 7 respectively. For other pin configuration consult the data sheet (we have already used NAND gates in the first lab so it should not be a problem). Wire your circuit according to the logic diagram for XOR gate as given above. Once you have wired the circuit, check it with your instructor and, if approved, power up your circuit. The outputs should be connected to the LEDs on the Logic Trainer for monitoring purpose. Apply different input combinations at the input and note down the outputs and fill in the following truth table. This truth table should confirm to the one given in theory.

3.3. EXPERIMENTAL RESULT

Fill in the following truth table in the presence of the lab instructor.

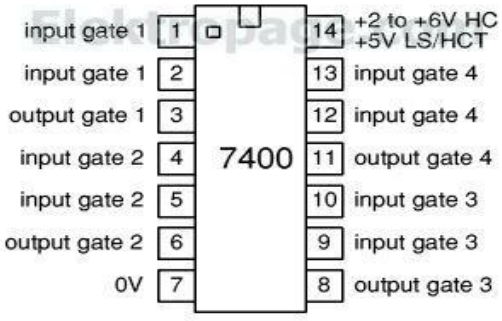
1. **Truth Table for XNOR Gate: (Details above)**

Input A	Input B	Output F
0	0	
0	1	
1	0	
1	1	

2. Write Boolean function for XNOR gate:

F = ----------

Pin Configuration



NAND IC Pin Configuration

Note: Every Student Must Submit Simulation on Logisim.