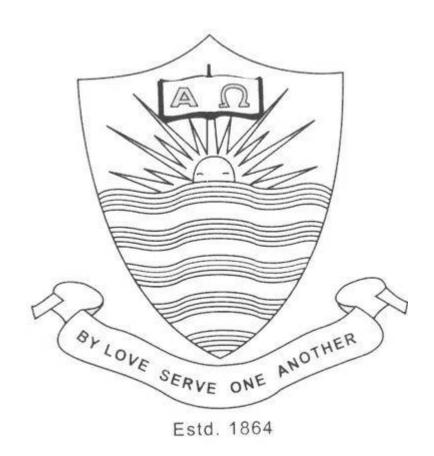
Department of Computer Science Forman Christian College

(A Chartered University)
Lahore



Digital Logic Design COMP 206

DIGITAL LOGIC DESIGN COMP 206 LAB 08- RUBRIX

DESCRIPTION	MARKS ALLOCATED
Attendance	5%
Proper handling of components, ICs and wiring	20%
Hardware wired completely(for all circuits)	30%
Expression	10%
Circuit Diagram	15%
Data Table 4	20%

Marks will be deducted in case if students have not completely and correctly filled the data tables.

Note that these marks are max in each category. We may assign less than the given percentage of marks in case students have not successfully completed all the requirements.

This lab is time constrained. Please note that you must finish your work and submitted duly filled handout to the lab engineer within given time.

LAB 08 IMPLEMENTATION OF A DECODER

Name:

Roll No:

Date:

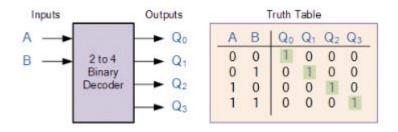
Learning Objectives:

By the end of this lab, you will be able to form a 2-to-4 binary decoder using basic AND, OR, NOT gates.

Background:

The name "Decoder" means to translate or decode coded information from one format into another, so a binary decoder transforms "n" binary input signals into an equivalent code using 2ⁿ outputs.

Binary Decoders are another type of digital logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an n-bit code, and therefore it will be possible to represent 2^n possible values. Thus, a decoder generally decodes a binary value into a non-binary one by setting exactly one of its n outputs to logic "1". Basic working of a 2—to-4 decoder is shown in the following figure:



TASK 1: Obtain expressions for the outputs

Q0, Q1, Q2 and Q3.

TASK 2: Obtain circuit diagram for this decoder

TASK 3: Implement this decoder on Logisim and record your results in the following table:

A	В	Q0	Q1	Q2	Q3
0	0				
0	1				
1	0				
1	1				