Department of Computer Science
Forman Christian College
(A Chartered University)
Lahore

Digital Logic Design
COMP 206

DIGITAL LOGIC DESIGN
COMP 206
LAB 02- RUBRIX

DESCRIPTION	MARKS ALLOCATED
Attendance	5%
Proper handling of components, ICs and wiring	20%
Hardware wired completely(for all circuits)	30%
Data table 1	10%
Data Table 2	10%
Data Table 3	5%
Data Table 4	10%
End questions	10%

Marks will be deducted in case if students have not completely and correctly filled the data tables.
Note that these marks are max in each category. We may assign less than the given percentage of marks in case students have not successfully completed all the requirements.
This lab is time constrained. Please note that you must finish your work and submitted duly filled handout to the lab engineer within given time.

LAB 02
WORKING WITH UNIVERSAL LOGIC GATES

Name:

Roll Number:

Date:

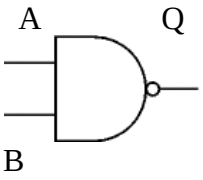
Objective:

After completion of this experiment Students shall be able to understand the behavior of logic NAND & NOR as the universal gates by obtaining the result like basic AND, OR, NOT gates.

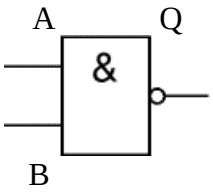
1. Basic Information of Universal Gates:

The NAND and the NOR gate can be said to be universal gates since combinations of them can be used to accomplish any of the basic operations and can thus produce an inverter, an OR gate or an AND gate. The non-inverting gates do not have this versatility since they can't produce an invert.

a. **NAND Gate**



Traditional symbol

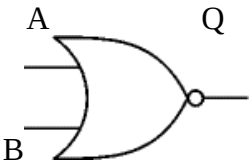


IEC symbol

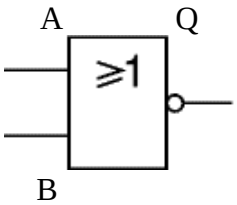
Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

b. NOR Gate:



Traditional symbol



IEC symbol

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

2. Experimental Work :

This Experiment has two parts.

Part-1: ***Working with NAND Gate***
Part-2: ***Working with NOR Gate***

Material Required

- Logic Trainer
- Connecting wires
- Components: 7402, 7400

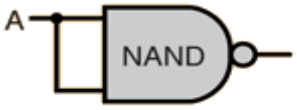
Procedure:

- Install the ICs on trainer's breadboard.
- Wire the pins 14 &7 of IC's to +5v and GND respectively.
- Wire the circuit according to the diagrams provided in step 4.1 & 4.3 for NAND and NOR gates.
- Mention the input as "A" "B" and output as A', A+B, and AB with respective logic circuit.
- Write down the results of Boolean expression of the interconnected gates at step 4.2, 4.4 with respect to the basic logic gates in the table provided.

3. EXPERIMENTAL RESULTS

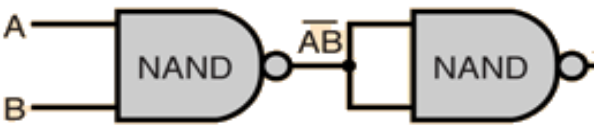
Working with NAND Gate

1. Implement the following circuit & obtain the Truth table and expression for the output



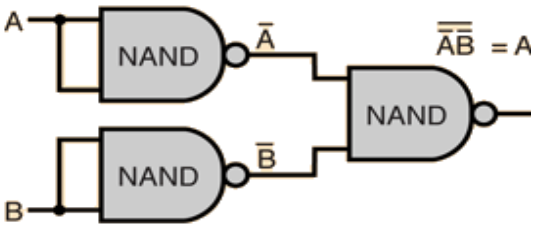
A	Out
0	
1	

2. Implement the following circuit & obtain the Truth table and expression for the output



A	B	Out
0	0	
0	1	
1	0	
1	1	

3. Implement the following circuit & obtain the Truth table and expression for the output



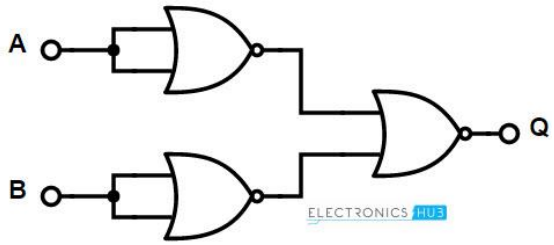
A	B	Out
0	0	
0	1	
1	0	
1	1	

Working with NOR Gate

1. Implement the following circuit & obtain the Truth table and expression for the output

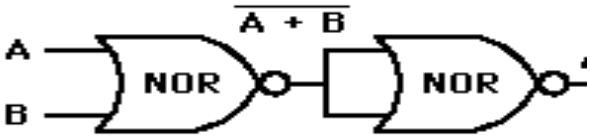
A	Out
0	
1	

2. Implement the following circuit & obtain the Truth table and expression for the output



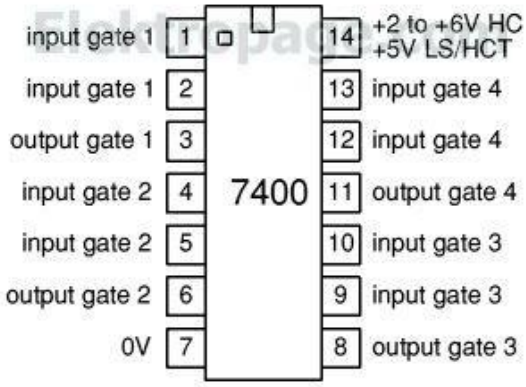
A	B	Out
0	0	
0	1	
1	0	
1	1	

3. Implement the following circuit & obtain the Truth table and expression for the output

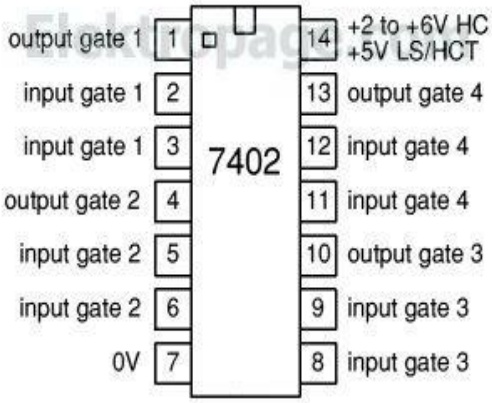


A	B	Out
0	0	
0	1	
1	0	
1	1	

Pin Configurations



NAND IC Pin Configuration



NOR IC pin Configuration

Note: Online Students must simulate circuit on Logisim.