Department of Computer Science
Forman Christian College
(A Chartered University)
Lahore

Digital Logic Design
COMP 206

DIGITAL LOGIC DESIGN

COMP 206

LAB 6- RUBRIX

DESCRIPTION	MARKS ALLOCATED
Attendance	5%
Proper handling of components, ICs and wiring	20%
Hardware wired completely(for all circuits)	30%
Data table 1	10%
Data Table 2	10%
Data Table 3	5%
Data Table 4	10%
End questions	10%

Marks will be deducted in case if students have not completely and correctly filled the data tables.
Note that these marks are max in each category. We may assign less than the given percentage of marks in case students have not successfully completed all the requirements.
This lab is time constrained. Please note that you must finish your work and submitted duly filled handout to the lab engineer within given time.

LAB 06
IMPLEMENTATION OF HALF ADDER & FULL ADDER

Name:

Roll Number:

Date:

1. Objectives:

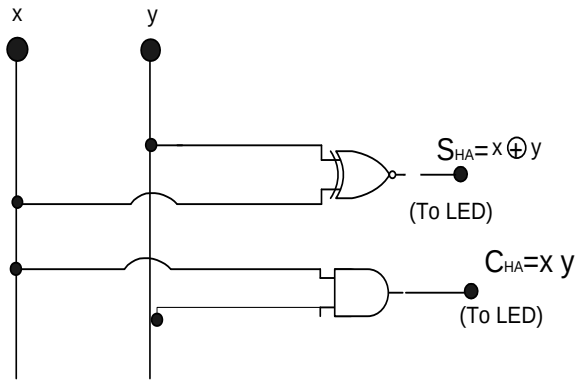
Having completed this experiment you will be able to

- Understand the use of logic gates in arithmetic operations.
- Understand the addition of two binary digits using. Logic circuit as a half adder.
- Understand the performance of combinational circuit that performs the addition of three bits (two significant bits and a previous carry) called a full-adder.

2. Basic Information:

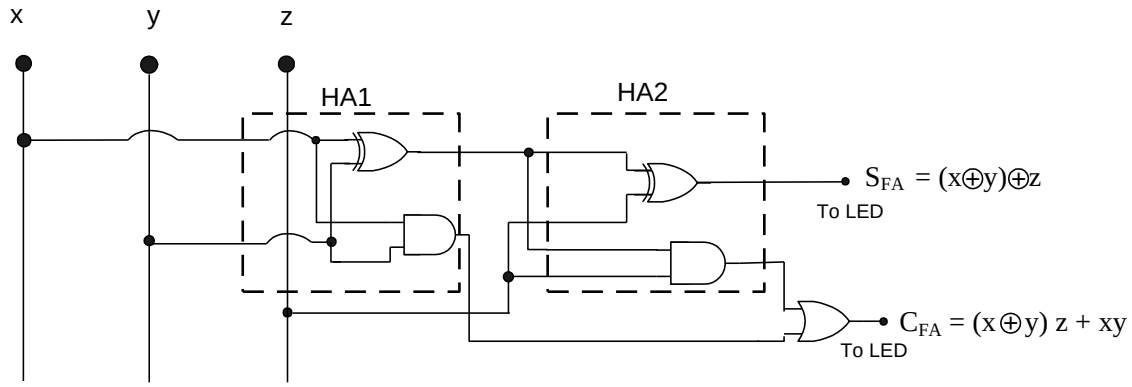
2.1.Half Adder:

Half Adder is combinational logic circuit that generates the sum of two binary numbers (each having 1 bit length). The logic circuit has two inputs and two outputs i.e. Sum & Carry.



2.2.Full Adder:

Full Adder is combination logic circuit that performs the sum of 3 input binary numbers, (each having 1 bit length). Two of the binary input variables are x and y represent the two significant bits to be added the third input z, represents the carry from previous lower significant position. Outputs of Full Adder are Sum and Carry represented as S_{FA} and C_{FA} respectively.



3. Experimental Work

3.1.Material Used:

- Connecting wires
- Logic Trainer
- Components: 7432 (OR), 7408 (AND), 7486 (XOR)

3.2.Procedure:

- Wire the circuit according to the pins supply indicator i.e. +5v to pin number 7, 14 respectively.
- Interconnect the basic logic gates as per logic diagrams given for half adder and full-adder
- Implement the given Boolean expression by basic logic gates, verify and write the result in the truth table

3.3.Experimental Results

Truth Table

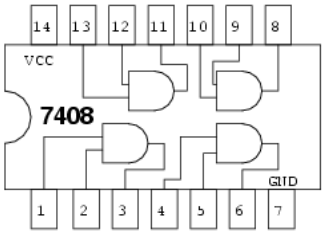
Inputs		Output	
X	**Y**	$S_{HA} = x'y+xy'$	$C_{HA} = x\ y$
0	0		
0	1		
1	0		
1	1		

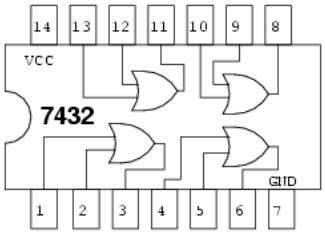
Truth Table

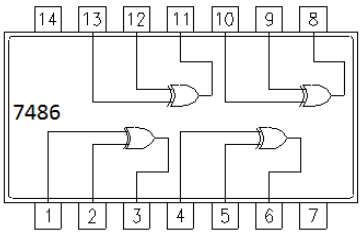
i/p's			o/p's			
			S_{FA}		C_{FA}	
x	**Y**	**z**	**Actual**	**Observed**	**Actual**	**Observed**
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

3.4.Obtain the expressions for Half adder and Full adder (both sum & carry).

4. Pin Configuration







5. In Case of Trouble:

- Check the power supply.
- Check the Vcc and GND at pin number 14 and 7 of the IC under test.
- Check all the wire connections and remove the breaks.
- Check the IC under test using truth table.