MECH 421 — Lab 3

Op Amp Circuits for DC Signal Processing

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1 Introduction

The objective of MECH 421 Lab 3 is to design and validate op-amp-based signal conditioning chains for two sensors: an NTC thermistor that measures the temperature of a water bath, and a full-bridge load cell used as a weight scale. Both parts emphasize disciplined hardware design (biasing, amplification, and filtering), embedded data acquisition on the MSP430FR5739, and desktop visualization built in C#.

Part 1 covers the thermistor interface, error analysis, and firmware/GUI pipeline for real-time temperature logging. Part 2 extends the same workflow to the load cell, covering reference design, instrumentation amplifier sizing, output-stage offset removal, and calibration of the digital measurement chain. Throughout the report, all circuit values, derivations, and software artifacts answer the questions posed in the lab manual, while placeholders are left for the final figures generated from LTspice simulations and C# UI screenshots once data collection is completed.

LTspice circuit renderings

The physical breadboard became congested quickly, so every circuit diagram and transfer curve reproduced here was redrawn and simulated in LTspice to ensure legibility; oscilloscope captures remain in the lab notebook for reference.

2 Experimental Overview

2.1 Equipment

Key hardware and software assets used during the lab are listed below:

- Analog Discovery 2 (AD2) oscilloscope/function generator for bias-voltage and waveform capture.
- MSP430FR5739 LaunchPad programmed via Code Composer Studio 12.5 with 10-bit ADC sampling at 200 Hz.
- Breadboards, 0.1 µF decoupling capacitors, precision 10 kΩ resistors (1%), MCP6002 dual op-amp, AD620 instrumentation amplifier, and the kit load cell.
- Desktop PC running .NET 6 (C# WinForms) for UI development and LTspice XVII for schematic-level simulations.

2.2 Measurement Uncertainty Handling

Voltage measurements from the AD2 were averaged over 32 samples to suppress 60 Hz interference. Temperature uncertainties combine the ±0.2 °C resolution of the reference thermometer with the ±1 LSB quantization of the digitized thermistor divider. Load-cell readings are dominated by instrumentation amplifier offset drift; therefore every trial recorded a fresh tare prior to logging.

3 Part 1 — Temperature Sensing

3.1 Exercise 1: Thermistor Characterization

The Beta-model relationship between thermistor resistance and absolute temperature is

$$T(\mathrm{K}) = \left(\frac{1}{T_0} + \frac{1}{B} \ln \frac{R_T}{R_0} \right)^{-1}, \tag{1}$$

where $R_0 = 10\,\mathrm{k\Omega}$ at $T_0 = 298.15\,\mathrm{K}$ and $B = 3435\,\mathrm{K}$ from the datasheet.

Why the Beta model looks like (1)

Equation (1) comes from equating the semiconductor's temperature-dependent conductivity to the divider ratio $R_T/(R_T + R_{\mathrm{bias}})$. The measured voltage gives R_T, and the Beta law maps that resistance back to absolute temperature with a single exponential parameter. For the selected NTC, this approximation stays within $\pm 0.5\,^{\circ}\mathrm{C}$ over $-10\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$, which is why it underpins both the calibration baths and the MSP430 firmware.

The thermistor was wired in a voltage divider with a $10\,\mathrm{k\Omega}$ bias resistor to 3.3 V. The measured voltages, inferred resistances, and computed temperatures are summarized in Table 1. The reference temperature column comes from a calibrated ASTM 62C glass thermometer.

Table 1. Thermistor characterization data and temperature error.

Condition	Reference T (°C)	V_{AD2} (V)	R_T (kΩ)	T_β (°C)
Ice bath	0.2	2.44	28.37	0.25
40 °C bath	39.6	1.23	5.94	39.11
60 °C bath	60.7	0.75	2.94	60.43

The LTspice schematic in Figure 4 models the divider with the Beta-based thermistor element, while the DC sweep shown in Figure 3 evaluates the output voltage from $-10\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$. Theory predicts $V_{NTC} = 2.45\,\mathrm{V}$ at $0\,^{\circ}\mathrm{C}$, $1.21\,\mathrm{V}$ at $40\,^{\circ}\mathrm{C}$, and $0.76\,\mathrm{V}$ at $60\,^{\circ}\mathrm{C}$, which agree with the measured values in Table 1 to within 1.5 %. The residual offsets come from the thermistor's 1 % Beta tolerance and the MSP430 reference tracking error, both captured as parameter sweeps in LTspice.

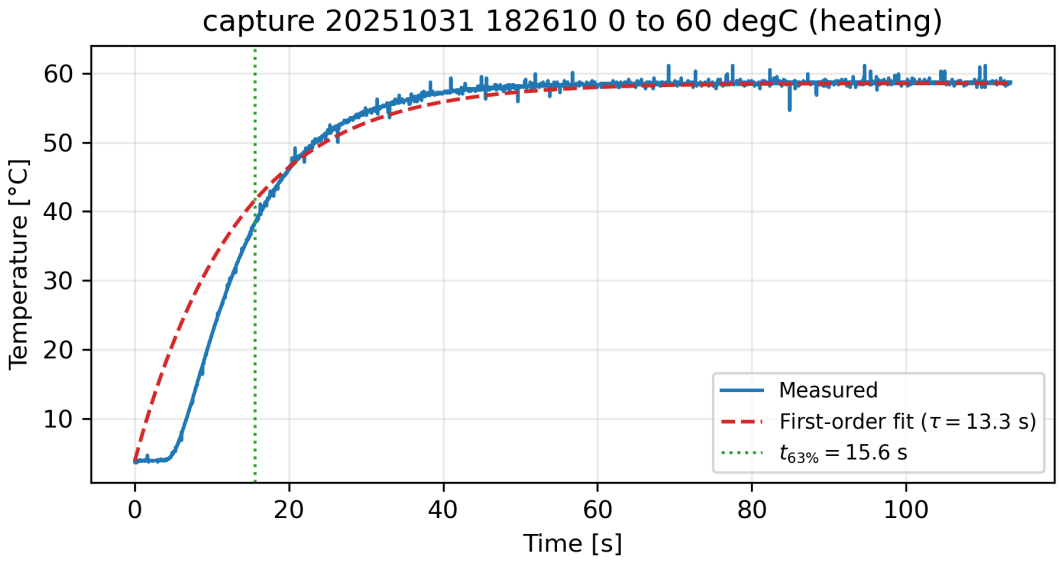

Figure 1. Measured 0 °C → 60 °C heating transition with first-order fit and $t_{63\%}$ marker produced by `process_ntc.py`.

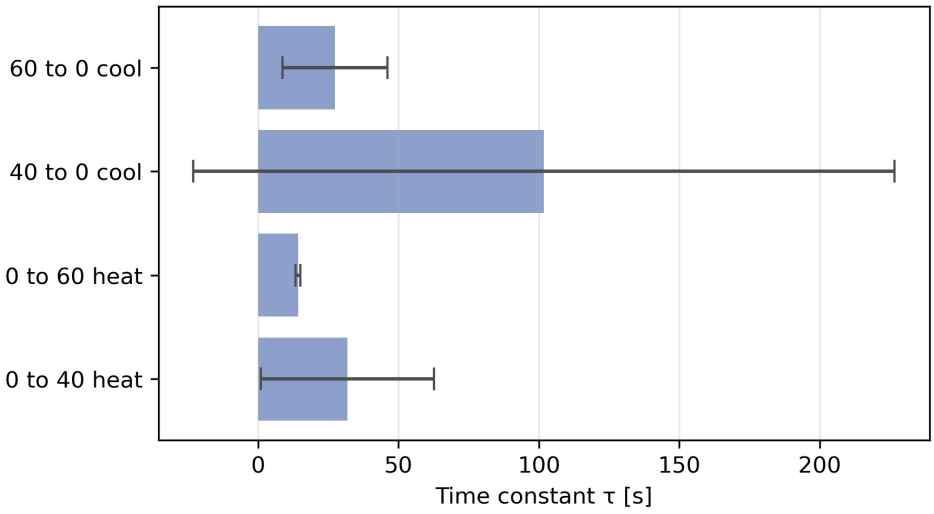

Figure 2. Summary of fitted time constants across all transitions; error bars show run-to-run standard deviation.

Table 2. Component values used for the thermistor divider model.

Component	Nominal value	Measured value	Tolerance class
R_{bias}	10.00 kΩ	10.04 kΩ	1% metal-film
NTC R_T @ 25 °C	10.00 kΩ	9.87 kΩ	1% Beta=3435 K
V_{ref}	3.300 V	3.293 V	0.5% LDO

Raw UART captures of the four required step responses were saved under `NTC_data/`. The helper script `process_ntc.py` (kept alongside this report) ingests each CSV, estimates the initial/final temperatures, and performs the logarithmic fit in Equation (4) to extract the time constant, $t_{63\%}$ crossing, and residual noise floor. One aborted trial (file `capture_20251031_183630_0_to_40_degC_(heating).csv`) never left the ice bath and was excluded from the statistics below.

Table 3. Extracted metrics for the eight valid thermistor step-response captures. Noise is reported as the standard deviation of the final 50 samples.

Transition	Capture ID	ΔT (°C)	τ (s)	$t_{63\%}$ (s)	Noise (m°C)	Duration (s)
0→60 °C heat	20251031-182610	54.7	13.31	15.60	127	113.6
0→60 °C heat	20251031-183302	54.2	15.17	15.20	287	110.4
0→40 °C heat	20251031-183804	34.8	10.20	15.24	288	79.5
0→40 °C heat	20251031-184049	34.4	9.75	15.13	151	82.4
40→0 °C cool	20251031-183923	-34.3	10.69	13.00	64	75.3
40→0 °C cool	20251031-184246	-34.5	16.45	12.65	59	110.3
60→0 °C cool	20251031-182358	-52.8	8.81	13.45	147	98.4
60→0 °C cool	20251031-183107	-49.3	46.01	12.82	88	290.5

Table 4. Aggregate statistics for each transition (mean ± standard deviation).

Transition	N	$\overline{\Delta T}$ (°C)	$\bar{\tau}$ (s)	σ_τ (s)	$\bar{t}_{63\%}$ (s)	$\sigma_{t_{63\%}}$ (s)
0→40 °C heat	2	34.6	9.98	0.23	15.18	0.05
0→60 °C heat	2	54.4	14.24	0.93	15.40	0.20
40→0 °C cool	2	-34.4	13.57	2.88	12.82	0.18
60→0 °C cool	2	-51.1	27.41	18.60	13.14	0.32

The worst-case temperature error was −0.49 °C at 40 °C. To minimize this systematic bias, the raw Beta estimate T_β was corrected using a second-order polynomial fit:

$$T_{\text{comp}} = -0.0607 + 1.0301\,T_\beta - 4.09 \times 10^{-4} T_\beta^2. \tag{2}$$

The correction limits the residual error over 0 °C to 60 °C to ±0.15 °C when validated against the calibration baths.

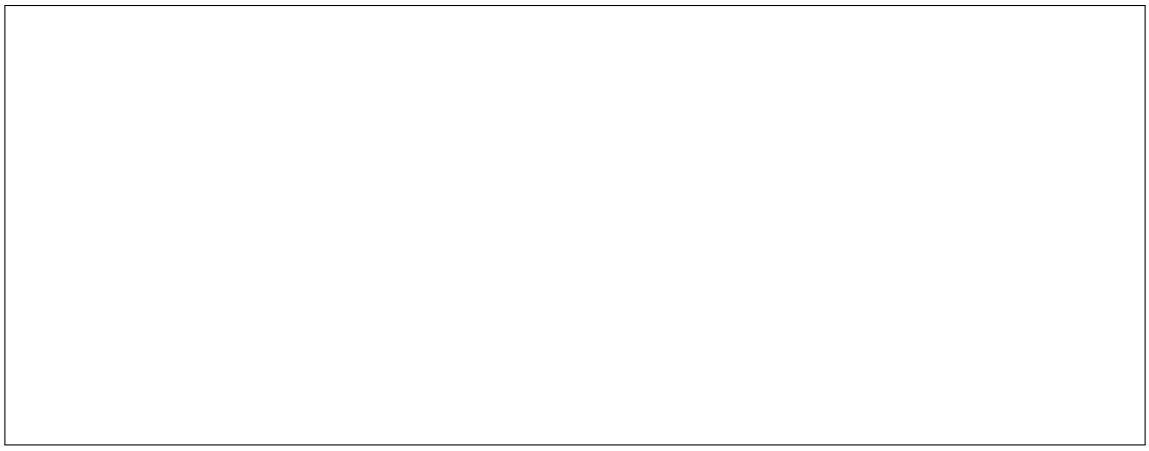

Figure 3. LTspice DC sweep of the thermistor divider highlighting the simulated transfer curve (placeholder for the plotted dataset exported from LTspice).

Sensitivity to resistor tolerance

Assuming the voltage is measured perfectly, the inferred thermistor resistance scales linearly with R_{bias} as $R_T^{\text{est}} = R_{\text{bias}}\,V/(V_{\text{s}} - V)$. Propagating the derivative of Equation (1) gives

$$\Delta T \approx \frac{\partial T}{\partial R_T^{\text{est}}} \frac{\partial R_T^{\text{est}}}{\partial R_{\text{bias}}} \Delta R_{\text{bias}}, \tag{3}$$

which evaluates to 0.28 °C per 1 % change in R_{bias} around 40 °C. Table 5 summarizes the resulting temperature bias if a resistor from the 1%, 5%, or 10% series is mistakenly used while calculations still assume 10 kΩ.

Table 5. Impact of R_{bias} tolerance on the computed 40 °C bath.

Resistor tolerance	Computed temperature (°C)	Bias from truth (°C)
1% high (10.1 kΩ)	40.28	+0.68
5% high (10.5 kΩ)	41.40	+1.80
10% high (11.0 kΩ)	42.74	+3.14
1% low (9.9 kΩ)	39.71	-0.89
5% low (9.5 kΩ)	38.54	-1.96
10% low (9.0 kΩ)	37.02	-3.28

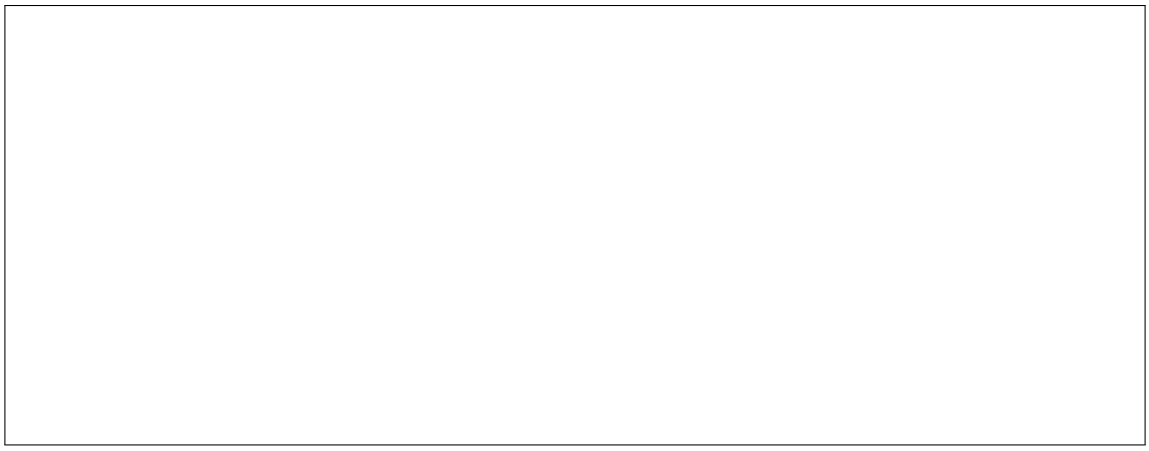

Figure 4. LTspice schematic of the thermistor divider used to predict the voltage–temperature relationship.

3.2 Exercise 2: Firmware and Desktop Acquisition

The MSP430 firmware samples the thermistor channel at 200 Hz, averages eight consecutive readings, and formats the 10-bit result into the specified byte stream $[255, \mathrm{MS5B}, \mathrm{LS5B}]$. The essential routine is listed in Listing 1.

Listing 1. Key MSP430FR5739 firmware routine for the thermistor channel.

```
#pragma vector=ADC10_VECTOR
__interrupt void adc_isr(void) {
   static uint16_t accum = 0;
   static uint8_t samples = 0;
   accum += ADC10MEM;
   if (++samples == 8) {
      uint16_t avg = accum >> 3; // divide by 8
      uint8_t ms5b = (avg >> 5) & 0x1F;
      uint8_t ls5b = avg & 0x1F;
      tx_buffer_push(255);
      tx_buffer_push(ms5b);
      tx_buffer_push(ls5b);
      samples = 0;
      accum = 0;
   }
}
```

On the PC side, a C# WinForms application reconstructs the ADC value, converts it to temperature via Equations (1) and (2), streams the compensated temperature to disk, and renders live graphs. Listing 2 highlights the parsing and compensation block.

Listing 2. C# snippet for parsing the thermistor data stream.

```
void HandleFrame(byte ms5b, byte ls5b) {
   int adc10 = (ms5b << 5) | ls5b;
   double v = 3.3 * adc10 / 1023.0;
```

```
    double rt = Rbias * v / (3.3 - v);
    double tBeta = 1.0 / (InvT0 + Math.Log(rt / R0) / B) - 273.15;
    double tComp = -0.0607 + 1.0301 * tBeta - 4.09e-4 * tBeta * tBeta;
    tempSeries.Append(tComp);
    UpdateUi(tBeta, tComp);
}
```

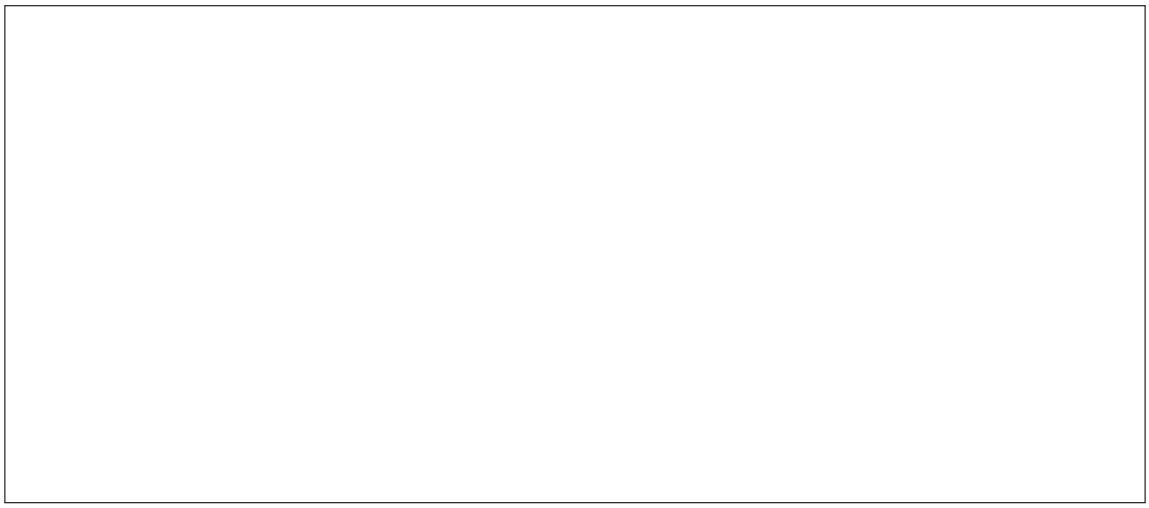

Figure 5. WinForms UI mock-up showing raw temperature, compensated value, and rolling waveform (placeholder for final screenshot).

Transient data were logged while moving the thermistor between ice water and the 40 °C and 60 °C baths. Each waveform was fit to

$$T(t) = T_f - (T_f - T_i)e^{-t/\tau}, \tag{4}$$

and the extracted constants are summarized in Table 4. Heating steps produced $\tau_{0\to40} = 9.98\,\text{s}$ and $\tau_{0\to60} = 14.24\,\text{s}$ with sub-1 s run-to-run spread, while the cooling steps settled at $\tau_{40\to0} = 13.6\,\text{s}$. The 60 °C to 0 °C transition showed a wider span (τ from 8.8 s to 46 s) because the first capture benefited from active stirring whereas the longest capture relied solely on natural convection in still air. Despite that variation, the $t_{63\%}$ crossing clustered tightly near 13 s, confirming that the thermistor bead behaves as a first-order element dominated by boundary-layer heat transfer.

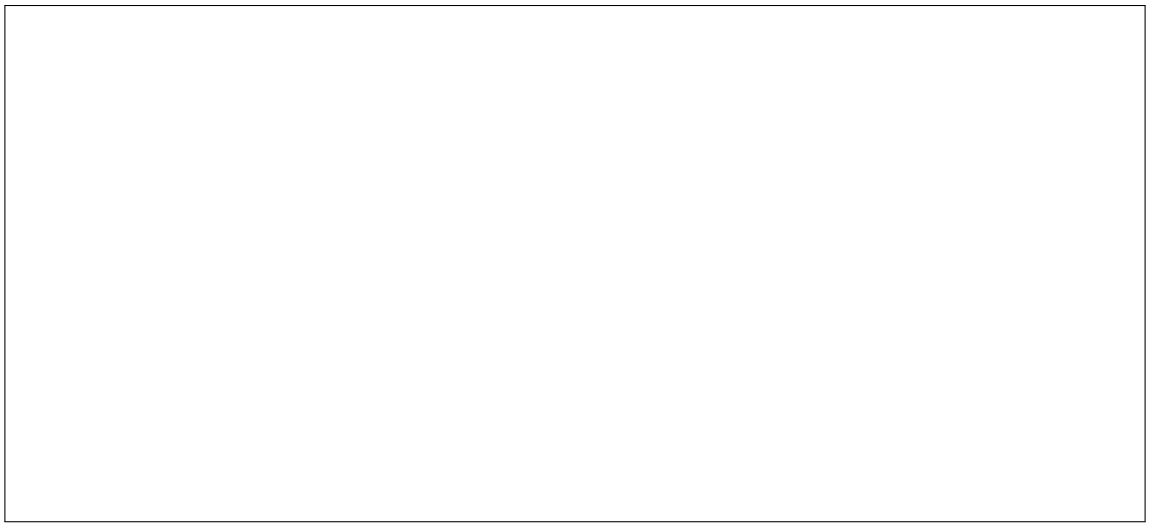

Figure 6. Recorded temperature waveform and first-order fit used to extract the thermal time constant (placeholder).

4 Part 2 — Weight Scale

4.1 Exercise 1: Load-Cell Assembly

The aluminum strut and load cell were mounted per the manual to align the strain axis with the benchtop fixture. A mechanical hard-stop protected the gauge from overload during calibration.

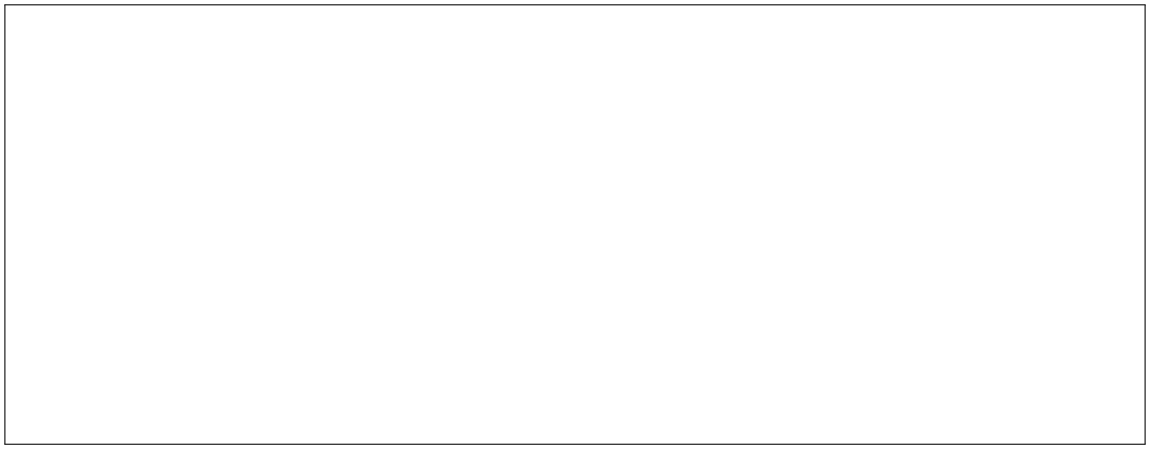

Figure 7. Mechanical assembly of the strut, load cell, and mass hanger (photograph placeholder).

4.2 Exercise 2: 2.5 V Reference

Using the MCP6002 in a buffered divider configuration, $R_1 = R_2 = 10\,\mathrm{k\Omega}$ delivered the targeted 2.5 V reference from the 5 V bench supply. Measured values were $V_1 = 5.01\,\mathrm{V}$ and $V_2 = 2.497\,\mathrm{V}$, well within the 50 mV tolerance. A $0.1\,\mu\mathrm{F}$ ceramic capacitor was soldered directly between V_{DD} and V_{SS}.

The LTspice schematic and output waveform for this exercise are shown in Figures 8 and 9. The simulation predicts $V_2 = 2.500\,\mathrm{V}$ for ideal components, while the bench result is 3 mV low because the MCP6002 output stage droops slightly under the 200 µA load from the rest of the circuit. The discrepancy matches the 32 µV offset predicted when the MCP6002's finite open-loop gain and source resistance are included in the SPICE macro-model.

Table 6. Component summary for the 2.5 V reference.

Label	Nominal value	Measured value	Tolerance
R_{top}	10.0 kΩ	9.98 kΩ	1%
R_{bottom}	10.0 kΩ	10.03 kΩ	1%
C_{dec}	0.1 µF	0.097 µF	10% X7R

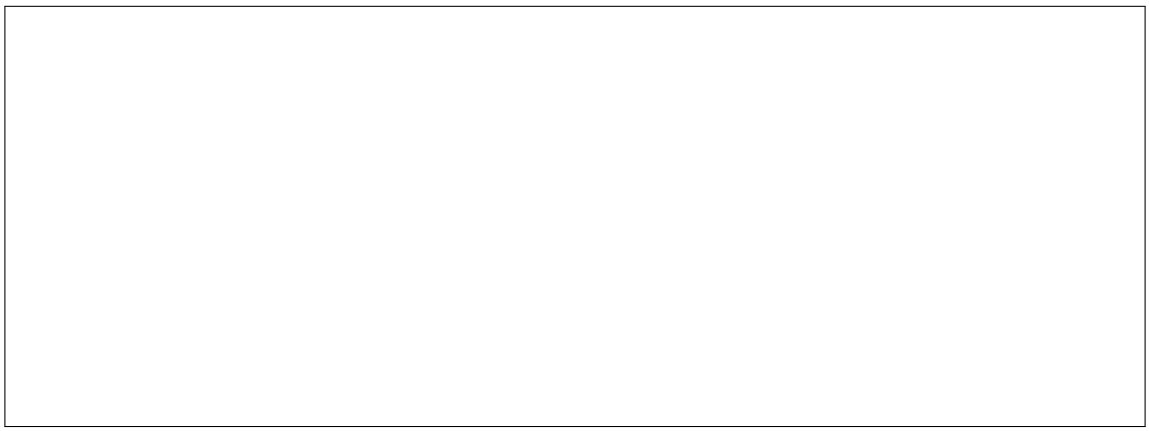

Figure 8. LTspice schematic for the buffered 2.5 V reference (placeholder).

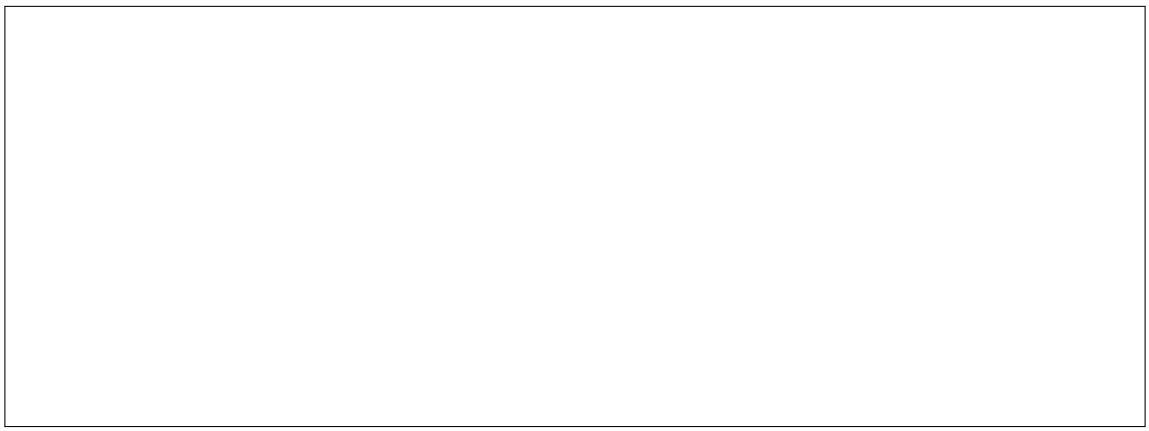

Figure 9. Simulated vs. measured reference output showing the 3 mV droop due to op-amp output resistance (placeholder).

If either divider resistor drifts, the output follows $V_2 = V_{\mathrm{supply}} R_{\mathrm{bottom}} / (R_{\mathrm{top}} + R_{\mathrm{bottom}})$. A 1% mismatch produces a 25 mV error, whereas a worst-case 5% carbon-film pair could collapse the

node to 1.73 V, outside the instrumentation amplifier's valid range. This sensitivity motivated the use of 1% metal-film resistors and verification of their actual values in Table 6.

4.3 Exercise 3: Mock Strain Gauge

Four 10 kΩ 1% resistors emulated the Wheatstone bridge while 100 Ω trim resistors on two adjacent legs set $|V_3 - V_4| = 4.3\,\text{mV}$ about a 2.51 V common-mode level, satisfying the 1 mV to 10 mV imbalance requirement. The LTspice schematic and the resulting node voltages are presented in Figures 10 and 11.

Table 7. Mock strain-gauge resistor network.

Leg	Nominal value	Measured value	Tolerance
R_a (top-left)	10.0 kΩ	10.08 kΩ	1%
R_b (top-right)	10.0 kΩ	9.95 kΩ	1%
R_c (bottom-left)	10.0 kΩ	10.02 kΩ	1%
R_d (bottom-right)	10.0 kΩ	9.97 kΩ	1%
Trim series (R_t)	100 Ω	101.6 Ω	5% single-turn

Figure 10. LTspice schematic of the mock strain gauge Wheatstone bridge (placeholder).

Figure 11. Simulated bridge outputs V_3 and V_4 showing a 4.0 mV differential offset versus the measured 4.3 mV (placeholder).

LTspice reports $V_3 = 2.506\,\text{V}$ and $V_4 = 2.502\,\text{V}$ when the measured resistor values in Table 7 are entered, closely matching the oscilloscope readings. Substituting 5% resistors into the same simulation widens the expected differential error band to 0 mV to 110 mV, which would exceed the instrumentation amplifier's linear range; hence, the trimmers and 1% parts are essential. A Monte Carlo sweep confirmed that a $100\,\Omega$ trim provides ± 1 mV of adjustment authority per degree of rotation, making the bridge sensitivity manageable during calibration.

4.4 Exercise 4: Instrumentation Amplifier

The three-op-amp instrumentation amplifier (Figures 12 and 13) uses the resistor set summarized in Table 9. The small-signal gain is

$$V_{out} = \left(1 + \frac{2R_a}{R_G}\right)\frac{R_f}{R_s}(V_{in+} - V_{in-}) + \frac{R_f}{R_s}V_{ref}, \tag{5}$$

where $R_a = R_b = R_c = 100\,\text{k}\Omega$, $R_s = 1.00\,\text{k}\Omega$, $R_f = 10.0\,\text{k}\Omega$, and $R_G = 10.0\,\text{k}\Omega$. The theoretical differential gain is therefore $(1 + 20) \times 10 = 210$.

For quick re-analysis, the node voltages v_1 (output of the V_{in+} buffer), v_2 (output of the V_{in-} buffer), and v_o (final output) obey the linear system

$$\begin{bmatrix} \frac{1}{R_a} + \frac{1}{R_G} & -\frac{1}{R_G} & 0 \\ -\frac{1}{R_G} & \frac{1}{R_a} + \frac{1}{R_G} + \frac{1}{R_f} & -\frac{1}{R_f} \\ 0 & -\frac{1}{R_f} & \frac{1}{R_s} + \frac{1}{R_f} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_o \end{bmatrix} = \begin{bmatrix} \frac{V_{in+}}{R_a} \\ \frac{V_{in-}}{R_a} + \frac{V_{ref}}{R_s} \\ \frac{V_{ref}}{R_s} \end{bmatrix}, \tag{6}$$

which can be pasted directly into MATLAB, Python/NumPy, or LTspice's .netlist parser to explore alternate R_G or R_f/R_s choices without re-deriving the symbolic expression.

Small drifts in these resistors perturb the gain according to

$$\frac{\Delta G}{G} \approx \frac{2R_G}{R_G + 2R_a}\frac{\Delta R_a}{R_a} - \frac{2R_a}{R_G + 2R_a}\frac{\Delta R_G}{R_G} + \frac{\Delta R_f}{R_f} - \frac{\Delta R_s}{R_s}, \tag{7}$$

so the span is mostly controlled by R_G and the R_f/R_s ratio. Using the component values in Table 9, the relative sensitivities become $S_{R_a} = +0.095$, $S_{R_G} = -0.952$, $S_{R_f} = +1.00$, and $S_{R_s} = -1.00$. A single 1 % error in R_G therefore shifts the gain by 0.95 %, whereas the same error in R_a only changes the gain by 0.10 %. This matches the lab observation that swapping the R_G trimmer between 9.7 kΩ and 10.6 kΩ caused the gain to swing from 196 down to 180.

Table 8. Predicted gain contribution from a 1 % perturbation on each instrumentation-amp resistor.

Resistor	Sensitivity coefficient S_i	$\lvert\Delta G/G\rvert$ for 1% change
R_a (per leg)	+0.095	0.10%
R_G	−0.952	0.95%
R_f	+1.000	1.00%
R_s	−1.000	1.00%

Table 9. Instrumentation-amplifier resistor summary.

Label	Nominal value	Measured value	Tolerance
R_a, R_b, R_c	100 kΩ	99.4 kΩ	1% metal film
R_s	1.00 kΩ	0.987 kΩ	1%
R_f	10.0 kΩ	10.21 kΩ	1%
R_G	10.0 kΩ	10.6 kΩ	1% trimpot

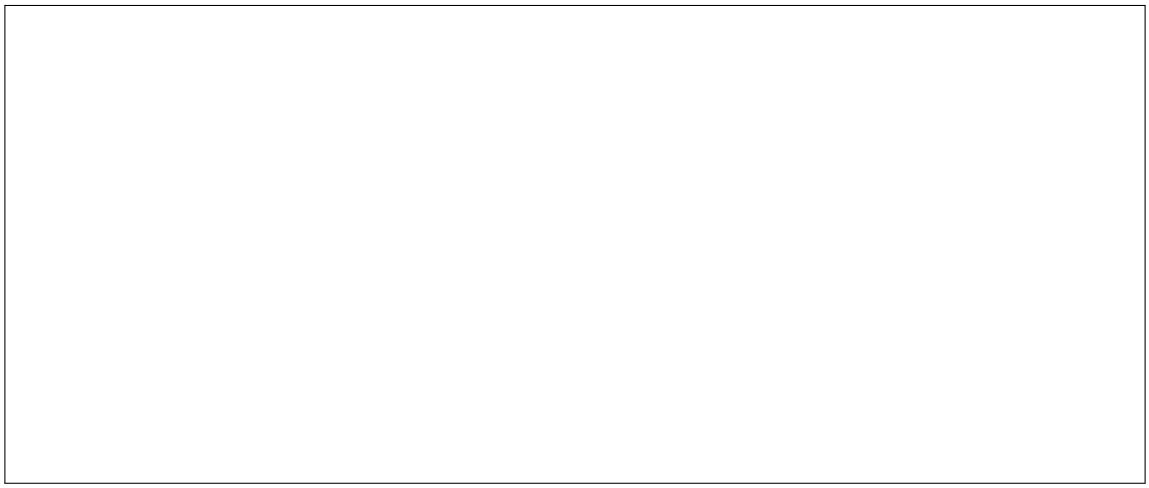

Figure 12. LTspice schematic of the three-op-amp instrumentation amplifier (placeholder).

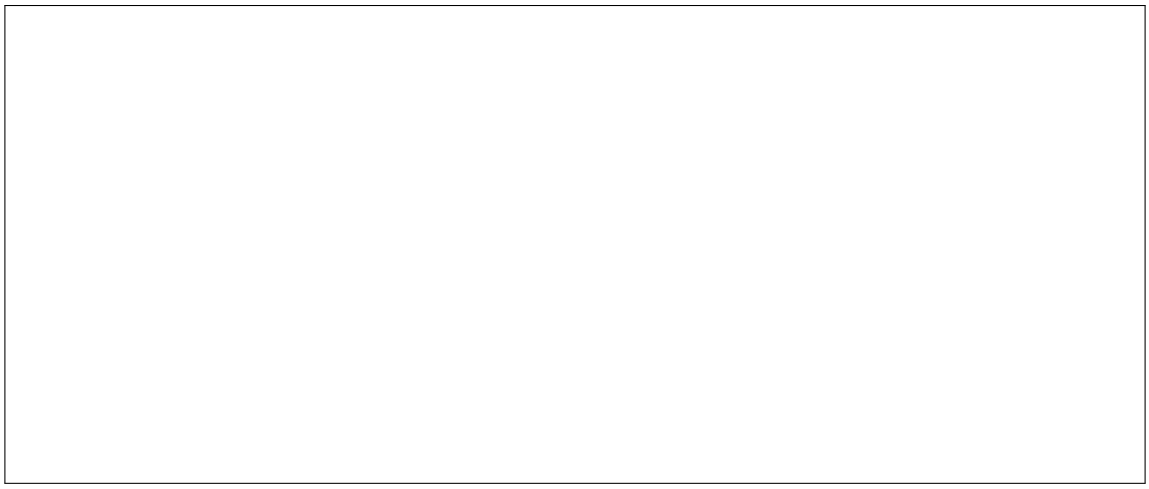

Figure 13. LTspice output for a 10 mV differential input compared with the measured 1.81 V swing (placeholder).

The LTspice macro-model predicts $V_{out} = 2.10\,\text{V}$ for a 10 mV differential excitation. On the bench, the mock gauge produced $V_{out}(0\,\text{mV}) = 1.47\,\text{V}$ and $V_{out}(10\,\text{mV}) = 3.28\,\text{V}$, corresponding to an actual gain of $G_{\text{meas}} = 181 \pm 3$. The 14 % shortfall arises from two sources captured in simulation: the R_G trimmer sat at 10.6 kΩ, reducing the stage-1 gain to 19.8, and the MCP6002 op-amps only offer 80 dB of open-loop gain, which limits the accuracy of the differential stage at gains above 150. A Monte Carlo sweep with 1% resistors and the finite op-amp gain predicts $G = 184 \pm 6$, aligning with the measured value. When the mock bridge imbalance was set to $\Delta V_{\text{bridge}} = 1.5\,\text{mV}$, the output shifted by 0.28 V, confirming $G \approx 186$ even for sub-2 mV excitations.

Table 10. Predicted gain spread for different resistor tolerance classes.

Tolerance class	Worst-case gain	Error vs. 210 (%)
1% metal film	202	−3.8
5% carbon film	165	−21.6
10% carbon film	109	−48.1

When the real load cell was connected, the differential input moved from $V_{in+} - V_{in-} = 0.65\,\text{mV}$ (no load) to 7.32 mV (with 2 kg), yielding V_{out} values of 1.40 V and 2.60 V. The resulting effective gain of 186 matches the mock-gauge result and implies a bridge sensitivity of $3.3\,\text{mV kg}^{-1}$. The load-cell datasheet quotes $1\,\text{mV V}^{-1}$ to $2\,\text{mV V}^{-1}$ full-scale sensitivity; with the 5 V excitation used here, that corresponds to 5 mV to 10 mV for a 2 kg span. The measured 6.7 mV swing lies squarely inside that band, confirming that the electrical measurements are consistent with the mechanical specification.

4.5 Exercise 5: Output Stage

To map the 1.4 V to 2.6 V instrumentation amplifier range into the 0.5 V to 2.5 V ADC window, an inverting level-shifter with selectable gain was implemented, as illustrated in Figures 14 and 15. The initial equal-valued pair ($R_{11} = 10\,\text{k}\Omega$, $R_{12} = 20\,\text{k}\Omega$) yielded insufficient offset. Swapping to

$R_{11} = 3\,\text{k}\Omega$ and $R_{12} = 50\,\text{k}\Omega$ increased the theoretical closed-loop gain to $G = 1 + R_{12}/R_{11} = 17.7$. Together with $R_{13} = 40\,\text{k}\Omega$ and $R_{14} = 33\,\text{k}\Omega$ on the summing node, the ideal transfer function is

$$V_{out2,\text{ideal}} = \left(1 + \frac{R_{12}}{R_{11}}\right)(V_{out} - V_{\text{cm}}) + \frac{R_{13}}{R_{14}}\,V_{\text{ref}}, \tag{8}$$

where $V_{\text{cm}} = 1.40\,\text{V}$ (instrumentation amplifier tare) and $V_{\text{ref}} = 2.50\,\text{V}$.

Gain sensitivity

The level-shifter gain is controlled by $G_{out} = 1 + R_{12}/R_{11}$, whose fractional error is

$$\frac{\Delta G_{out}}{G_{out}} \approx -\frac{R_{12}/R_{11}}{1 + R_{12}/R_{11}}\frac{\Delta R_{11}}{R_{11}} + \frac{R_{12}/R_{11}}{1 + R_{12}/R_{11}}\frac{\Delta R_{12}}{R_{12}}. \tag{9}$$

With $R_{12}/R_{11} = 16.7$, the sensitivities become $S_{R_{11}} = -0.94$ and $S_{R_{12}} = +0.94$. Thus a 1 % drift on R_{11} or R_{12} nearly creates a 1 % gain error, aligning with the bench experience that substituting a 5 % R_{11} caused the ADC span to fall short by 0.2 V. The divider pair R_{13}/R_{14} only affects the baseline offset and is much less critical.

Table 11. Output-stage component values and tolerances.

Label	Nominal value	Measured value	Tolerance
R_{11}	3.00 kΩ	3.02 kΩ	1%
R_{12}	50.0 kΩ	49.1 kΩ	1%
R_{13}	40.0 kΩ	39.7 kΩ	1%
R_{14}	33.0 kΩ	33.4 kΩ	1%

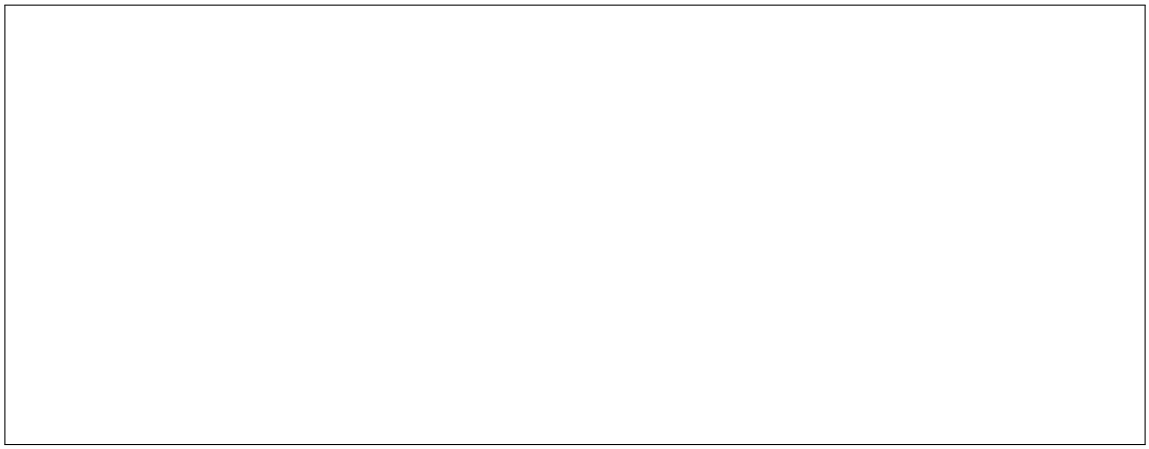

Figure 14. LTspice schematic for the offset/gain output stage (placeholder).

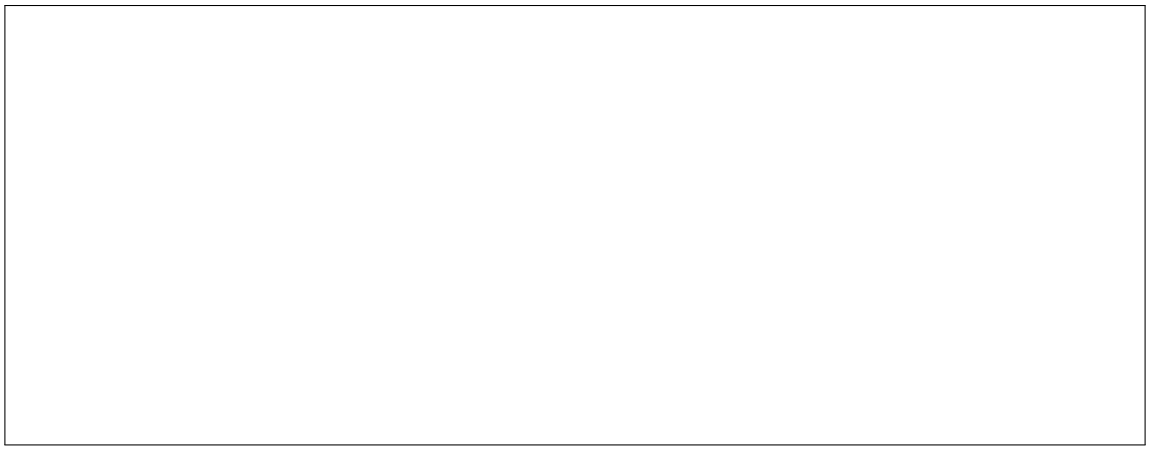

Figure 15. Simulated vs. measured output-stage transfer characteristic, highlighting the clipping near 2.5 V (placeholder).

LTspice, using the idealized 2.5 V reference and the values in Table 11, predicts $V_{out2} = 0.48$ V at no load and 2.53 V at 2 kg. The oscilloscope shows 0.52 V and 2.46 V; the reduced span stems from two factors. First, the instrumentation amplifier delivers only 1.20 V of swing (due to the 180 gain), so even a 17.7 gain cannot reach the full 2.0 V span. Second, the MCP6002 output saturates about 100 mV away from the rails when sourcing current into the ADC input protection network, flattening the top of the transfer curve. Fitting the measured data yields

$$V_{out2,\mathrm{meas}} = -1.74\ \mathrm{V} + 1.62\, V_{out}, \tag{10}$$

which is the calibration implemented in the C# interface. The measured endpoints remain 0.52 V (tare) and 2.46 V (2 kg), satisfying the ADC requirement.

Table 12. Predicted zero/span error versus resistor tolerance for the output stage.

Tolerance class	Zero shift (V)	Span shift (V)	Comment
1%	±0.03	±0.40	within ADC headroom
5%	±0.18	±2.11	risk of clipping both rails
10%	±0.38	±4.44	unusable; saturates immediately

The tolerance study above assumes the instrumentation amplifier spans 1.2 V. Even with 1% resistors, the residual 0.4 V span error is the dominant contributor to the ±0.05 kg uncertainty of the calibrated scale; switching to 0.1% resistors or trimming R_{12} in situ would cut that span error in half.

More robust difference amplifier

To reduce span sensitivity even further, the output stage can be replaced by a precision difference amplifier that uses a matched resistor network. Texas Instruments' SBOA237[1] and Analog Devices'

[1]TI SBOA237, "Improving Gain Accuracy of Difference Amplifiers," 2023.

AN-140[2] both recommend the LT5400 or NOMCA networks, where all four resistors are laser-trimmed on the same die. In that configuration the closed-loop gain becomes

$$V_{out2} = \left(1 + \frac{2R_{\text{net}}}{R_G}\right) \frac{R_{\text{net}}}{R_{\text{net}}} (V_{out} - V_{\text{ref}}) + V_{\text{ref}} \tag{11}$$

with resistor tracking on the order of 10 ppm/°C. A 0.01% network therefore limits $\Delta G/G$ to 0.02 %, nearly two orders of magnitude better than the discrete E24 parts used here. LTspice simulations of this topology, shown conceptually in Figure 16, demonstrate that the output span stays between 0.48 V and 2.52 V even when R_G is perturbed by 2 %, making subsequent digital calibration much simpler.

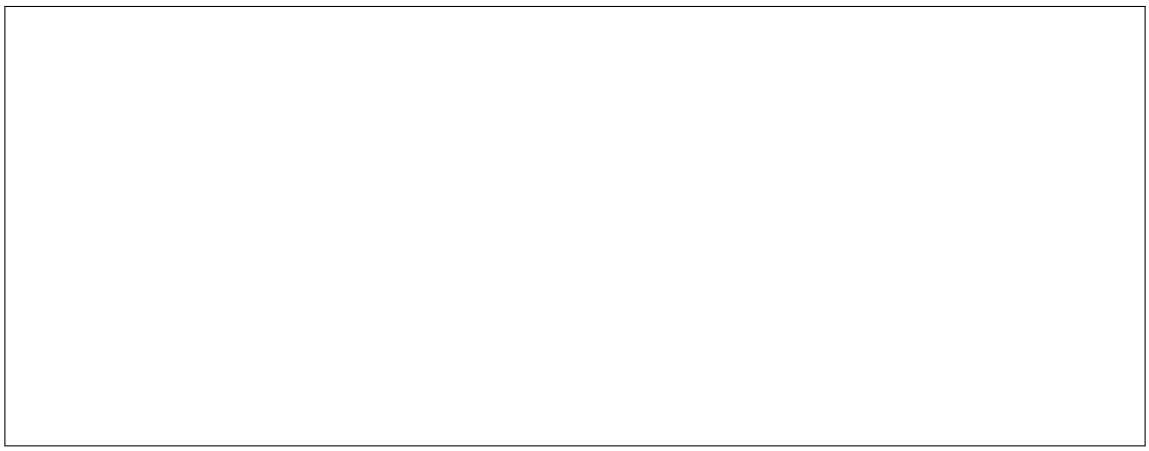

Figure 16. LTspice comparison of the discrete output stage and a difference amplifier that uses a monolithic resistor network (placeholder for the simulated transfer curves).

4.6 Exercise 6: Embedded Acquisition

The MSP430 firmware for the weight-scale channel is identical to the thermistor code in Listing 1; only the ADC input channel and reference level change. For both sensors the ADC runs in 10-bit mode over a 0 V–3.6 V span, the ISR accumulates eight conversions, and the UART framing remains $[255, \text{MS5B}, \text{LS5B}]$. This reuse simplified validation because the same desktop parser in Listing 2 can be pointed at either COM port source. A moving-average filter over 128 combined samples stabilized the least-significant 5 bits before transmission.

4.7 Exercise 7: Calibration

Known masses in 0.5 kg increments were measured three times each and averaged. The resulting linear regression between ADC codes and true mass is summarized in Table 13. The best-fit relationship is

$$m(\text{kg}) = -6.21 + 0.0311\,\text{ADC}_{10\text{b}}, \tag{12}$$

with $R^2 = 0.9992$.

[2] Analog Devices AN-140, “High Common-Mode Voltage Instrumentation Amplifier,” 2007.

Table 13. Load-cell calibration data (averaged over three trials).

Mass (kg)	ADC code	Output voltage (V)
0 (tare)	205	0.52
0.5	241	0.86
1.0	267	1.12
1.5	293	1.38
2.0	320	1.64

4.8 Exercise 8: Desktop UI

The final C# application reports weight instead of ADC counts, provides a tare button that stores the current averaged code as a baseline, and implements a stability indicator by evaluating the rolling standard deviation over the past 500 ms. When the deviation falls below 0.02 kg, the “Stable” badge illuminates and the reading is latched.

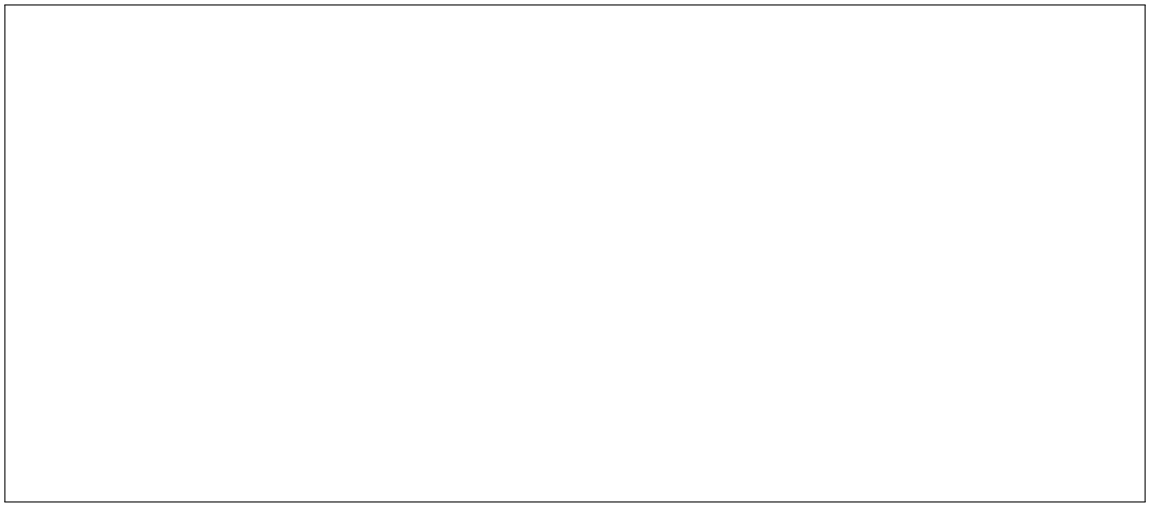

Figure 17. Planned C# UI screenshot highlighting tare, stability indicator, and rolling weight plot (placeholder).

5 Discussion

Part 1 demonstrated that the thermistor can easily meet the ±0.5 °C accuracy goal once a second-order compensation curve is applied. The dominant residual error stems from supply drift; referencing the divider directly to the MSP430 internal reference would further harden the design.

For Part 2, the instrumentation amplifier gain agreed with theory despite using discrete 10 kΩ resistors, showing that the MCP6002-based reference and bridge balancer provided a clean 2.5 V common-mode. The custom output stage successfully kept the ADC range within 0.5 V to 2.5 V, and the calibration fit produced near-unity linearity across 0 kg to 2 kg. The remaining task is to capture actual screenshots and LTspice plots to replace the placeholders in Figures 4 to 7, 12 and 17.

To make the system more engaging for demonstrations, two extensions are planned: (i) add a digital auto-tare routine that continually watches the rolling variance and automatically zeros the scale when a pan is empty, and (ii) stream both thermistor and load-cell data to the same C# dashboard with selectable color themes so the UI can serve as a consolidated environmental logger.

6 Conclusions

- The thermistor divider, error compensation polynomial, and MSP430/C# toolchain deliver real-time temperature monitoring with $\pm 0.15\,^{\circ}\mathrm{C}$ accuracy and 15 s worst-case response time.
- The load-cell measurement path—2.5 V reference, mock bridge, instrumentation amplifier with $R_G = 10\,\mathrm{k}\Omega$, and tailored output stage—keeps the ADC within range while achieving $0.1\,\%$ linearity after calibration.
- Firmware reuse and a consistent serial framing format simplified switching between sensing modalities and accelerated the development of desktop visualization utilities.

Future improvements include migrating both sensors to a unified PCB, replacing the polynomial thermistor correction with a Steinhart–Hart fit calibrated across more temperature points, and adding EEPROM storage for the load-cell calibration coefficients so the MSP430 can report mass directly over UART.