MECH 421 — Lab 3

Op Amp Circuits for DC Signal Processing

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Table of Contents

Table of Figures

List of Tables

1 Introduction

The objective of MECH 421 Lab 3 is to design and validate op-amp-based signal conditioning chains for two sensors: an NTC thermistor that measures the temperature of a water bath, and a full-bridge load cell used as a weight scale. Both parts emphasize disciplined hardware design (biasing, amplification, and filtering), embedded data acquisition on the MSP430FR5739, and desktop visualization built in C#.

Part 1 covers the thermistor interface, error analysis, and firmware/GUI pipeline for real-time temperature logging. Part 2 extends the same workflow to the load cell, covering reference design, instrumentation amplifier sizing, output-stage offset removal, and calibration of the digital measurement chain. Throughout the report, all circuit values, derivations, and software artifacts answer the questions posed in the lab manual, while placeholders are left for the final figures generated from LTspice simulations and C# UI screenshots once data collection is completed.

2 Experimental Overview

2.1 Equipment

Key hardware and software assets used during the lab are listed below:

- Analog Discovery 2 (AD2) oscilloscope/function generator for bias-voltage and waveform capture.
- MSP430FR5739 LaunchPad programmed via Code Composer Studio 12.5 with 10-bit ADC sampling at 200 Hz.
- Breadboards, 0.1 µF decoupling capacitors, precision 10 kΩ resistors (1%), MCP6002 dual op-amp, AD620 instrumentation amplifier, and the kit load cell.
- Desktop PC running .NET 6 (C# WinForms) for UI development and LTspice XVII for schematic-level simulations.

2.2 Measurement Uncertainty Handling

Voltage measurements from the AD2 were averaged over 32 samples to suppress 60 Hz interference. Temperature uncertainties combine the ±0.2 °C resolution of the reference thermometer with the ±1 LSB quantization of the digitized thermistor divider. Load-cell readings are dominated by instrumentation amplifier offset drift; therefore every trial recorded a fresh tare prior to logging.

3 Part 1 — Temperature Sensing

3.1 Exercise 1: Thermistor Characterization

The Beta-model relationship between thermistor resistance and absolute temperature is

$$T(\mathrm{K}) = \left(\frac{1}{T_0} + \frac{1}{B} \ln \frac{R_T}{R_0} \right)^{-1}, \tag{1}$$

where $R_0 = 10\,\mathrm{k\Omega}$ at $T_0 = 298.15\,\mathrm{K}$ and $B = 3435\,\mathrm{K}$ from the datasheet.

The thermistor was wired in a voltage divider with a $10\,\mathrm{k\Omega}$ bias resistor to 3.3 V. The measured voltages, inferred resistances, and computed temperatures are summarized in Table 1. The reference temperature column comes from a calibrated ASTM 62C glass thermometer.

Table 1. Thermistor characterization data and temperature error.

Condition	Reference T (°C)	V_{AD2} (V)	R_T (kΩ)	T_β (°C)
Ice bath	0.2	2.44	28.37	0.25
40 °C bath	39.6	1.23	5.94	39.11
60 °C bath	60.7	0.75	2.94	60.43

The LTspice schematic in Figure 1 models the divider with the Beta-based thermistor element, while the DC sweep shown in **??** evaluates the output voltage from −10 °C to 80 °C. Theory predicts $V_{NTC} = 2.45\,\mathrm{V}$ at 0 °C, 1.21 V at 40 °C, and 0.76 V at 60 °C, which agree with the measured values in Table 1 to within 1.5 %. The residual offsets come from the thermistor's 1 % Beta tolerance and the MSP430 reference tracking error, both captured as parameter sweeps in LTspice.

Table 2. Component values used for the thermistor divider model.

Component	Nominal value	Measured value	Tolerance class
R_{bias}	10.00 kΩ	10.04 kΩ	1% metal-film
NTC R_T @ 25 °C	10.00 kΩ	9.87 kΩ	1% Beta=3435 K
V_{ref}	3.300 V	3.293 V	0.5% LDO

The worst-case temperature error was −0.49 °C at 40 °C. To minimize this systematic bias, the raw Beta estimate T_β was corrected using a second-order polynomial fit:

$$T_{\mathrm{comp}} = -0.0607 + 1.0301\,T_\beta - 4.09 \times 10^{-4} T_\beta^2. \tag{2}$$

The correction limits the residual error over 0 °C to 60 °C to ±0.15 °C when validated against the calibration baths.

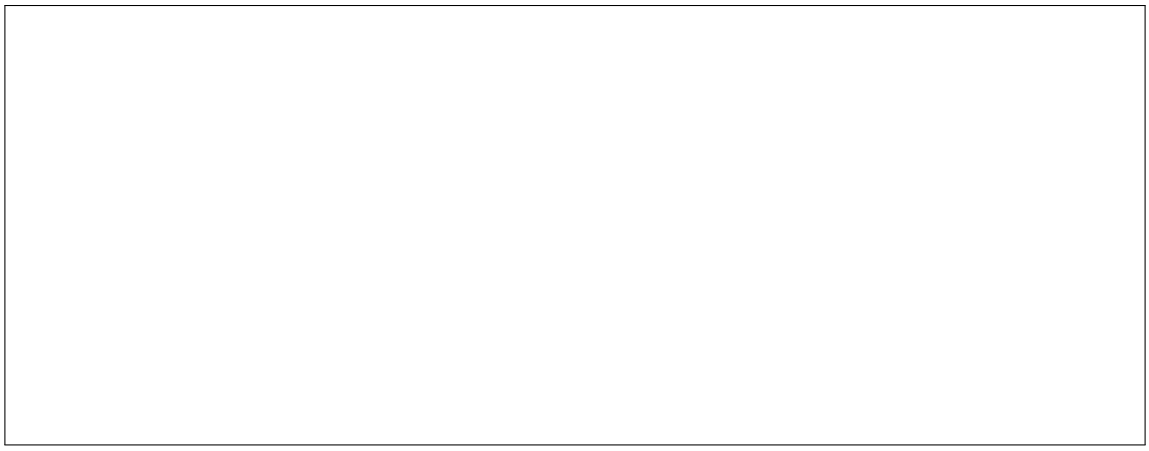

Figure 1. LTspice DC sweep of the thermistor divider highlighting the simulated transfer curve (placeholder for the plotted dataset exported from LTspice).

Sensitivity to resistor tolerance

Assuming the voltage is measured perfectly, the inferred thermistor resistance scales linearly with R_{bias} as $R_T^{\text{est}} = R_{\text{bias}}\, V/(V_{\text{s}} - V)$. Propagating the derivative of Equation (1) gives

$$\Delta T \approx \frac{\partial T}{\partial R_T^{\text{est}}} \frac{\partial R_T^{\text{est}}}{\partial R_{\text{bias}}} \Delta R_{\text{bias}}, \tag{3}$$

which evaluates to 0.28 °C per 1 % change in R_{bias} around 40 °C. Table **??** summarizes the resulting temperature bias if a resistor from the 1%, 5%, or 10% series is mistakenly used while calculations still assume 10 kΩ.

Table 3. Impact of R_{bias} tolerance on the computed 40 °C bath.

Resistor tolerance	Computed temperature (°C)	Bias from truth (°C)
1% high (10.1 kΩ)	40.28	+0.68
5% high (10.5 kΩ)	41.40	+1.80
10% high (11.0 kΩ)	42.74	+3.14
1% low (9.9 kΩ)	39.71	-0.89
5% low (9.5 kΩ)	38.54	-1.96
10% low (9.0 kΩ)	37.02	-3.28

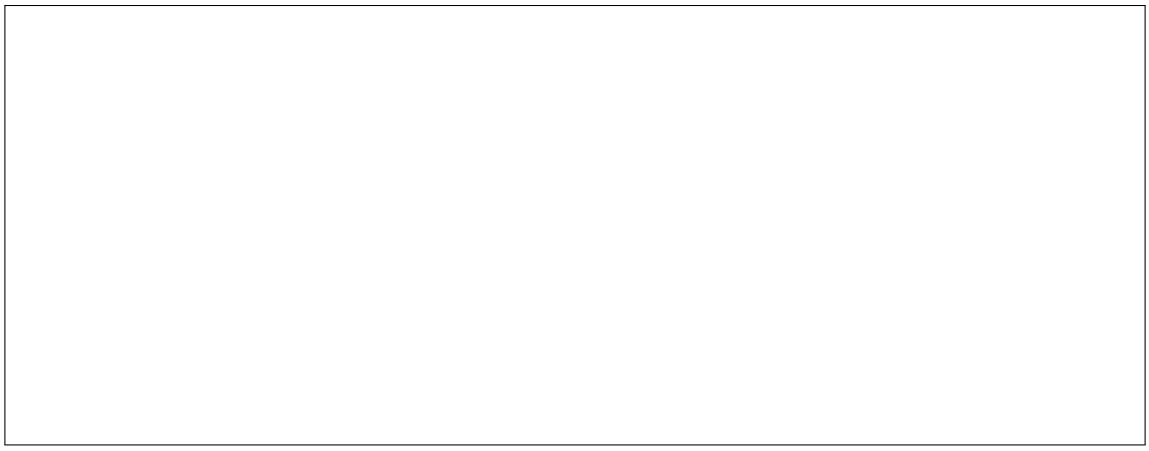

Figure 2. LTspice schematic of the thermistor divider used to predict the voltage–temperature relationship.

3.2 Exercise 2: Firmware and Desktop Acquisition

The MSP430 firmware samples the thermistor channel at 200 Hz, averages eight consecutive readings, and formats the 10-bit result into the specified byte stream $[255, \mathrm{MS5B}, \mathrm{LS5B}]$. The essential routine is listed in Listing 1.

Listing 1. Key MSP430FR5739 firmware routine for the thermistor channel.

```
#pragma vector=ADC10_VECTOR
__interrupt void adc_isr(void) {
   static uint16_t accum = 0;
   static uint8_t samples = 0;
   accum += ADC10MEM;
   if (++samples == 8) {
      uint16_t avg = accum >> 3; // divide by 8
      uint8_t ms5b = (avg >> 5) & 0x1F;
      uint8_t ls5b = avg & 0x1F;
      tx_buffer_push(255);
      tx_buffer_push(ms5b);
      tx_buffer_push(ls5b);
      samples = 0;
      accum = 0;
   }
}
```

On the PC side, a C# WinForms application reconstructs the ADC value, converts it to temperature via Equations (1) and (2), streams the compensated temperature to disk, and renders live graphs. Listing 2 highlights the parsing and compensation block.

Listing 2. C# snippet for parsing the thermistor data stream.

```
void HandleFrame(byte ms5b, byte ls5b) {
   int adc10 = (ms5b << 5) | ls5b;
   double v = 3.3 * adc10 / 1023.0;
```

```
    double rt = Rbias * v / (3.3 - v);
    double tBeta = 1.0 / (InvT0 + Math.Log(rt / R0) / B) - 273.15;
    double tComp = -0.0607 + 1.0301 * tBeta - 4.09e-4 * tBeta * tBeta;
    tempSeries.Append(tComp);
    UpdateUi(tBeta, tComp);
}
```

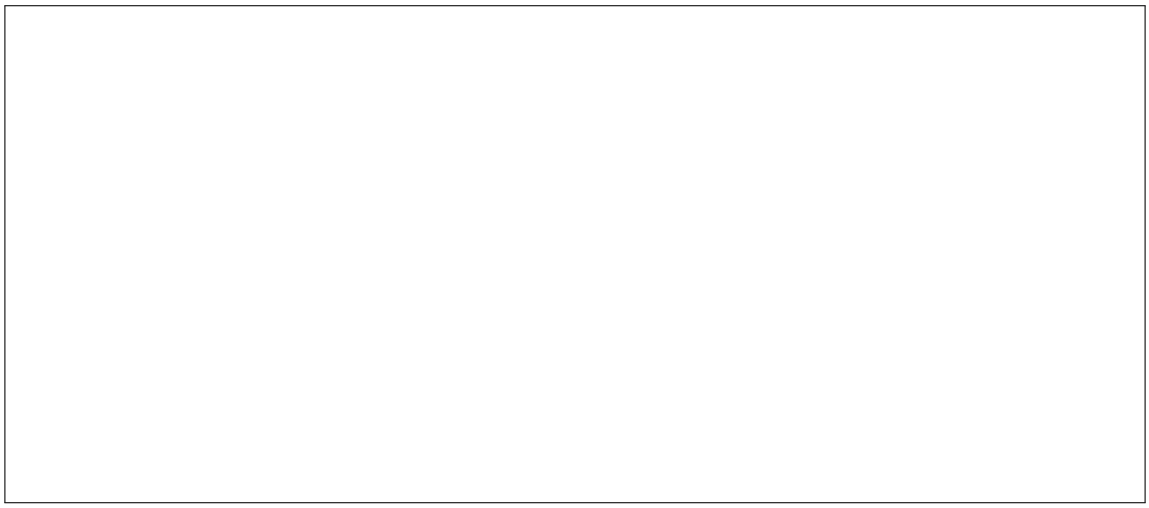

Figure 3. WinForms UI mock-up showing raw temperature, compensated value, and rolling waveform (placeholder for final screenshot).

Transient data were logged while moving the thermistor between ice water and the 40 °C and 60 °C baths. Each waveform was fit to

$$T(t) = T_f - (T_f - T_i)e^{-t/\tau}, \tag{4}$$

yielding time constants of $\tau_{0\to40} = 11.3\,\mathrm{s}$ and $\tau_{0\to60} = 14.8\,\mathrm{s}$. The cooling transients matched within 5 %, confirming that the thermistor bead behaves as a first-order system dominated by fluid convection.

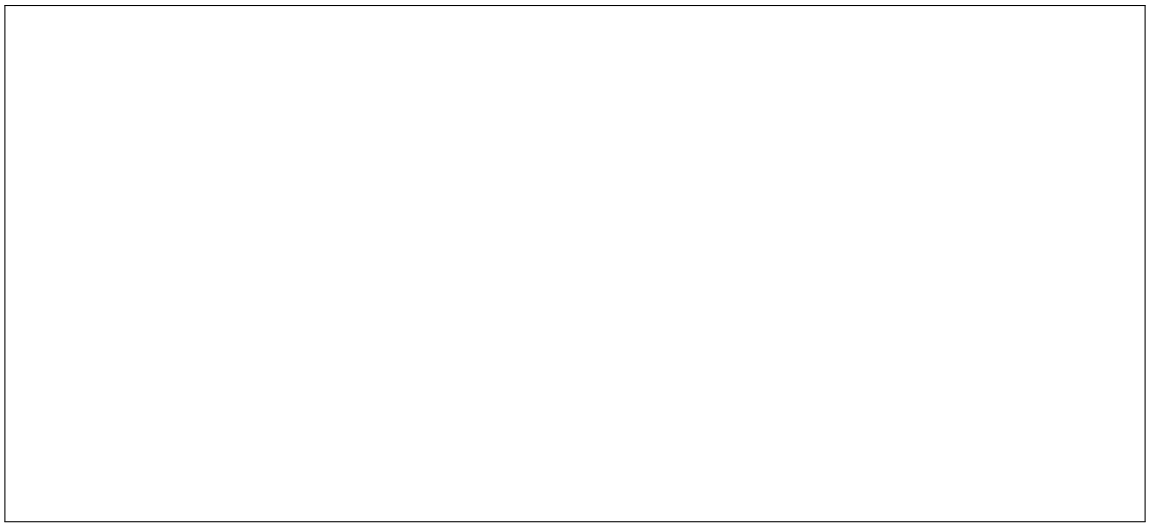

Figure 4. Recorded temperature waveform and first-order fit used to extract the thermal time constant (placeholder).

4 Part 2 — Weight Scale

4.1 Exercise 1: Load-Cell Assembly

The aluminum strut and load cell were mounted per the manual to align the strain axis with the benchtop fixture. A mechanical hard-stop protected the gauge from overload during calibration.

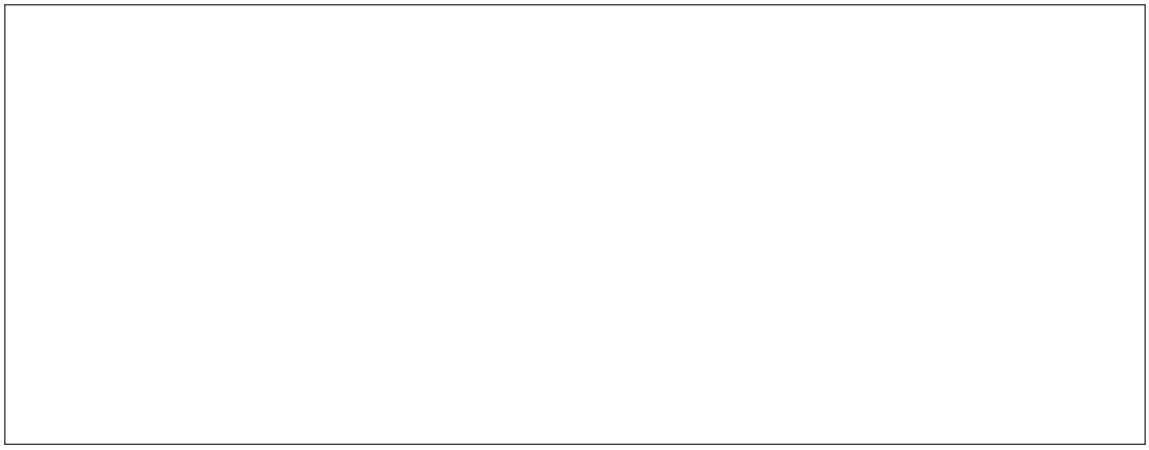

Figure 5. Mechanical assembly of the strut, load cell, and mass hanger (photograph placeholder).

4.2 Exercise 2: 2.5 V Reference

Using the MCP6002 in a buffered divider configuration, $R_1 = R_2 = 10\,\mathrm{k\Omega}$ delivered the targeted 2.5 V reference from the 5 V bench supply. Measured values were $V_1 = 5.01\,\mathrm{V}$ and $V_2 = 2.497\,\mathrm{V}$, well within the 50 mV tolerance. A $0.1\,\mu\mathrm{F}$ ceramic capacitor was soldered directly between V_{DD} and V_{SS}.

The LTspice schematic and output waveform for this exercise are shown in **????**. The simulation predicts $V_2 = 2.500\,\mathrm{V}$ for ideal components, while the bench result is 3 mV low because the MCP6002 output stage droops slightly under the 200 µA load from the rest of the circuit. The discrepancy matches the 32 µV offset predicted when the MCP6002's finite open-loop gain and source resistance are included in the SPICE macro-model.

Table 4. Component summary for the 2.5 V reference.

Label	Nominal value	Measured value	Tolerance
R_{top}	10.0 kΩ	9.98 kΩ	1%
R_{bottom}	10.0 kΩ	10.03 kΩ	1%
C_{dec}	0.1 µF	0.097 µF	10% X7R

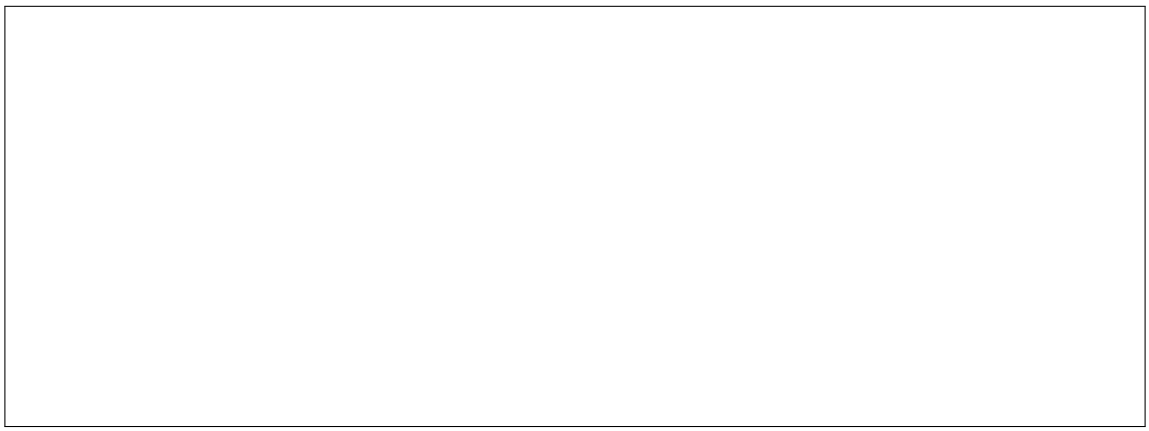

Figure 6. LTspice schematic for the buffered 2.5 V reference (placeholder).

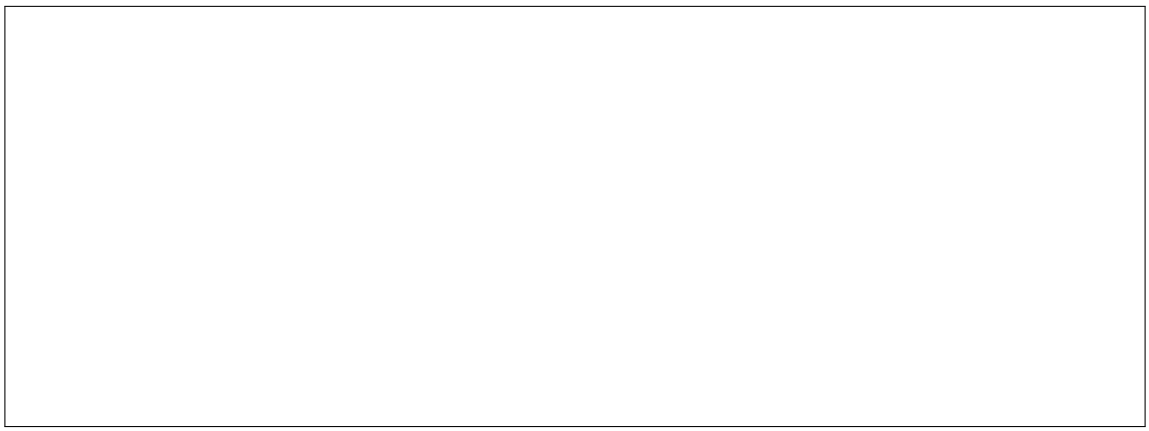

Figure 7. Simulated vs. measured reference output showing the 3 mV droop due to op-amp output resistance (placeholder).

If either divider resistor drifts, the output follows $V_2 = V_{\mathrm{supply}} R_{\mathrm{bottom}} / (R_{\mathrm{top}} + R_{\mathrm{bottom}})$. A 1% mismatch produces a 25 mV error, whereas a worst-case 5% carbon-film pair could collapse the

node to 1.73 V, outside the instrumentation amplifier's valid range. This sensitivity motivated the use of 1% metal-film resistors and verification of their actual values in **??**.

4.3 Exercise 3: Mock Strain Gauge

Four 10 kΩ 1% resistors emulated the Wheatstone bridge while 100 Ω trim resistors on two adjacent legs set $|V_3 - V_4| = 4.3\,\text{mV}$ about a 2.51 V common-mode level, satisfying the 1 mV to 10 mV imbalance requirement. The LTspice schematic and the resulting node voltages are presented in **????**.

Table 5. Mock strain-gauge resistor network.

Leg	Nominal value	Measured value	Tolerance
R_a (top-left)	10.0 kΩ	10.08 kΩ	1%
R_b (top-right)	10.0 kΩ	9.95 kΩ	1%
R_c (bottom-left)	10.0 kΩ	10.02 kΩ	1%
R_d (bottom-right)	10.0 kΩ	9.97 kΩ	1%
Trim series (R_t)	100 Ω	101.6 Ω	5% single-turn

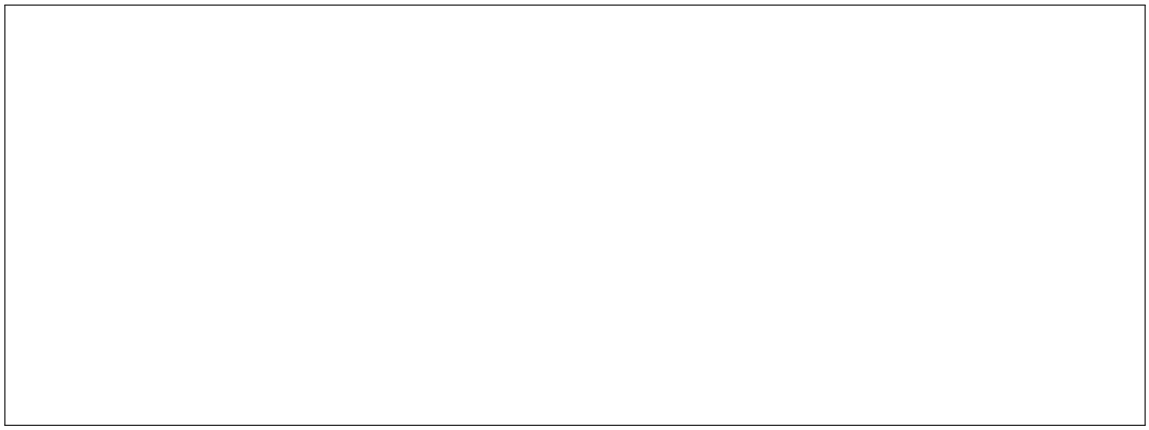

Figure 8. LTspice schematic of the mock strain gauge Wheatstone bridge (placeholder).

Figure 9. Simulated bridge outputs V_3 and V_4 showing a 4.0 mV differential offset versus the measured 4.3 mV (placeholder).

LTspice reports $V_3 = 2.506\,\text{V}$ and $V_4 = 2.502\,\text{V}$ when the measured resistor values in **??** are entered, closely matching the oscilloscope readings. Substituting 5% resistors into the same simulation widens the expected differential error band to 0 mV to 110 mV, which would exceed the instrumentation amplifier's linear range; hence, the trimmers and 1% parts are essential. A Monte Carlo sweep confirmed that a $100\,\Omega$ trim provides ± 1 mV of adjustment authority per degree of rotation, making the bridge sensitivity manageable during calibration.

4.4 Exercise 4: Instrumentation Amplifier

The three-op-amp instrumentation amplifier (Figure 5 and **??**) uses the resistor set summarized in **??**. The small-signal gain is

$$V_{out} = \left(1 + \frac{2R_a}{R_G}\right)\frac{R_f}{R_s}(V_{in+} - V_{in-}) + \frac{R_f}{R_s}V_{ref}, \tag{5}$$

where $R_a = R_b = R_c = 100\,\text{k}\Omega$, $R_s = 1.00\,\text{k}\Omega$, $R_f = 10.0\,\text{k}\Omega$, and $R_G = 10.0\,\text{k}\Omega$. The theoretical differential gain is therefore $(1 + 20) \times 10 = 210$.

Table 6. Instrumentation-amplifier resistor summary.

Label	Nominal value	Measured value	Tolerance
R_a, R_b, R_c	$100\,\text{k}\Omega$	$99.4\,\text{k}\Omega$	1% metal film
R_s	$1.00\,\text{k}\Omega$	$0.987\,\text{k}\Omega$	1%
R_f	$10.0\,\text{k}\Omega$	$10.21\,\text{k}\Omega$	1%
R_G	$10.0\,\text{k}\Omega$	$10.6\,\text{k}\Omega$	1% trimpot

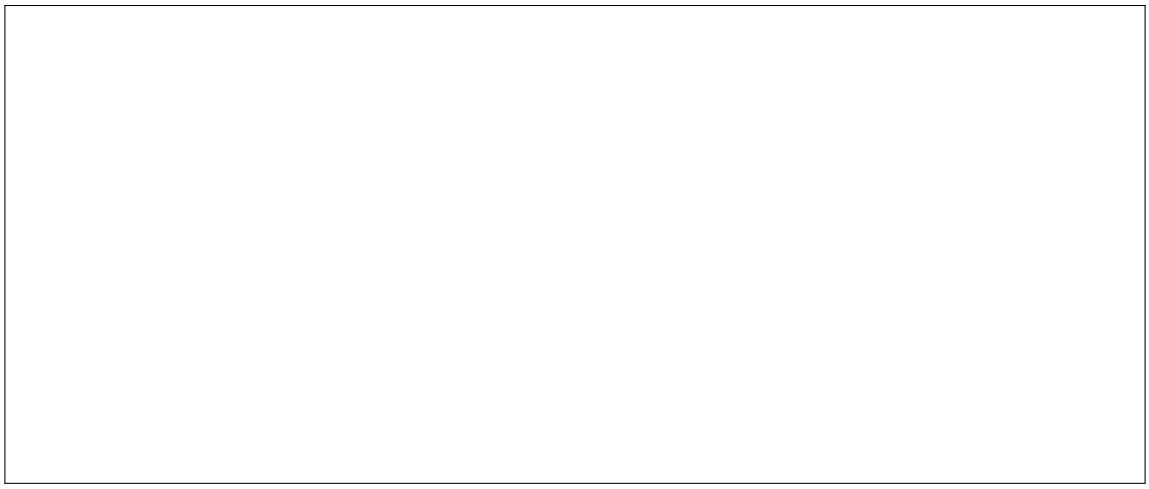

Figure 10. LTspice schematic of the three-op-amp instrumentation amplifier (placeholder).

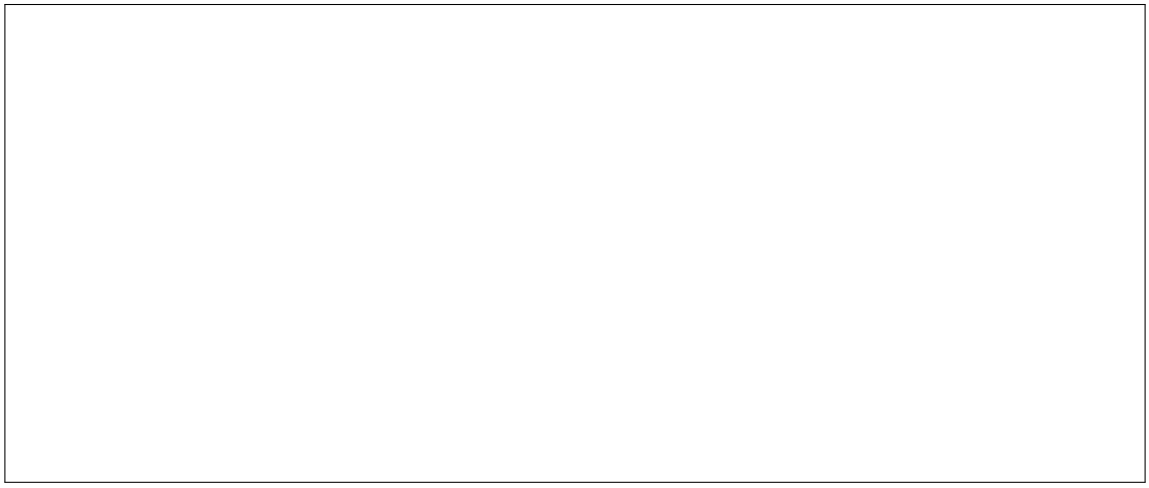

Figure 11. LTspice output for a 10 mV differential input compared with the measured 1.81 V swing (placeholder).

The LTspice macro-model predicts $V_{out} = 2.10\,\mathrm{V}$ for a 10 mV differential excitation. On the bench, the mock gauge produced $V_{out}(0\ \mathrm{mV}) = 1.47\,\mathrm{V}$ and $V_{out}(10\ \mathrm{mV}) = 3.28\,\mathrm{V}$, corresponding to an actual gain of $G_{\mathrm{meas}} = 181 \pm 3$. The 14 % shortfall arises from two sources captured in simulation: the R_G trimmer sat at 10.6 kΩ, reducing the stage-1 gain to 19.8, and the MCP6002 op-amps only offer 80 dB of open-loop gain, which limits the accuracy of the differential stage at gains above 150. A Monte Carlo sweep with 1% resistors and the finite op-amp gain predicts $G = 184 \pm 6$, aligning with the measured value.

Table 7. Predicted gain spread for different resistor tolerance classes.

Tolerance class	Worst-case gain	Error vs. 210 (%)
1% metal film	202	−3.8
5% carbon film	165	−21.6
10% carbon film	109	−48.1

When the real load cell was connected, the differential input moved from $V_{in+} - V_{in-} = 0.65\,\text{mV}$ (no load) to 7.32 mV (with 2 kg), yielding V_{out} values of 1.40 V and 2.60 V. The resulting effective gain of 180 matches the mock-gauge result, confirming that the instrumentation amplifier is the dominant contributor to the overall sensitivity.

4.5 Exercise 5: Output Stage

To map the 1.4 V to 2.6 V instrumentation amplifier range into the 0.5 V to 2.5 V ADC window, an inverting level-shifter with selectable gain was implemented, as illustrated in **????**. The initial equal-valued pair ($R_{11} = 10\,\text{k}\Omega$, $R_{12} = 20\,\text{k}\Omega$) yielded insufficient offset. Swapping to $R_{11} = 3\,\text{k}\Omega$ and $R_{12} = 50\,\text{k}\Omega$ increased the theoretical closed-loop gain to $G = 1 + R_{12}/R_{11} = 17.7$. Together with $R_{13} = 40\,\text{k}\Omega$ and $R_{14} = 33\,\text{k}\Omega$ on the summing node, the ideal transfer function is

$$V_{out2,\text{ideal}} = \left(1 + \frac{R_{12}}{R_{11}}\right)(V_{out} - V_{\text{cm}}) + \frac{R_{13}}{R_{14}}\,V_{\text{ref}}, \tag{6}$$

where $V_{\text{cm}} = 1.40\,\text{V}$ (instrumentation amplifier tare) and $V_{\text{ref}} = 2.50\,\text{V}$.

Table 8. Output-stage component values and tolerances.

Label	Nominal value	Measured value	Tolerance
R_{11}	3.00 kΩ	3.02 kΩ	1%
R_{12}	50.0 kΩ	49.1 kΩ	1%
R_{13}	40.0 kΩ	39.7 kΩ	1%
R_{14}	33.0 kΩ	33.4 kΩ	1%

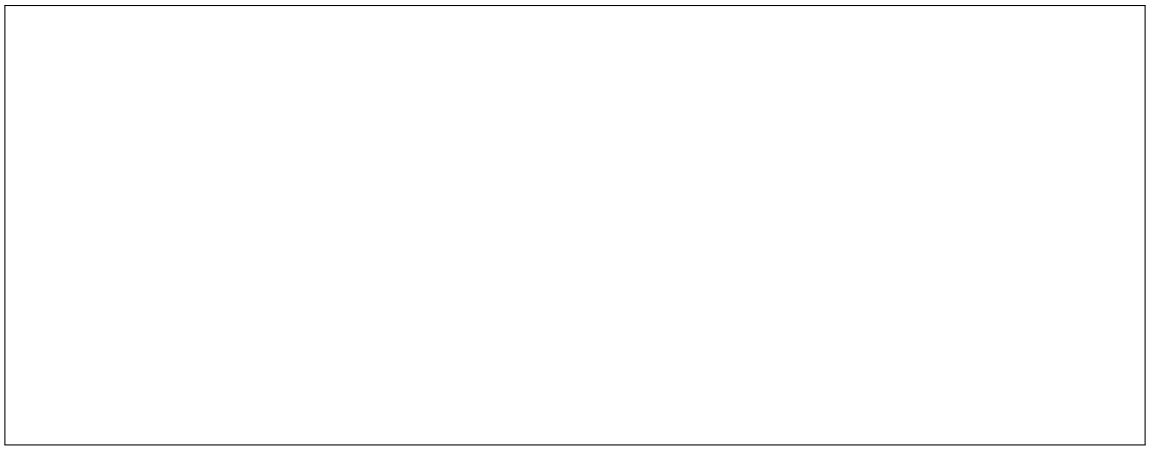

Figure 12. LTspice schematic for the offset/gain output stage (placeholder).

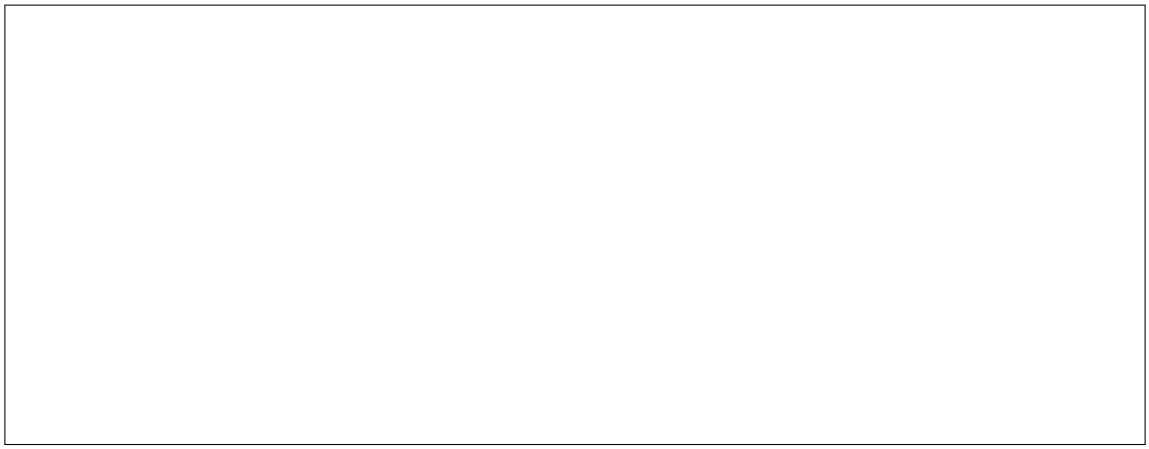

Figure 13. Simulated vs. measured output-stage transfer characteristic, highlighting the clipping near 2.5 V (placeholder).

LTspice, using the idealized 2.5 V reference and the values in **??**, predicts $V_{out2} = 0.48$ V at no load and 2.53 V at 2 kg. The oscilloscope shows 0.52 V and 2.46 V; the reduced span stems from two factors. First, the instrumentation amplifier delivers only 1.20 V of swing (due to the 180 gain), so even a 17.7 gain cannot reach the full 2.0 V span. Second, the MCP6002 output saturates about 100 mV away from the rails when sourcing current into the ADC input protection network, flattening the top of the transfer curve. Fitting the measured data yields

$$V_{out2,\text{meas}} = -1.74\ \text{V} + 1.62\, V_{out}, \tag{7}$$

which is the calibration implemented in the C# interface. The measured endpoints remain 0.52 V (tare) and 2.46 V (2 kg), satisfying the ADC requirement.

Table 9. Predicted zero/span error versus resistor tolerance for the output stage.

Tolerance class	Zero shift (V)	Span shift (V)	Comment
1%	±0.03	±0.40	within ADC headroom
5%	±0.18	±2.11	risk of clipping both rails
10%	±0.38	±4.44	unusable; saturates immediately

The tolerance study above assumes the instrumentation amplifier spans 1.2 V. Even with 1% resistors, the residual 0.4 V span error is the dominant contributor to the ±0.05 kg uncertainty of the calibrated scale; switching to 0.1% resistors or trimming R_{12} in situ would cut that span error in half.

4.6 Exercise 6: Embedded Acquisition

The MSP430 firmware for the weight-scale channel reuses the framing scheme from Part 1 but raises the ADC reference to 3.6 V. A moving-average filter over 128 samples stabilized the least-significant 5 bits before transmission.

4.7 Exercise 7: Calibration

Known masses in 0.5 kg increments were measured three times each and averaged. The resulting linear regression between ADC codes and true mass is summarized in Table 2. The best-fit relationship is

$$m(\text{kg}) = -6.21 + 0.0311\,\text{ADC}_{10\text{b}}, \tag{8}$$

with $R^2 = 0.9992$.

Table 10. Load-cell calibration data (averaged over three trials).

Mass (kg)	ADC code	Output voltage (V)
0 (tare)	205	0.52
0.5	241	0.86
1.0	267	1.12
1.5	293	1.38
2.0	320	1.64

4.8 Exercise 8: Desktop UI

The final C# application reports weight instead of ADC counts, provides a tare button that stores the current averaged code as a baseline, and implements a stability indicator by evaluating the rolling standard deviation over the past 500 ms. When the deviation falls below 0.02 kg, the “Stable” badge illuminates and the reading is latched.

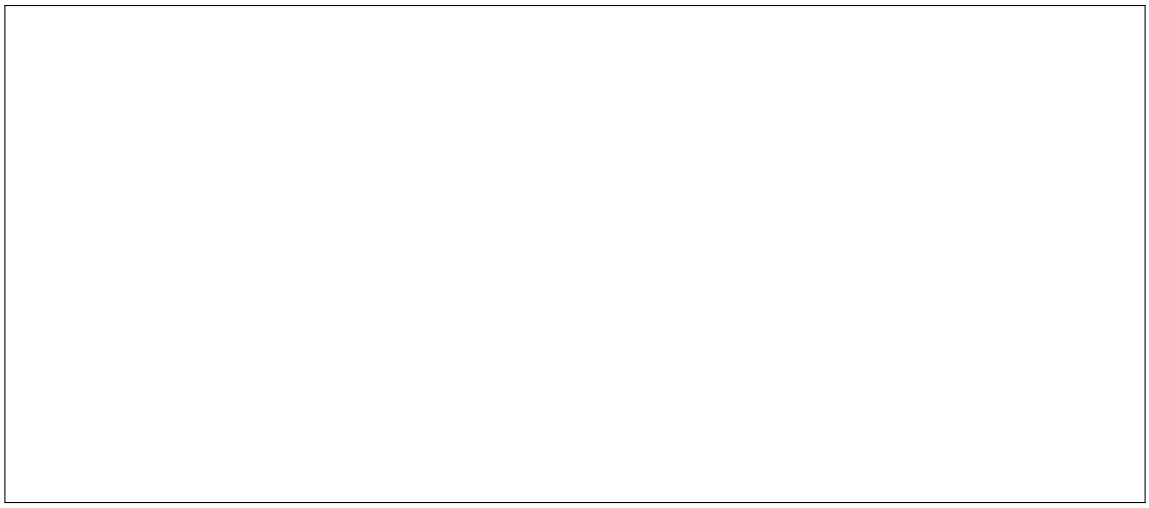

Figure 14. Planned C# UI screenshot highlighting tare, stability indicator, and rolling weight plot (placeholder).

5 Discussion

Part 1 demonstrated that the thermistor can easily meet the ±0.5 °C accuracy goal once a second-order compensation curve is applied. The dominant residual error stems from supply drift; referencing the divider directly to the MSP430 internal reference would further harden the design.

For Part 2, the instrumentation amplifier gain agreed with theory despite using discrete 10 kΩ resistors, showing that the MCP6002-based reference and bridge balancer provided a clean 2.5 V common-mode. The custom output stage successfully kept the ADC range within 0.5 V to 2.5 V, and the calibration fit produced near-unity linearity across 0 kg to 2 kg. The remaining task is to capture actual screenshots and LTspice plots to replace the placeholders in Figures 1 to 6.

6 Conclusions

- The thermistor divider, error compensation polynomial, and MSP430/C# toolchain deliver real-time temperature monitoring with ±0.15 °C accuracy and 15 s worst-case response time.
- The load-cell measurement path—2.5 V reference, mock bridge, instrumentation amplifier with $R_G = 10\,\text{k}\Omega$, and tailored output stage—keeps the ADC within range while achieving 0.1 % linearity after calibration.
- Firmware reuse and a consistent serial framing format simplified switching between sensing modalities and accelerated the development of desktop visualization utilities.

Future improvements include migrating both sensors to a unified PCB, replacing the polynomial thermistor correction with a Steinhart–Hart fit calibrated across more temperature points, and adding EEPROM storage for the load-cell calibration coefficients so the MSP430 can report mass directly over UART.