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| **Architetture dei Sistemi di Elaborazione** | Delivery date:  October 29th 2021 |
| **Laboratory**  **3** | Expected delivery of lab\_03.zip must include:   * program\_2\_a.s, program\_2\_b.s and program\_2\_c.s * this file compiled and if possible in pdf format. |

Please, configure the winMIPS64 simulator with the *Base Configuration* provided in the following:

* Code address bus: 12
* Data address bus: 12
* Pipelined FP arithmetic unit (latency): 4 stages
* Pipelined multiplier unit (latency): 8 stages
* divider unit (latency): not pipelined unit, 12 clock cycles
* Forwarding is enabled
* Branch prediction is disabled
* Branch delay slot is disabled
* *Integer ALU: 1 clock cycle*
* *Data memory: 1 clock cycle*
* *Branch delay slot: 1 clock cycle*.

1. Starting from the assembly program you created in the previous lab called **program\_2.s**,:

for (i = 0; i < 40; i++){

v5[i] = v1[i]+(v2[i] \* v3[i]);

v6[i] = v5[i]\*v4[i];

v7[i] = v6[i]/v2[i];

}

* + 1. Detect manually the different data, structural and control hazards that provoke a pipeline stall
    2. Optimize the program by re-scheduling the program instructions in order to eliminate as much hazards as possible. Compute manually the number of clock cycles the new program (**program\_2\_a.s**) requires to execute, and compare the obtained results with the ones obtained by the simulator.
    3. Starting from **program\_2\_a.s**, enable the *branch delay slot* and re-schedule some instructions in order to improve the previous program execution time. Compute manually the number of clock cycles the new program (**program\_2\_b.s**) requires to execute, and compare the obtained results with the ones obtained by the simulator.
    4. Unroll 4 times the program (**program\_2\_b.s**), if necessary re-schedule some instructions and renaming the used registers. Compute manually the number of clock cycles the new program (**program\_2\_c.s**) requires to execute, and compare the obtained results with the ones obtained by the simulator.

Complete the following table with the obtained results:

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| --- | --- | --- | --- | --- |
| **Program**    **Clock cycle computation** | **program\_2.s** | **program\_2\_a.s** | **program\_2\_b.s** | **program\_2\_c.s** |
| **By hand** |  |  |  |  |
| **By simulation** |  |  |  |  |

Compare the results obtained in the point 1, and provide some explanation in the case the results are different.

Eventual explanation: