

8 bit adder Subtractor

A_i

B_i

C_{i-1}

$$[A_i + B_i]_2 \leq [C_{i-1}]_{10}$$

$$S_i = A_i \oplus B_i \oplus C_{i-1} \quad \text{if } C_{i-1} = 0$$

$$S_i = C_{i-1}(A_i \oplus B_i) + A_i B_i \quad \text{if } C_{i-1} = 1$$

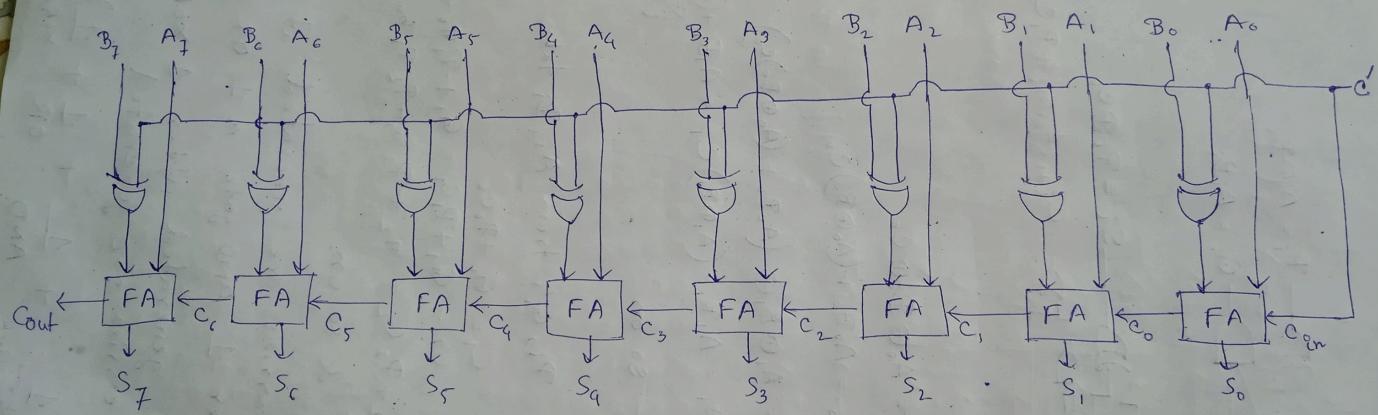
1 bit Full Adder circuit

no. of gates in a FA (1bit) = 5

No. of FA(1bit) used = 8

extra xor gates = 8

Total no. of gates = $8 * 5 + 8 = \underline{48}$



8 bit adder-Subtractor circuit

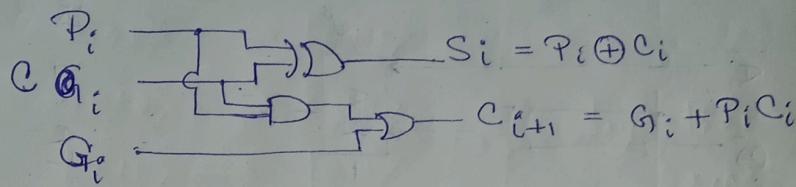
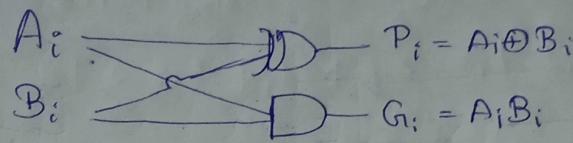
$C' = 0$; circuit is adder

$C' = 1$; " " subtractor

FA = 1 bit full adder circuit.

After 1 gate delay due to the XOR gates
inputs to 1st FA is ready
each FA introduces 3 gate delays.
 \Rightarrow Total delay = $8 \times 3 + 1 = 25$

8 bit Carry look ahead adder



$$S_0 = P_0 \oplus C_0 = A_0 \oplus B_0 \oplus C_0$$

$$C_1 = G_0 + P_0 C_0 = A_0 B_0 + (A_0 \oplus B_0) C_0$$

$$S_1 = P_1 \oplus C_1 = A_1 \oplus B_1 \oplus (A_0 B_0 + (A_0 \oplus B_0) C_0)$$

$$C_2 = G_1 + P_1 C_1 = A_1 B_1 + (A_1 \oplus B_1) C_1 = A_1 B_1 + (A_1 \oplus B_1) \{ A_0 B_0 + (A_0 \oplus B_0) C_0 \}$$

& so on

Generation of P_i, G_i 's from A_i, B_i takes 1 gate delay

$$\cancel{\text{C } i \text{ 's only}} \quad C_1 = G_0 + P_0 C_0$$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_0 P_1 C_0$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_1 P_0 G_0 + P_2 P_1 P_0 C_0$$

& so on.

Thus all carries are generated at same time
i.e. after 1 AND gate & 1 OR gate delay

Sums are generated after 1 XOR gate delay after carries are generated

Total $(\underbrace{1}_{\text{PG block}} + \underbrace{1}_{\text{AND}} + \underbrace{1}_{\text{OR}} + \underbrace{1}_{\text{XOR}}) = 4 \text{ gate delay}$



\Rightarrow CTA is faster