DRIVER RESETABLE INPUTS

NON-DRIVER RESETABLE INPUTS

Fix_AMS
U1
74LVC1G08GW,125
3.3V_0
GND

Fix_IMD
U2
74LVC1G08GW,125
3.3V_1
GND

Fix_BSPD
U3
74LVC1G08GW,125
3.3V_2
GND

Fix_PDOC
U8
74LVC1G08GW,125
3.3V_PDOC
GND

TestPoint
NON_RESETS1

Reset_In and Driver_Reset_In connect to buttons that
switch to ground when pressed, and are open-circuit when not pressed.

R2
CRCW0805
SAFTEY_IND

BZT52HC3V0WF-7
D1

C2
GCM0805_1u
GND
GND

U6
74LVC1G08GW,125
3.3V
GND

This works the same way as the other flip-flop,
but includes an input from the previous stage
as well as an input from the end of the switch/interlock loop.

SHOULDER RESET

R3
CRCW0805
100K
3.3V
GND

U5A
MC14013BDR2G
D   S   Q
R   Q

U4
74AHC1GU04GW,125
3.3V
GND

TestPoint
SHOULDER_RESET1

R1
CRCW0805
SHOULDER_RESET
SHOULDER_RESET_SIGNAL

C1
GCM0805_1u
GND

U32
SN74LVC1G126
EN
BUFFER VCC
GND
3.3V

R4
CRCW0805
220R
SHOULDER_OUT_LED

LED2
GREEN
GND

TestPoint
NON_RESETS_OUT1

DRIVER_RESET_IND
R5
CRCW0805

R6
CRCW0805
100K
3.3V

C3
GCM0805_1u
GND

DRIVER RESET

HIGH=3.3V= good
LOW=0V=fault

U5B
MC14013BDR2G
GND
D   Q
S
R   Q

U7
74AHC1GU04GW,125
3.3V
GND

DRIVER_OUTPUT
TestPoint
DRIVER_OUTPUT1

U33
SN74LVC1G126
EN
BUFFER VCC
GND
3.3V
DRIVER_OUTPUT_LED

R7
CRCW0805
220R

LED1
GREEN
GND

This is setup a bit weird for a flip-flop.
On power-on, Q is low, rest of system is off.
If any Fix_Input_X is low, then Q is forced low as well
due to R (Reset) being held high. Nothing can change this.

When ALL Fix_Input_X's are high, D becomes high, and R becomes low.
This allows the flip-flop to change the state of Q to that of D (high).
This state change will occur when the Reset_In line is pulsed low (button pushed), causing a single clock cycle to happen.

Subsequent button pushes will do nothing, as D and Q will already be the same state.

UNUSED LOGIC

U5C
MC14013BDR2G
VDD
VSS
3.3V
C45
GCM0805_0.1u
GND