### 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

- 1							
	funct7	rs2	rs1	funct3	rd	opcode	R-type
	imm[11:	0]	rs1	funct3	rd	opcode	I-type
	imm[11:5]	rs2	rs1	funct3	imm[4:0]	opcode	S-type
	imm[12 10:5]	rs2	rs1	funct3	rd	opcode	B-type
		imm[31:12]			rd	opcode	U-type
	im	m[20 10:1 11 1	9:12]		rd	opcode	J-type

# **Zbb**: "Basic bit-manipulation" Extension

31						25	24				20	19		15	14		12	11		7	6						0	
0	1	0	0	0	0	0			rs2				rs1		1	1	1		rd		0	1	1	0	0	1	1	ANDN
0	1	0	0	0	0	0			rs2				rs1		1	1	0		rd		0	1	1	0	0	1	1	ORN
0	1	0	0	0	0	0			rs2				rs1		1	0	0		rd		0	1	1	0	0	1	1	XNOR
0	1	1	0	0	0	0	0	0	0	0	0		rs1		Ø	0	1		rd		0	0	1	0	0	1	1	CLZ
0	1	1	0	0	0	0	0	0	0	0	1		rs1		0	0	1		rd		0	0	1	0	0	1	1	CTZ
0	1	1	0	0	0	0	0	0	0	1	0		rs1		0	0	1		rd		0	0	1	0	0	1	1	CPOP
0	0	0	0	1	0	1			rs2				rs1		1	1	0		rd		0	1	1	0	0	1	1	MAX
0	0	0	0	1	0	1			rs2				rs1		1	1	1		rd		0	1	1	0	0	1	1	MAXU
0	0	0	0	1	0	1			rs2	2			rs1		1	0	0		rd		0	1	1	0	0	1	1	MIN
0	0	0	0	1	0	1			rs2				rs1		1	0	1		rd		0	1	1	0	0	1	1	MINU
0	1	1	0	0	0	0	0	0	1	0	0		rs1		0	0	1		rd		0	0	1	0	0	1	1	SEXT.B
0	1	1	0	0	0	0	0	0	1	0	1		rs1		0	0	1		rd		0	0	1	0	0	1	1	SEXT.H
0	0	0	0	1	0	0	0	0	0	0	0		rs1		1	0	0		rd		0	1	1	0	0	1	1	ZEXT.H
0	1	1	0	0	0	0			rs2	:			rs1		0	0	1		rd		0	1	1	0	0	1	1	ROL
0	1	1	0	0	0	0			rs2				rs1		1	0	1		rd		0	1	1	0	0	1	1	ROR
0	1	1	0	0	0	0		S	har	it			rs1		1	0	1		rd		0	0	1	0	0	1	1	RORI
0	0	1	0	1	0	0	0	0	1	1	1		rs1		1	0	1		rd		0	0	1	0	0	1	1	ORC.B
0	1	1	0	1	0	0	1	1	0	0	0		rs1		1	0	1		rd		0	0	1	0	0	1	1	REV8

#### 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

funct7	rs2	rs1	funct3	rd	opcode	R-type
imm[11:	0]	rs1	funct3	rd	opcode	I-type
imm[11:5]	rs2	rs1	funct3	imm[4:0]	opcode	S-type
imm[12 10:5]	rs2	rs1	funct3	rd	opcode	B-type
	imm[31:12]			rd	opcode	U-type
in	nm[20 10:1 11 1	9:12]		rd	opcode	J-type

## Zri: "Load/Store indirect with Index" Extension

31						25	24 20	19 15	14		12	11	7	6						0	_
0	0	0	0	0	0	0	rs2	rs1	1	1	1	rd		0	0	0	0	0	1	1	LB.R
0	0	0	0	0	0	1	rs2	rs1	1	1	1	rd		0	0	0	0	0	1	1	LH.R
0	0	0	0	0	1	0	rs2	rs1	1	1	1	rd		0	0	0	0	0	1	1	LW.R
1	0	0	0	0	0	0	rs2	rs1	1	1	1	rd		0	0	0	0	0	1	1	LBU.R
1	0	0	0	0	0	1	rs2	rs1	1	1	1	rd		0	0	0	0	0	1	1	LHU.R
0	0	0	0	0	0	0	rs3	rs1	1	1	1	rs2		0	1	0	0	0	1	1	SB.R
0	0	0	0	0	0	1	rs3	rs1	1	1	1	rs2		0	1	0	0	0	1	1	SH.R
0	0	0	0	0	1	0	rs3	rs1	1	1	1	rs2		0	1	0	0	0	1	1	SW.R

lb rd, rs2(rs1)
lh rd, rs2(rs1)
lw rd, rs2(rs1)
lbu rd, rs2(rs1)

lhu rd, rs2(rs1)

sb rs2, rs3(rs1)

rs2, rs3(rs1) sh

rs2, rs3(rs1) SW

#### 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

funct7	rs2	rs1	funct3	rd	opcode	R-type
imm[11:	0]	rs1	funct3	rd	opcode	I-type
imm[11:5]	rs2	rs1	funct3	imm[4:0]	opcode	S-type
imm[12 10:5]	rs2	rs1	funct3	rd	opcode	B-type
	imm[31:12]			rd	opcode	U-type
in	m[20 10:1 11 1	9:12]		rd	opcode	J-type

# Zor: "Objective RISC" Extension

## <u>Unprivileged:</u>

31						25	24				20	19			15	14		12	11 7	6						0	_
0	0	0	0	0	0	0			rs2				r	าร1		0	0	0	rs3	0	0	0	1	0	1	1	SP.R
0	0	0	0	0	0	1			rs2				r	າs1		0	0	0	rd	0	0	0	1	0	1	1	LP.R
0	0	0	0	0	1	0	i	.nde	2x[4	1:0	]		fr	ame		Ø	0	0	rs1	0	0	0	1	0	1	1	SV
0	0	0	0	0	1	1	i	.nde	2x[4	1:0	]		fr	ame		0	0	0	rd	0	0	0	1	0	1	1	RST
0	0	0	0	1	0	0		Z	zer	)			r	າs1		0	0	0	rd	0	0	0	1	0	1	1	QDTB
0	0	0	0	1	0	1		Z	zer	)			r	rs1		Ø	0	0	rd	0	0	0	1	0	1	1	QDTH
0	0	0	0	1	1	0		Z	zer	)			r	າs1		0	0	0	rd	0	0	0	1	0	1	1	QDTW
0	0	0	0	1	1	1		Z	zer	)			r	າs1		0	0	0	rd	0	0	0	1	0	1	1	QDTD
0	0	0	1	0	0	0		Z	zer	)			r	າs1		0	0	0	rd	0	0	0	1	0	1	1	QPI
0	0	1	0	0	0	0			rs2				r	rs1		0	0	0	zero	0	0	0	1	0	1	1	JLIB
0	1	0	0	0	0	0		Z	zer	)			Z	ero		0	0	0	rd	0	0	0	1	0	1	1	GCP
1	0	0	0	0	0	0		Z	zer	)			fr	rame		0	0	0	zero	0	0	0	1	0	1	1	POP
1	0	0	0	0	0	1		Z	zer	)			Z	ero		0	0	0	zero	0	0	0	1	0	1	1	RTLIB
1	0	0	0	0	1	0		Z	zer	)			Z	ero		0	0	0	zero	0	0	0	1	0	1	1	CPFC
1	0	0	0	0	1	1		Z	zer	)			Z	ero		0	0	0	zero	0	0	0	1	0	1	1	CHECK
		imm	[11	:5	]				rs2				r	າs1		0	0	1	imm[4:0]	0	0	0	1	0	1	1	SP
				in	nm [	11:	0]						r	າs1		0	1	0	rd	0	0	0	1	0	1	1	LP
				in	nm [	11:	0]						r	rs1		0	1	1	zero	0	0	0	1	0	1	1	JLIBI
0	0	0	0	0	0	0			rs2				r	າs1		1	0	0	rd	0	0	0	1	0	1	1	ALC
				р	i[1	1:6	9]						r	າs1		1	0	1	rd	0	0	0	1	0	1	1	ALCI.P
				d	t[1	1:0	ð] <sup>-</sup>						r	າs1		1	1	0	rd	0	0	0	1	0	1	1	ALCI.D
		dt	[6:	0]			0	0	0	0	0			rd		1	1	1	pi[4:0]	0	0	0	1	0	1	1	ALCI
		dt	[6:	0]			0	0	0	1	0		fr	ame		1	1	1	pi[4:0]	0	0	0	1	0	1	1	PUSHG
		dt	[6:	0]			0	0	0	1	1		fr	ame		1	1	1	pi[4:0]	0	0	0	1	0	1	1	PUSHT

### Machine Mode:

31					26	25	24				20	19				15	14		12	11	7	6						0	
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	rd		1	1	1	0	0	1	1	ALCB
1	1	1	1	1	1	1			rs2					rs1			0	0	0	rd		1	1	1	0	0	1	1	CIOP
1	1	1	1	1	1	0	1	0	0	0	0			rs1			0	0	0	rd		1	1	1	0	0	1	1	CCP
1	1	1	1	1	1	0	1	0	0	0	1			rs1			0	0	0	rd		1	1	1	0	0	1	1	RPR
1	1	1	1	1	1	0	1	0	1	0	0			rs1			0	0	0	rd		1	1	1	0	0	1	1	QPIR
1	1	1	1	1	1	0	1	0	1	0	1			rs1			0	0	0	rd		1	1	1	0	0	1	1	QDTR
1	1	1	1	1	1	Ø	1	0	1	1	0			rs1			0	0	0	rd		1	1	1	0	0	1	1	QPTR
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	rd		1	1	1	0	0	1	1	SEAL
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	rd		1	1	1	0	0	1	1	UNSL

## Misc:

reg	alias	reg	alias
x0	zero	x16	a6
x1	rix	x17	a7
x2	frame	x18	s2
х3	rcd/root/core	x19	s3
x4	ctxt	x20	s4
x5	t0	x21	s5
х6	t1	x22	s6
x7	t2	x23	s7
x8	s0	x24	s8
x9	s1	x25	s9
x10	a0	x26	s10/bm
x11	a1	x27	cnst
x12	a2	x28	t3
x13	a3	x29	t4
x14	a4	x30	t5
x15	a5	x31	t6

implemented as
lp rd, imm(rs1)
sp x0, imm(rs1)
sp rs2, imm(rs1)
addi rs2, x0,0
alci frame, pi,dt
·
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R R R R R R R R R R S I I R I I S S S

R

R R R R R R ale rd, rsh, rsz

