EXPERIMENT NO: - 1

a) ***AND gate characteristics*:** To study the AND gate (using 7408 IC, a quad two input AND gate). Taking any one of the four gate (in Fig (a) gate with input at pin no 1 & 2 and output pin at 3 is taken) connect the circuit as shown in Fig (a). Now apply input voltage of 5V (logical 1) to the pin no 1 and apply the varying voltage to pin no 2 of the same AND gate through the centre point of the 25K potentiometer present on the component development system given. Now by varying the potentiometer measure the each input voltage at pin no 2 and the corresponding output voltage at pin no 3 with respect to the common ground by using a digital voltmeter provided to you. Connect pin no 14 to V_{cc} = 5V and pin no 7 to Gnd for AND IC 7408 which is not shown in the Fig (a) to give necessary power to the IC. Now make a table of V_{in} vs V_{out} from different measured values of Vin and V_{out}. From the different values of the V_{in} and V_{out} plot a curve showing the variation of Vout with V_{in} either using manually or using any Plot software in a PC. From this characteristics determine the magnitude of the voltage gain at a point between the two logic states. Justify whether the characteristics for the AND gate is inverting or non-inverting. Note: Vary input voltage from 0V to 5V in steps of 0.2V. Note: Output voltage for logical 0 or binary 0 output $\Rightarrow$ 0V to 0.2V and output voltage for logical 1 or binary 1 output $\Rightarrow$ 3.2V to 4.4V.

b) NAND gate as a universal gate: To show this we have to realise the truth table of all the other gates (such as NOT, OR, NOR, AND, XOR and XNOR gates) by using NAND gates only. For this use the circuit of Fig b (1) to Fig b (6) respectively to verify the truth table of the following gates. In all these circuits you have to use 7400 IC, a quad two input NAND gate. To Verify the truth table of different gates connect pin no 14 to V_{CC} = 5V and pin no 7 to gnd for each 7400 IC. Also connect the output of each of the Fig b (1) to Fig b (6) to any one of the eight output LED's present in the component development system (CDS) given. Now apply the different combination of binary inputs 0 or 1 by connecting the inputs of each figure to the input switches present on the CDS. Any switch placed at the upward direction implies logical 1 or binary 1 input and any switch placed in the downward direction implies logical 0 or binary 0 input. Output status for each Fig b (1) to Fig b (6) is dictated by the on or off condition of the output LED's. ***When output LED's will be on implies output is at logical 1 or binary 1 and when output LED's will be off implies output is at logical 0 or binary 0.***

Note: Circuit of Fig b (1) is used to realise NOT from NAND gate. Circuit of Fig b (2) is used to realise AND gate from NAND gate. Circuit of Fig b (3) is used to realise OR gate from NAND gate. Circuit of Fig b (4) is used to realise NOR gate from NAND gate. Circuit of Fig b (5) is used to realise XOR gate from NAND gate. Circuit of Fig b (6) is used to realise XNOR from NAND gate.

For inputs, V_{IN} = 0V to 0.8V $\Rightarrow$ logical 0 or binary 0 and V_{IN} = 4V to 5V $\Rightarrow$ logical 1 or binary 1.
For outputs, Y_{OUT} = 0V to 0.2V $\Rightarrow$ logical 0 or binary 0 and Y_{OUT} = 3.2V to 4.4V $\Rightarrow$ logical 1 or binary 1. Draw the layout of the circuit in a piece of paper for proper connection with single strand wire.

Truth Table of different gates to be verified by using different circuit from Fig b (1) to Fig b (6) is as under.

Truth Table		Truth Table			Truth Table			Truth Table			Truth Table			Truth Table		
A	Y_{not}	A	B	Y_{and}	A	B	Y_{or}	A	B	Y_{nor}	A	B	Y_{xor}	A	B	Y_{xnor}
0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
1	0	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0
		1	0	0	1	0	1	1	0	0	1	0	1	1	0	0
		1	1	1	1	1	1	1	1	0	1	1	0	1	1	1
Table b (1)		Table b (2)			Table b (3)			Table b (4)			Table b (5)			Table b (6)		

c) Verification of Demorgan's Theorem: $\overline{A + B} = \overline{A} \cdot \overline{B}$. To verify above Demorgan's theorem connect the circuit as shown in Fig (c). This circuit uses three different IC's 7432 (a quad two input OR gate), 7404 (a hex inverter or NOT gate and 7408 (a quad two input AND gate). For all these IC's connect pin no 14 to V_{CC} = 5V and pin no 7 to gnd. Now apply input at A and B through two input switches present in the CDS. Connect Y1 and Y2 to the two output LED's present on the CDS. Now apply all possible combination (4 possible combination can be used for two inputs) of logical or binary inputs by connecting the input switches appropriately. Now if the status of LED at both Y1 and Y2

outputs are equal for each and every combination of the inputs then the Demorgan's theorem will be verified. ***(Use +5V d.c. (Red) supply terminal and the Gnd (Black) terminal only from the CDS.***

CIRCUIT DIAGRAMS FOR EXPERIMENT NO -1

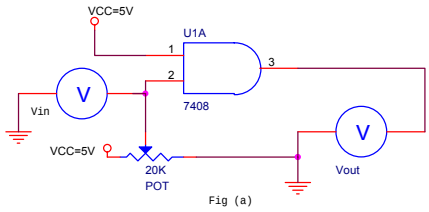


Fig (a)

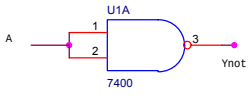


Fig b(1)

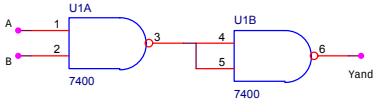


Fig b(2)

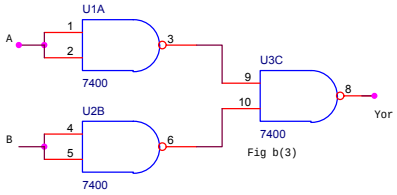


Fig b(3)

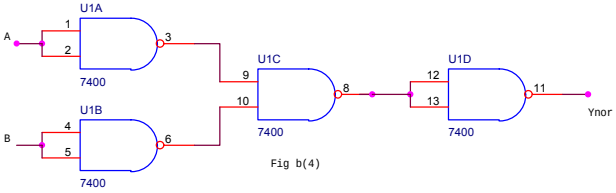


Fig b(4)

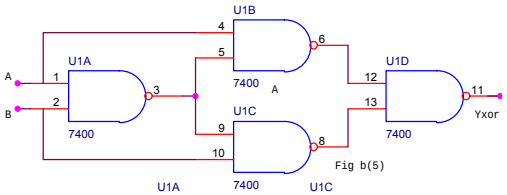


Fig b(5)

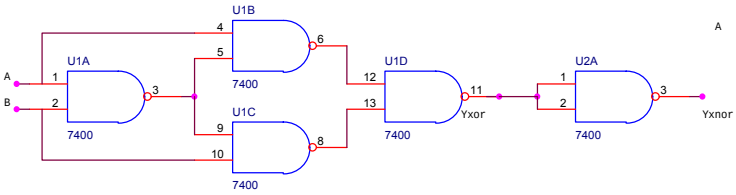


Fig b(6)

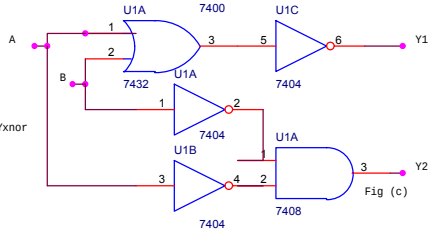


Fig (c)

EXPERIMENT NO: - 2

d) ***NAND gate characteristics*:** To study the NAND gate characteristics (using 7400 IC, a quad two input NAND gate). Taking any one of the four gate (in Fig (a) gate with input at pin no 1 & 2 and output pin at 3 is taken) connect the circuit as shown in Fig (a). Now apply input voltage of 5V (logical 1) to the pin no 1 and apply the varying voltage to pin no 2 of the same NAND gate through the centre point of the 25K potentiometer present on the component development system given. Now by varying the potentiometer knob measure the each input voltage at pin no 2 and the corresponding output voltage at pin no 3 with respect to the common ground by using a digital voltmeter provided to you. Connect pin no 14 to V_{cc} = 5V and pin no 7 to Gnd for NAND IC 7400 which is not shown in the Fig (a) to give necessary power to the IC. Now make a table of V_{in} vs V_{out} from different measured values V_{in} and V_{out}. From the different values of the V_{in} and V_{out} plot a curve showing the variation of Vout with V_{in} either using manually or using any Plot software in a PC. From this characteristics determine the magnitude of the voltage gain at a point between the two logic states. Justify whether the characteristics for the NAND gate is inverting or non-inverting. Note: Vary input voltage from 0V to 5V in steps of 0.2V. Note: Output voltage for logical 0 or binary 0 output $\Rightarrow$ 0V to 0.2V and output voltage for logical 1 or binary 1 output $\Rightarrow$ 3.2V to 4.4V.

e) *NOR gate as a universal logic gate:* To show this we have to realise the truth table of all the other gates (such as NOT, OR, AND, NAND, XNOR and XOR gates) by using NOR gates only. For this use the circuit of Fig b(1) to Fig b(6) respectively to verify the truth table of the following gates. In all these circuits you have to use 7402 IC, a quad two input NOR gate. To Verify the truth table of different gates connect pin no 14 to V_{CC} = 5V and pin no 7 to gnd for each 7402 IC. Also connect the output of each of the Fig b(1) to Fig b(6) to any one of the eight output LED's present in the component development system (CDS) given. Now apply the different combination of binary inputs 0 or 1 by connecting the inputs of each figure to the input switches present on the CDS. Any switch placed at the upward direction implies logical 1 or binary 1 input and any switch placed in the downward direction implies logical 0 or binary 0 input. Output status for each Fig b(1) to Fig b(6) is dictated by the on or off condition of the output LED's. ***When output LED's will be on implies output is at logical 1 or binary 1 and when output LED's will be off implies output is at logical 0 or binary 0.***

Note: Circuit of Fig b(1) is used to realise NOT from NOR gate. Circuit of Fig b(2) is used to realise OR gate from NOR gate. Circuit of Fig b(3) is used to realise AND gate from NOR gate. Circuit of Fig b(4) is used to realise NAND gate from NOR gate. Circuit of Fig b(5) is used to realise XNOR gate from NOR gate. Circuit of Fig b(6) is used to realise XOR from NOR gate.

For inputs, V_{IN} = 0V to 0.8V $\Rightarrow$ logical 0 or binary 0 and V_{IN} = 4V to 5V $\Rightarrow$ logical 1 or binary 1.

For outputs, Y_{OUT} = 0V to 0.2V $\Rightarrow$ logical 0 or binary 0 and Y_{OUT} = 3.2V to 4.4V $\Rightarrow$ logical 1 or binary 1. Draw the layout of the circuit in a piece of paper for proper connection with single strand wire.

Truth Table of different gates to be verified are shown in Table b(1) to Table b(6) below:

A	Y_{not}
0	1
1	0

Table b(1)

A	B	Y_{or}
0	0	0
0	1	1
1	0	1
1	1	1

Table b(2)

A	B	Y_{and}
0	0	0
0	1	0
1	0	0
1	1	1

Table b(3)

A	B	Y_{nand}
0	0	1
0	1	1
1	0	1
1	1	0

Table b(4)

A	B	Y_{xnor}
0	0	1
0	1	0
1	0	0
1	1	1

Table b(5)

A	B	Y_{xor}
0	0	0
0	1	1
1	0	1
1	1	0

Table b(6)

f) ***Verification of Demorgan's Theorem:*** $A \cdot B = \overline{A} + \overline{B}$. To verify above Demorgan's theorem connect the circuit as shown in Fig (c) to realise the L.H.S. and R.H.S. of the above theorem by the outputs Y1 and Y2 respectively. This circuit uses three different IC's 7432 (a quad two input OR gate), 7404 (a hex inverter or NOT gate and 7408 (a quad two input AND gate). For all these IC's connect pin no 14 to V_{CC} = 5V and pin no 7 to gnd. Now apply input at A and B through two input switches present in the CDS. Connect Y1 and Y2 to the two output LED's present on the CDS. Now apply all possible

combination (4 possible combination can be used for two inputs) of logical or binary inputs by connecting the input switches appropriately. Now if the status of LED at both Y1 and Y2 outputs are equal for each and every combination of the inputs then the Demorgan's theorem will be verified. ***(Use +5V d.c. (Red) supply terminal and the gnd (Black) terminal only from the CDS.***

CIRCUIT DIAGRAMS FOR EXPERIMENT NO -2

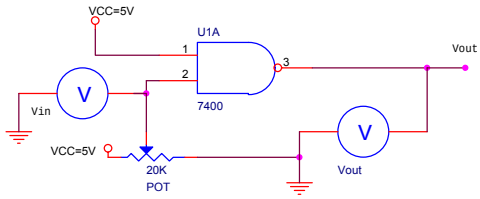


Fig (a)

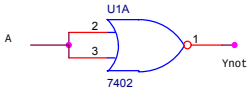


Fig b(1)

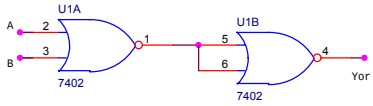


Fig b(2)

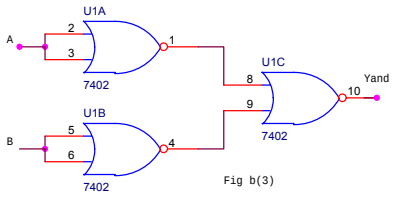


Fig b(3)

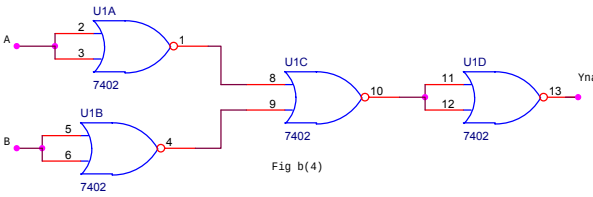


Fig b(4)

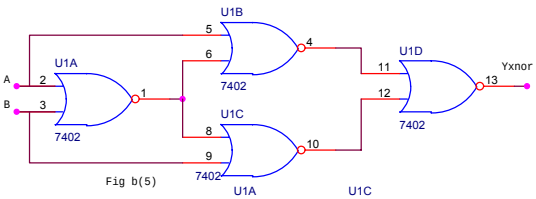


Fig b(5)

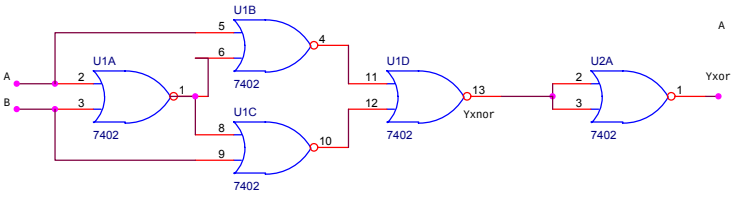


Fig b(6)

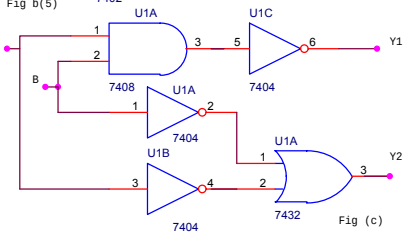


Fig (c)

EXPERIMENT NO: - 3

A. ***Realisation of Half Adder circuit by using Nand gates only:*** A Half adder circuit is used to add two binary bits at a time. It has got two inputs as say A and B and two outputs as S (Sum) and C (Carry).The logical expression for Sum(S) and Carry(C) are $S = A \cdot \overline{B} + \overline{A} \cdot B = A \oplus B$ and $C = A \cdot B$ respectively. The truth table of Half Adder circuit is shown in Table (1). Connect the circuit as shown in Fig (a) (using NAND gates only i.e. by using 7400 IC) to verify the truth table of Half Adder circuit. Connect the inputs A and B of Fig (a) through two input switches and connect the two outputs S and C of the circuit of Fig (a) to the two LED's present on the CDS. Connect pin no 14 of all 7400 IC's to V_{CC} = 5V and pin no 7 of all 7400 IC's to ground. (for Fig (a)). Now apply various combination of inputs at A and B by varying the two input switch position and observe the corresponding LED outputs of Fig (a) to verify the truth table of Half Adder circuit.

B. ***Realisation of Half Subtractor circuit by using Nand gates only:*** A Half subtractor circuit is used to subtract two binary bits at a time. It has got two inputs as say A and B and two outputs as D (Difference) and β (Borrow). The logical expression for Difference and Borrow are $D = A \cdot \overline{B} + \overline{A} \cdot B = A \oplus B$ and $\beta = \overline{A} \cdot B$ respectively. The truth table of Half Subtractor circuit is shown in Table (2). Connect the circuit as shown in Fig (b) (using NAND gates only i.e. by using 7400 IC) to verify the truth table of Half subtractor circuit (keep intact the Sum part realisation of Half Adder circuit of Fig (a) as both S and D satisfy XOR logic between the inputs A and B and modify only the carry part of the circuit of Fig (a) to realise Borrow β). Connect the inputs A and B of Fig (a) through two input switches and connect the two outputs D and β of the circuit of Fig (a) to the two LED's present on the CDS. Connect pin no 14 of all 7400 IC's to V_{CC} = 5V and pin no 7 of all 7400 IC's to ground. (for Fig (b)). Now apply various combination of inputs at A and B by varying the two input switch position and observe the corresponding LED outputs of Fig (b) to verify the truth table of Half Subtractor circuit.

Truth Table of Half Adder Circuit.

Dec	A	B	S	C
0	0	0	0	0
1	0	1	1	0
2	1	0	1	0
3	1	1	0	1

Table (1)

Truth Table of Half Subtractor Circuit.

Dec	A	B	D	β
0	0	0	0	0
1	0	1	1	1
2	1	0	1	0
3	1	1	0	0

Table (2)

C. ***Realisation of Five bit Even / Odd parity checker circuit:*** Connect the circuit as shown in Fig (c) using four two input XOR gates (i.e. using a single 7486 IC) and one NOT gate (i.e. using a one NOT gate of a single 7404 IC). Connect pin no 14 and pin no 7 to V_{CC} =5 V and Gnd respectively for both 7486 and 7404 IC's. Apply the five inputs through five input switches and connect the Y_{even} output of Fig (c) to one LED of CDS. Then verify that the output LED will glow when the inputs contain even number of 1's or all inputs are o's to indicate even parity of the 5 input bits. If the output LED does not glow for any inputs which contain odd number of 1's indicate Odd parity of five input bits. Write down the truth table showing the relationship between Y_{even} and the five inputs A, B, C, D and E. The logical expression for the out put Y_{even} is :

$$Y_{even} = A \oplus B \oplus C \oplus D \oplus E$$

D. ***Realisation of the logical function*** $f(A, B, C) = \overline{A} \cdot B + A \cdot \overline{C} + B \cdot \overline{C}$ without minimization by using combination of AND, OR and NOT gates. Write down the truth table for this logical function and verify this truth table by connecting the circuit as shown in Fig (d). Connect pin no 14 of all IC's of Fig (d) to Vcc = 5V and pin no 7 of all IC's of Fig (d) to GND.

Connect inputs A, B and C to three input switches and the output f (A, B, C) to one LED of the CDS. Minimize the given logical function by using Karnaugh Map method and then realise this minimized logical expression by using combination of AND, OR and NOT gates. Comment on the realisation of the same logical function without or with minimization.

E. ***Design a combinational circuit having three inputs M, A, B and two outputs f_1 and f_2 which satisfy the following truth table (Table (3)). Use whatever gates you want.*** Identify the functions of this circuit for two different values of M i.e. for M=0 and for M=1.

Table (3)

Dec	M	A	B	f_1	f_2
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	0	0
5	1	0	1	1	1
6	1	1	0	1	0
7	1	1	1	0	0

CIRCUIT DIAGRAMS FOR EXPERIMENT NO -3

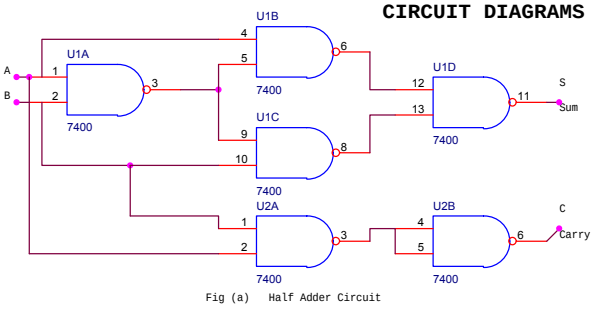


Fig (a) Half Adder Circuit

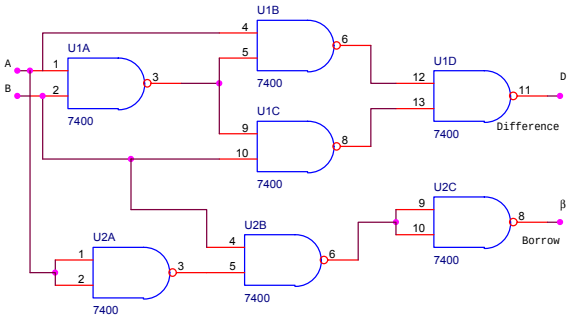


Fig (b) Half Subtractor Circuit

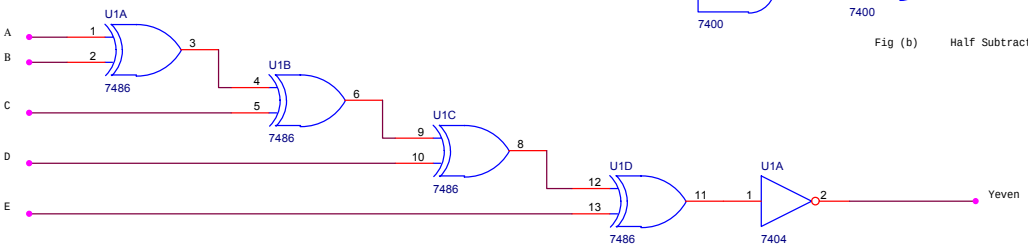


Fig (C) 5 bit Even Parity Checker Circuit.

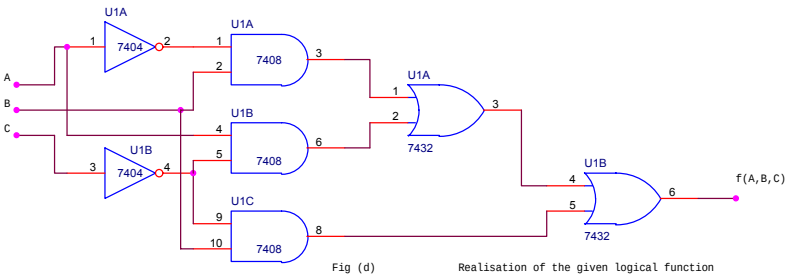


Fig (d) Realisation of the given logical function

EXPERIMENT NO: - 4

A. ***Realisation of Multiplexer as a universal logic:*** Connect the circuit as shown in Fig a(1) to Fig a (4) to realise the truth table of NOT, OR and NOR, AND and NAND, XOR and XNOR gates respectively by using a 74153 (a dual 4:1 multiplexer) multiplexer IC. Connect the input(s) through input switches and outputs to the LED's present in CDS for each of the above circuit shown in Fig a(1) to Fig a(4). For realising any logic gates take the one of the two 4:1 multiplexer as shown in each circuit of Fig a(1) to Fig a(4). Connect pin no 16 and pin no 8 to V_{CC} = 5V and GND respectively for all the above circuits. Connect the strobe/enable input (pin no 1 & 15 of 74153 IC) of the multiplexer through a switch to enable or disable the multiplexer. To verify the truth table of any gate you have to connect the strobe/enable input to logical 0. Verify that when strobe/enable input is connected to logical 1 the output of the multiplexer is always 0 i.e. output being independent of select/address inputs.

B. ***Design of Full Adder and Full Subtarctor circuit using a 4:1 multiplexer (74153 IC) and a not gate:*** Convert the three input truth table for Full Adder and Full Subtractor circuit into two input truth table as shown in Table-1 and Table-2 respectively by expressing the outputs as a function of third inputs. Connect the circuit as shown in Fig b(1) and Fig b(2). Connect the input of FA and FS circuit through three input switches and the two outputs to two LED's present in CDS for each of the above circuit shown in Fig b(1) to Fig b(2). To verify the truth table of Full adder and Full Subtarctor circuit connect pin no 16 and pin no 8 to V_{CC} = 5V and GND respectively for all the circuits shown in Fig b(1) to Fig b(2). Be careful to connect the strobe/enable inputs of both the multiplexer (i.e. pin no 1 and pin no 15) of Fig b(1) and Fig b(2) to logical 0 to enable both the multiplexer of 74153 IC for any select/address inputs. Connect pin no 14 and pin no 7 of 7404 IC to V_{CC} = 5V and GND respectively for the circuit of Fig b(1) and Fig b(2).

Truth table of Full Adder Table-1

A	B	C_{i-1}	S	C_i	S	Ci
0	0	0	0	0	C_{i-1}	0
0	0	1	1	0		
0	1	0	1	0	$\overline{C}_{I-1}$	C_{i-1}
0	1	1	0	1		
1	0	0	1	0	$\overline{C}_{I-1}$	C_{i-1}
1	0	1	0	1		
1	1	0	0	1	C_{i-1}	1
1	1	1	1	1		

Truth table of Full Subtractor Table-2

A	B	β_{i-1}	D	β_i	D	βi
0	0	0	0	0	β_{i-1}	β_{i-1}
0	0	1	1	1		
0	1	0	1	1	$\overline{\beta}_{i-1}$	1
0	1	1	0	1		
1	0	0	1	0	$\overline{\beta}_{i-1}$	0
1	0	1	0	0		
1	1	0	0	0	β_{i-1}	β_{i-1}
1	1	1	1	1		

Two input truth table of FA circuit.

A	B	S	C_i
0	0	C_{i-1}	0
0	1	C_{i-1}	C_{i-1}
1	0	C_{i-1}	C_{i-1}
1	1	C_{i-1}	1

Two input truth table of FS circuit.

A	B	D	β_i
0	0	β_{i-1}	β_{i-1}
0	1	β_{i-1}	1
1	0	β_{i-1}	0
1	1	β_{i-1}	β_{i-1}

C. ***Realise the following logical function by using a 8:1 Multiplexer and one NOT gate:***
f (A, B, C, D) = Σ m (3,4,5,6,9,11,14,15)

D. ***Realise the following incompletely specified logical function by using multiplexer:***
f (A, B, C) = ΠM (0, 2, 4) · Πd (1, 3, 5).

E. ***Theoretically realise a 16:1 multiplexer by using several lower order multiplexers only and hence theoretically realise the logical function f (A,B,C,D)=ΠM (0,1,3,4,6,8,12,14,15): Show the design using appropriate IC's and their interconnections with appropriate pins of different IC's.***

F. ***Analyse the circuit of Fig (c) and hence determine the functional relationship between inputs (A, B, C, D, E) and output Y. Express Y in Min term or Max term form and also write down the truth table for the circuit of Fig (c).***

CIRCUIT DIAGRAMS FOR EXPERIMENT NO -4

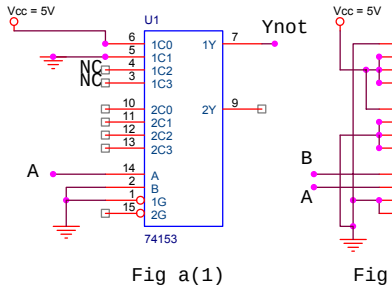


Fig a(1)

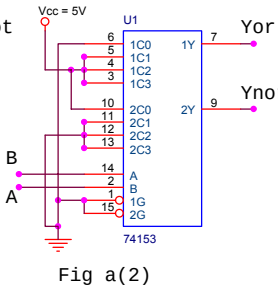


Fig a(2)

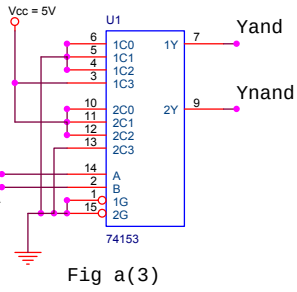


Fig a(3)

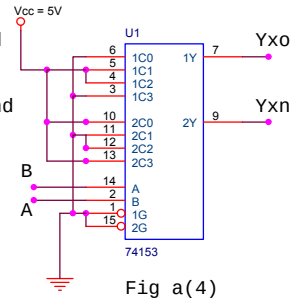


Fig a(4)

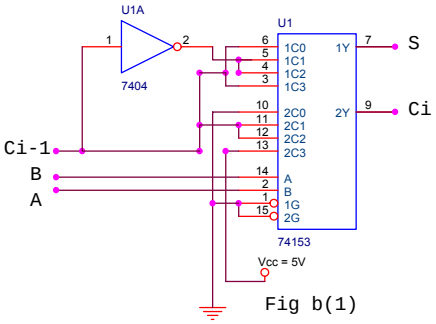


Fig b(1)

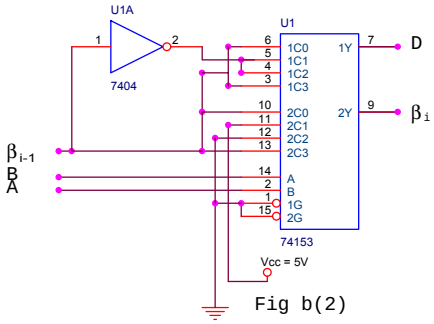
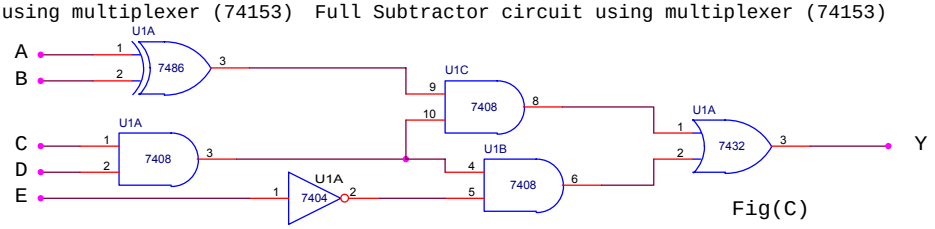


Fig b(2)

Full Adder circuit using multiplexer (74153) Full Subtractor circuit using multiplexer (74153)



Fig(C)

EXPERIMENT NO: - 5

A. ***Realising a BCD to decimal decoder circuit using decoder driver IC 7447 (with active low outputs) and common anode seven segment LED display LTS – 542:*** Connect the circuit as shown in Fig (a) Apply any BCD inputs at A, B, C and D inputs connected through four switches (where A is MSB and D is the LSB input) and check whether you can able to display all decimal numbers from 0 to 9. Connect RBO output (pin no 4) to one LED's of he CDS and verify that RBO output is 1 always for normal decoding and becomes 0 only during zero blanking interval. Also verify the function table of 7447-decoder driver IC shown in Table-1.

Function Table of Decoder Driver IC 7447. Table –1.

LT	RBI	BI / RBO	BCD inputs	Display Mode
0	×	×	×	Display 8 to verify all 7 segments.
1	1	Normally 1 as output, but output becomes 0 during 0 blanking interval.	Any BCD inputs.	Normal decoding. Display 0 to 9.
1	0	Normally 1 as output, but output becomes 0 during 0 blanking interval.	Any BCD inputs.	Normal decoding, 0 is not displayed.
×	×	0 as input	×	Display blank.

B. ***Verify the following function table of 74138(a 3 to 8 line decoder with active low outputs) and hence realise the following multiple output logical function by using this decoder IC and the gates shown:*** For verifying the function table of 74138 use the circuit of Fig b (1) and to realise the given multiple output function use the circuit of Fig b (2). For both these circuits connect the inputs A, B and C applied to the decoder inputs through three input switches. Connect the two outputs f_1 and f_2 to two output LED's of CDS.

$f_1(A, B, C) = \sum m (1, 2, 4, 7)$ and $f_2 (A, B, C) = \sum m (3, 5, 6, 7)$. Identify the function f_1 and f_2 .

Function table of 74138 decoder Table – 2.

G_1	$\overline{G}_{2A}$	$\overline{G}_{2B}$	A	B	C	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	×	×	×	×	×	1	1	1	1	1	1	1	1
×	1	×	×	×	×	1	1	1	1	1	1	1	1
×	×	1	×	×	×	1	1	1	1	1	1	1	1

C. ***Verify the Truth Table -3 of 74148 (an octal to binary priority encoder with active low inputs and outputs) using the circuit of Fig (c):*** Also verify that this can also be used as an ordinary octal to binary encoder when only one input is activated at any instant of time. Connect the circuit as shown in Fig (c). Connect the inputs 3, 4, 5, 6 and 7 through 5 input switches and connect all the five outputs $\overline{A}_2$, $\overline{A}_1$, $\overline{A}_0$, $\overline{GS}$, $\overline{EO}$ to five LED's of CDS. Connect inputs 0, 1 and 2 to V_{cc}= 5 V***. Connect the supply pins of all IC's to 5 V and Gnd pins of all IC's to power supply GND.***

Truth table of 74148 Table –3.

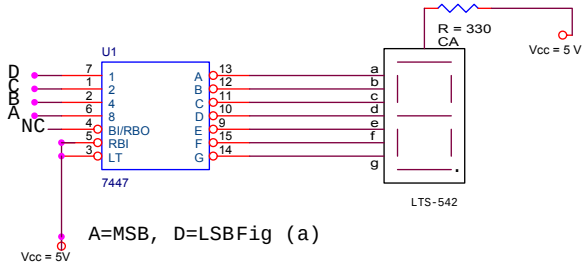
$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{A}_2$	$\overline{A}_1$	$\overline{A}_0$	$\overline{GS}$	$\overline{EO}$
1	×	×	×	×	×	×	×	×	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	×	0	1	1	1	1	1	1	1	1	0	0	1
0	×	×	0	1	1	1	1	1	1	0	1	0	1
0	×	×	×	0	1	1	1	1	1	0	0	0	1
0	×	×	×	×	0	1	1	1	0	1	1	0	1
0	×	×	×	×	×	0	1	1	0	1	0	0	1
0	×	×	×	×	×	×	0	1	0	0	1	0	1
0	×	×	×	×	×	×	×	0	0	0	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

D. Design a Normal Encoder (with active high inputs and outputs) having four inputs 0, 1, 2 and 3 and two outputs b_1 and b_0 satisfying the following truth table. Use whatever chips or device you require. How this circuit can be modified to realise a priority encoder having four inputs and two outputs.

Table – 4.

0	1	2	3	b_1	b_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

CIRCUIT DIAGRAMS FOR EXPERIMENT NO -5



A=MSB, D=LSBFig (a)

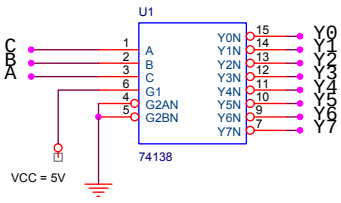


Fig b (1)

A=MSB, C=LSB

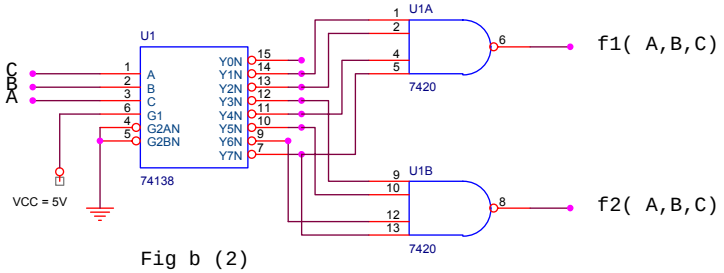
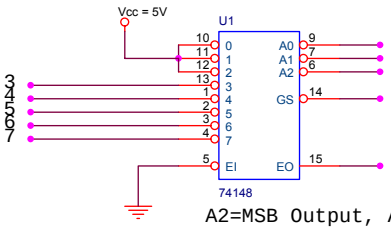


Fig b (2)

A=MSB, C=LSB



A2=MSB Output, A0=LSB Output

Fig (C)

EXPERIMENT NO: - 6

A. ***Verification of excitation table of J-K flip-flop:*** To verify the excitation table – 1 of J-K flip-flop connect the circuit as shown in Fig (a). Connect the PR, CLR, J and K inputs of J-K flip-flop (IC 7476, a dual J-K flip-flop) to four input switches and the output Q to one of the LED of CDS. Connect pin no 5 and pin no 13 to V_{CC} = 5V and GND respectively for 7476 IC. Apply external clock from the TTL clock output of CDS to the clock input (pin no 1 of 7476 IC). Verify that 7476 is a negative edge triggered J-K flip-flop. How would you connect J-K flip-flop to use it as a ÷ 2 or Mod 2 counter?

B. ***Verification of excitation table of D flip-flop:*** To verify the excitation table – 2 of D flip-flop connect the circuit as shown in Fig (b). Connect the PR, CLR and D inputs of D flip-flop (IC 7474, a dual D type flip-flop) to three input switches and the output Q to one of the LED of CDS. Connect pin no 14 and pin no 7 to V_{CC} = 5V and GND respectively for 7474 IC. Apply external clock from the TTL clock output of CDS to the clock input (pin no 3 of 7474 IC). Verify that 7474 is a positive edge triggered D type flip-flop.

C. ***Realisation of T type flip-flop from D type flip flop (using 7474, a dual D flip-flop):*** To verify the excitation table –3 of T type flip-flop using D type flip-flop, connect the circuit as shown in Fig (c). The minimised expression for D input is: $D = T \oplus Q_n$. (Verify this by using the flip-flop conversion (T type from D type) state table. Connect the PR, CLR and T inputs (as shown in Fig (C)) to three input switches and the output Q to one of the LED of CDS. Connect pin no 14 and pin no 7 to V_{CC} = 5V and GND respectively for 7474 and 7486(a quad 4 input XOR gates) IC. Apply external clock from the TTL clock output of CDS to the clock input (pin no 3 of 7474 IC). Verify the excitation table –3 of T type flip-flop, and also verify that T type flip-flop so realised from D type flip-flop IC 7474 (a positive edge triggered flip-flop) is also a positive edge triggered flip-flop.

Excitation Table-1 (for J-K F/F)

CLK	$\overline{PR}$	$\overline{CLR}$	J	K	Q_{N+1}
×	0	1	×	×	1
×	1	0	×	×	0
1	1	1	0	0	Q_N
1	1	1	0	1	0
1	1	1	1	0	1
1	1	1	1	1	$\overline{Q}_N$

Excitation Table-2 (for D F/F)

CLK	$\overline{PR}$	$\overline{CLR}$	D	Q_{N+1}
×	0	1	×	1
×	1	0	×	0
1	1	1	0	0
1	1	1	1	1

Excitation Table-3 (for T F/F).

CLK	$\overline{PR}$	$\overline{CLR}$	T	Q_{N+1}
×	0	1	×	1
×	1	0	×	0
1	1	1	0	Q_N
1	1	1	1	$\overline{Q}_N$

D. Design of asynchronous up counter using J-K flip-flops (IC 7476) having initial count 0 and modulus 6, with a prevention of lockout condition: ***This counter design requires the following minimised expression for preset and clear inputs of three J-K flip-flop: $PR_0 = PR_1 = PR_2 = 1$ and $CLR_0 = CLR_1 = CLR_2 = \overline{Q}_2 + \overline{Q}_1$. (Verify this by using the appropriate design procedure for asynchronous counter design). To realise the above counter connect the circuit as shown in Fig (d). Connect all J's and K's inputs of 7476 IC's to logical 1. Connect pin no 5 and pin no 13 of 7476 IC to V_{CC} = 5V and GND respectively. Connect pin no 14 and 7 of 7432 to V_{CC} = 5V and GND respectively. Connect the output Q_2 (MSB), Q_1 and Q_0 (LSB) of the counter to three LED's of CDS. Apply external clock input from TTL clock outputs of CDS to the clock input of LSB J-K flip-flop and the clock inputs for other flip-flop are as***

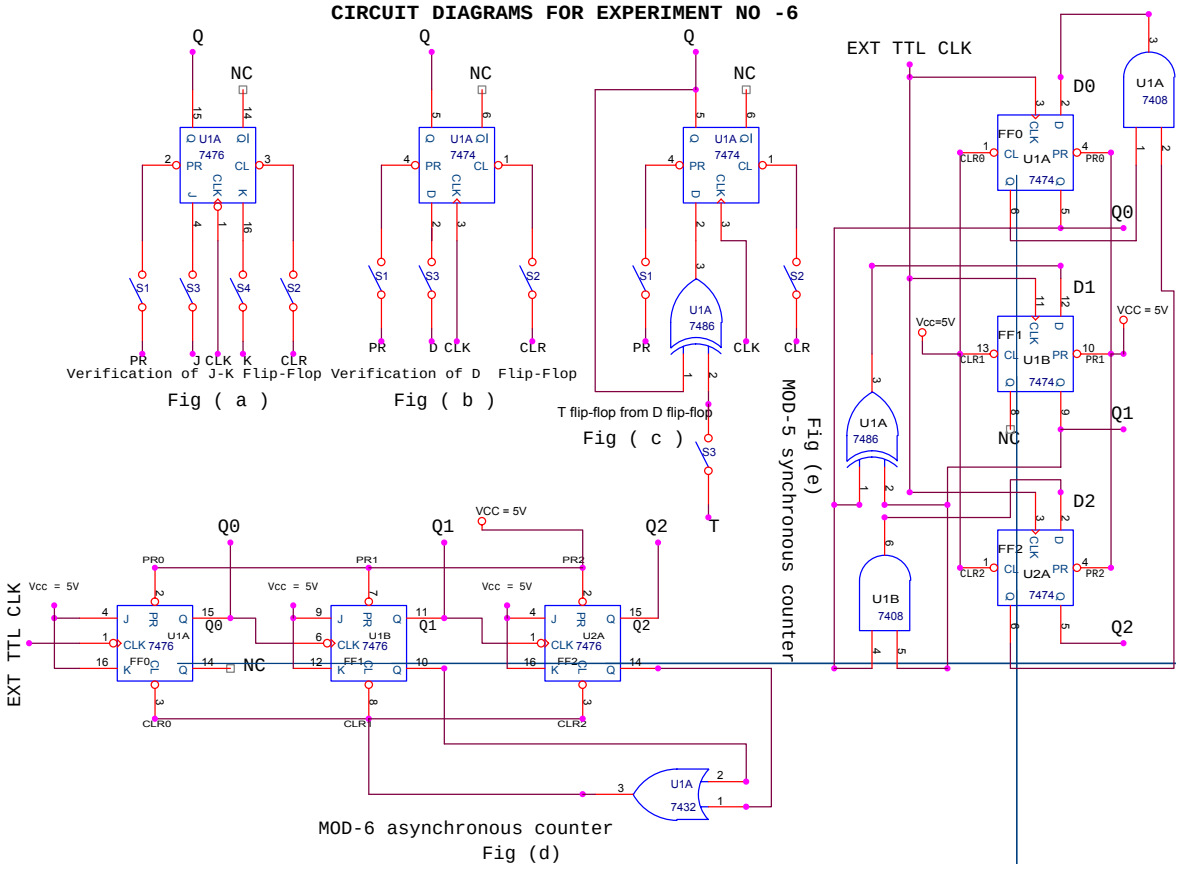
shown in Fig (d). Verify the following count sequence by observing the three output LED's: 0→1→2→3→4→5→0→1→2→3→4→5.

E. Design of Synchronous up counter using D flip-flops (IC 7474) having initial count 0 and modulus 5, without prevention of lockout condition: ***This counter design requires the following minimised expressions for the three D inputs of D flip-flop: $D_0 = \overline{Q_2} \cdot \overline{Q_0}$, $D_1 = Q_1 \oplus Q_0$ and $D_2 = Q_1 \cdot Q_0$. (Verify this by using the appropriate design procedure for synchronous counter design). To realise the above counter connect the circuit as shown in Fig (e). Connect all the preset and clear inputs of all D flip-flops (i.e. of 7474 IC) to logical 1. Connect pin no 14 and pin no 7 of 7474,7408 and 7486 IC's to V_{CC} = 5V and GND respectively. Connect the output Q_2 (MSB), Q_1 and Q_0 (LSB) of the counter to three LED's of CDS. Apply external clock from TTL clock output of CDS to the clock inputs of all the D flip-flop (i.e. IC 7474). Verify for the above counter the following count sequence by observing the output of three LED's: 0→1→2→3→4→0→1→2→3→4.***

F. Design theoretically a 3 bit Gray code synchronous counter of modulus 5 having the following sequence of states, using J-K flip-flop by preventing lockout***: 000→001→011→010→110→000→001→011→010→110. Show the complete circuit with proper connection with appropriate pins of the different IC's.***

G. Design theoretically an asynchronous counter having the following count sequence using J-K flip-flop by preventing lockout: ***2→3→4→5→6→7→2→3→4→5→6→7. Show the complete circuit with proper connection with appropriate pins of the different IC's.***

CIRCUIT DIAGRAMS FOR EXPERIMENT NO -6



EXPERIMENT NO: - 7

A. ***Study of asynchronous decade counter IC 7490:*** Connect the circuit as shown in Fig a (1) to Fig a (4) respectively to realise the following and verify the function table-1 of 7490 IC (a decade asynchronous counter) and also verify that the counter is negative edge triggered: For all the four circuits of Fig a (1) to Fig a (4) connect the four inputs MR1, MR2, MS1 and MS2 to four input switches. Connect pin no 5 and pin no 10 to V_{cc} = 5V and GND respectively for all the circuit of Fig a (1) to Fig a (4).

a) **Using circuit of Fig a (1) (Mode A connection) verify the MOD 10 or ÷ 10 decade counter sequence** by observing the four counter output connected to four LED's. For this apply TTL clock from CDS to the clock input CP_1 of the 7490 counter. Mod 10 sequence is: 0→1→2→3→4→5→6→7→8→9→0→1 and so on.

b) **Using circuit of Fig a (2) (Mode B connection) verify the MOD 10 or ÷ 10 symmetrical bi-quinary sequence** by observing the four counter output connected to four LED's. For this apply TTL clock from CDS to the clock input CP_2 of the 7490 counter. Mod 10 symmetrical bi-quinary sequence is: 0→2→4→6→8→1→3→5→7→9→0→2 and so on.

c) **Using circuit of Fig a (3) (Mode C connection) verify the MOD 2 or ÷ 2 sequence by observing the output of LED** connected with Q_0 output of the counter. For this apply TTL clock from CDS to the clock input CP_1 of the 7490 counter. Mod 2 sequence is 0→1→0 and so on.

d) **Using circuit of Fig a (4) (Mode D connection) verify the MOD 5 or ÷ 5 sequence by observing the output of LED** connected to Q_3, Q_2 and Q_1 outputs of the counter. For this apply TTL clock from CDS to the clock input CP_2 of the 7490 counter. Mod 5 sequence is 0→1→2→3→4→0→1 and so on.

B. ***Study of asynchronous binary counter or MOD 16 (÷16 counter) IC 7493:*** Connect the circuit as shown in Fig b (1) to Fig b (4) respectively to realise the following and verify the function table-2 of 7493 IC (a binary asynchronous counter) and also verify that the counter is negative edge triggered: For all the four circuits of Fig b (1) to Fig b (4) connect the two inputs MR1 and MR2 to two input switches. Connect pin no 5 and pin no 10 to V_{cc} = 5V and GND respectively for all the circuit of Fig b (1) to Fig b (4).

a) **Using circuit of Fig b (1) (Mode A connection) verify the MOD 16 or ÷ 16 binary counter sequence by observing the** four counter output connected to four LED's. For this apply TTL clock from CDS to the clock input CP_1 of the 7493 counter. Mod 16 sequence is: 0→1→2→3→4→5→6→7→8→9→10→11→12→13→14→15→0→1 and so on.

b) **Using circuit of Fig b (2) (Mode B connection) verify the MOD 16 or ÷ 16 symmetrical bi-octal sequence by observing the** four counter output connected to four LED's. For this apply TTL clock from CDS to the clock input CP_2 of the 7493 counter. Mod 16 symmetrical bi-octal sequence is: 0→2→4→6→8→10→12→14→1→3→5→7→9→11→13→15→0→2 and so on.

c) **Using circuit of Fig b (3) (Mode C connection) verify the MOD 2 or ÷ 2 sequence by observing the output of LED** connected with Q_0 output of the counter. For this apply TTL clock from CDS to the clock input CP_1 of the 7493 counter. Mod 2 sequence is 0→1→0 and so on.

d) **Using circuit of Fig b (4) (Mode D connection) verify the MOD 8 or ÷ 8 sequence by observing the output of LED** connected to Q_3, Q_2 and Q_1 outputs of the counter. For this apply TTL clock from CDS to the clock input CP_2 of the 7493 counter. Mod 8 sequence is 0→1→2→3→4→5→6→7→0→1 and so on.

Function Table – 1 of 7490 Counter

MR_1	MR_2	MS_1	MS_2	Q_3	Q_2	Q_1	Q_0
1	1	0	×	0	0	0	0
1	1	×	0	0	0	0	0
×	×	1	1	1	0	0	1
0	×	0	×	Count enable →Counter increment			
0	×	×	0	Count enable→Counter increment			
×	0	0	×	Count enable→Counter increment			
×	0	×	0	Count enable→Counter increment			

Function Table – 2 of 7493 Counter

MR_1	MR_2	Q_3	Q_2	Q_1	Q_0
1	1	0	0	0	0
0	×	Count enable ⇒Counter incre			
×	0	Count enable ⇒Counter incre			
0	0	Count enable ⇒Counter incre			

C. ***Study of synchronous decade counter IC 74160 to realise counter of various modulus:*** Connect the circuit as shown in Fig c (1) to Fig c (3). For all the three circuits connect P_3, P_2, P_1 and P_0 to four input switches and the four outputs Q_3, Q_2, Q_1 and Q_0 of the counter and TC output of the counter to five LED's of CDS. Connect pin no 16 and pin no 8 of all the 74160 IC used in Fig c (1) to Fig c (3) to V_{cc} = 5V and GND respectively. Apply TTL clock from CDS to the clock input pin no 2 of 74160 for all the three circuits. Verify the function table - 3 of 74160 synchronous counter by observing the four output LED's connected to the four outputs (Q_3, Q_2, Q_1 and Q_0) of the counter.

a) **To realise decade counter or ÷10 counter using 74160(using circuit of Fig c (1))** load 4 bit parallel data inputs as 0000. Verify that decade or ÷10 counter sequence is 0→1→2→3→4→5→6→7→8→9→0→1 and so on and also verify that this counter is positive edge triggered. Also note and observe the status of LED output connected to TC output of the counter for the above sequence.

b) **To realise Mod 6 counter or ÷6 counter using 74160(using circuit of Fig c (2))** load 4 bit parallel data inputs as 0100. Verify that decade or ÷10 counter sequence is 4→5→6→7→8→9→4→5 and so on and also verify that this counter is positive edge triggered. Also note and observe the status of LED output connected to TC output of the counter for the above sequence.

c) **To realise Mod 4 counter or ÷4 counter using 74160(using circuit of Fig c (3))** load 4 bit parallel data inputs as 0110. Verify that Mod 4 or ÷4 counter sequence is 6→7→8→9→6→7→8→9 and so on and also verify that this counter is positive edge triggered. Also note and observe the status of LED output connected to TC output of the counter for the above sequence.

D. ***Study of synchronous UP/DOWN decade counter 74192 IC:*** To realise UP or DOWN counter using 74192 (a decade UP/Down counter IC) connect the circuit as shown in Fig d (1) and Fig d (2) respectively. For all the two circuits, connect d/P_3, C/P_2, B/P_1 and A/P_0 to four input switches and the six outputs Q_3, Q_2, Q_1, Q_0, $\overline{C}O$ and $\overline{B}O$ of the counter is connected to six LED's of CDS. Connect pin no 16 and pin no 8 of all the 74192 IC used in Fig c (1) to Fig c (3) to V_{cc} = 5V and GND respectively.

a) **To realise UP count sequence by using 74192 counter IC** apply TTL clock from CDS to the UP clock input (pin no 5 of 74192) and connect DN clock input (pin no 4 of 74192) to logical 1 for the circuit of Fig d (1). Verify the function table - 4 of 74192 (an synchronous UP/DOWN counter) by observing the four output LED's connected to (Q_3, Q_2, Q_1 and Q_0) the four outputs of the counter. Verify the UP count sequence 0→1→2→3→4→5→6→7→8→9→0→1 and so on. Also verify that this counter is positive edge triggered. Note the status of LED's connected at $\overline{C}O$ and $\overline{B}O$ output during UP count sequence when the counter output switches from count 0 to count 9 and during down count sequence when the counter output switches from count 9 to count 0 respectively.

b) **To realise DOWN count sequence by using 74192 counter IC** apply TTL clock from CDS to the DOWN clock input (pin no 4 of 74192) and connect UP clock input (pin no 5 of 74192) to logical 1 for the circuit of Fig d (2). Verify the function table - 4 of 74192, an synchronous UP/DOWN counter by observing the four output LED's connected to (Q_3, Q_2, Q_1 and Q_0) the four outputs of the counter. Verify the DOWN count sequence 9→8→7→6→5→4→3→2→1→0→9→8 and so on. Also verify that this counter is positive edge triggered. Note the status of LED's connected at $\overline{C}O$ and $\overline{B}O$ output during

UP count sequence when the counter output switches from count 0 to count 9 and during down count sequence when the counter output switches from count 9 to count 0 respectively.

Function Table – 3 of 74160 (Synchronous decade counter)

$\overline{R}$	$\overline{PE}$	ENP	ENT	CLK	P_3	P_2	P1	P_0	Q_3	Q_2	Q_1 Q_0
0	×	×	×	×	×	×	×	×	0	0	0
0⇒ Asyn Reset/Clear.											
1	0	×	×	⌟	1	0	0	1	1	0	0
1⇒Syn. Parallel Load.											
1	1	1	1	⌟	×	×	×	×	Count enable/ Counter increment		
1	1	0	×	⌟	×	×	×	×	Counter Stops / Counter Hold		
1	1	×	0	⌟	×	×	×	×	Counter Stops / Counter Hold		

Function Table – 4 of 74192 (an UP/DOWN synchronous decade counter)

CLR	$\overline{LOAD}$	UP	DN	D/P_3	C/P_2	B/P_1	A/P_0	Q_3	Q_2	Q_1	Q_0
1	×	×	×	×	×	×	×	0	0	0	0⇒
0	0	×	×	1	0	0	0	1	0	0	1⇒
0	1	⌟	1	×	×	×	×	Counter increment⇒ Up count sequen			
0	1	1	⌟	×	×	×	×	Counter decrement⇒ Down count sequ			
0	1	0	×	×	×	×	×	Counter stop⇒ Counter Hold			
0	1	×	0	×	×	×	×	Counter stop⇒ Counter Hold			

E. ***How would you practically realise MOD-7 counter using 7490 IC (an asynchronous decade counter)?***

F. ***How would you practically realise MOD-13 counter using 7493 IC (an asynchronous MOD 16 or ÷16 binary counter)?***

G. ***How would you theoretically cascade several 74160 (a synchronous decade counter or Mod-10 counter IC) to realise a MOD 85 or ÷ 85 counter? Show the interconnections with proper pin diagram.***

H. ***How would you theoretically cascade several 74161 (a synchronous binary counter or Mod-16 counter IC) to realise a MOD 213 or ÷ 213 counter? Show the interconnections with proper pin diagram. (74160 IC and 74161 IC's are pin to pin compatible).***

I. ***How would you theoretically cascade two 7490 IC to realise ÷100 (Mod 100) counter.***

CIRCUIT DIAGRAMS FOR EXPERIMENT NO - 7

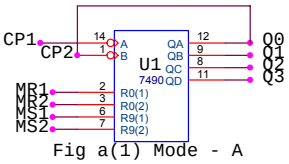


Fig a(1) Mode - A

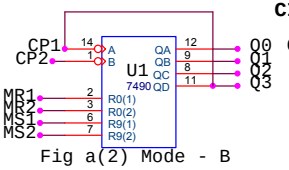


Fig a(2) Mode - B

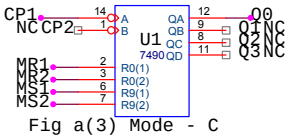


Fig a(3) Mode - C

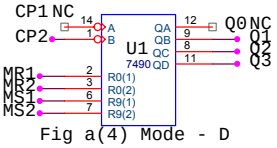


Fig a(4) Mode - D

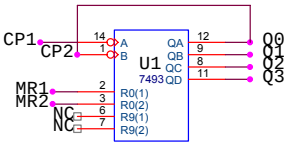


Fig b(1) Mode - A

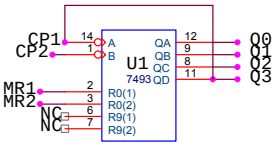


Fig b(2) Mode - B

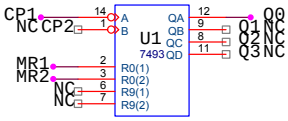


Fig b(3) Mode - C

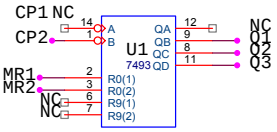


Fig b(4) Mode - D

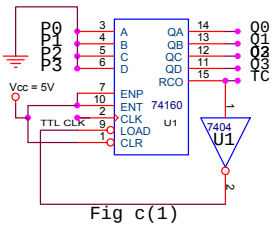


Fig c(1)

Mod-10(decade) counter by 74160

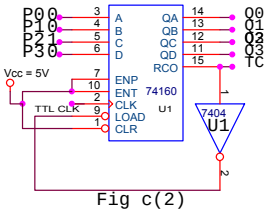


Fig c(2)

Mod-6 (decade) counter by 74160

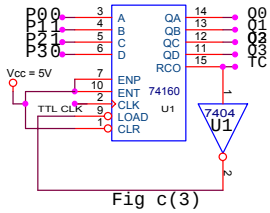


Fig c(3)

Mod-4 (decade) counter by 74160

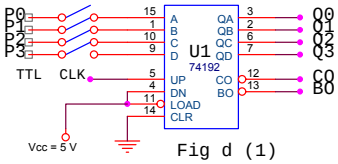


Fig d (1)

Circuit for up counter using 74192 IC

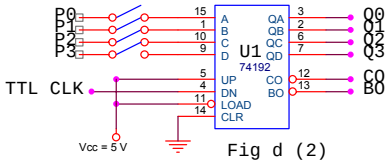


Fig d (2)

Circuit for down counter using 74192 IC

EXPERIMENT NO: - 8

A. ***Study of four bit one's complement binary Adder/Subtractor Circuit:*** Connect the circuit as shown in Fig (a). Connect A_4 (MSB), A_3, B_4 (MSB), B_3, M (the control input) through five input switches and connect the four outputs S_4, S_3, S_2, S_1 which represent 4 bit SUM or DIFFERENCE in 1's complement to the four output LED's of CDS. A_4 A_3 A_2 A_1 represent the four Augends or Minuend bits in 1's complement and B_4 B_3 B_2 B_1 represent the four Addend or Subtrahend bits in 1's complement. The inputs A_2, A_1, B_2, and B1 are left unconnected i.e. NC (means no connection which is equivalent to logical 1 input for TTL IC). Connect pin no 5 and pin no 12 for 7483 IC to V_{cc} = 5V and GND respectively. Connect also pin no 14 and pin no 7 of 7486 IC to V_{cc} = 5V and GND respectively. Show a table containing different values of control input M, 4 bit Augend / Minuend bits ($A_4A_3A_2A_1$), 4 bit Addend /Subtrahend bits ($B_4B_3B_2B_1$) and 4 bit Sum / Difference ($S_4S_3S_2S_1$) bits in 1's complement, operation performed, and remarks in different column. Indicate the operation performed for each input and check whether the results are OK (as required for 1's complement addition / subtraction operation) or not and check when overflow occurs.

B. ***Study of four bit two's complement binary Adder/Subtractor Circuit:*** Connect the circuit as shown in Fig (b). For this do not remove the circuit of Fig (a). From circuit of Fig a remove the short circuit between C_0 and C_4 and connect the control input M to C_0 input. Connect A_4 (MSB), A_3, B_4 (MSB), B_3, M (the control input) through five input switches and connect the four outputs S_4, S_3, S_3, S_0 which represent 4 bit SUM or DIFFERENCE in 2's complement to the four output LED's of CDS. A_4 A_3 A_2 A_1 represents the four Augend or Minuend bits in 2's complement and B_4 B_3 B_2 B_1 represent the four Addend or Subtrahend bits in 2's complement. The inputs A_2, A_1, B_2, and B1 are left unconnected i.e. NC (means no connection which is equivalent to logical 1 input for TTL IC). Connect pin no 5 and pin no 12 for 7483 IC to V_{cc} = 5V and GND respectively. Connect also pin no 14 and pin no 7 of 7486 IC to V_{cc} = 5V and GND respectively. Show a table containing different values of control input M, 4 bit Augend / Minuend bits ($A_4A_3A_2A_1$), 4 bit Addend / Subtrahend bits ($B_4B_3B_2B_1$) and 4 bit Sum / Difference ($S_4S_3S_2S_1$) bits in 2's complement, operation performed, and remarks in different column. Indicate the operation performed for each input and check whether the results are OK (as required for 2's complement addition / subtraction operation) or not and check when overflow occurs.

C. ***Study of four bit digital magnitude comparator IC 7485:***

a) ***Use of 7485 IC (a 4 bit digital magnitude comparator) as a 4-bit magnitude comparator.*** For this connect the circuit as shown in Fig c (1). Connect A_3, B_3 and A>B, A<B, A=B (the three cascading inputs) inputs of 7485 through five input switches and connect the three outputs OA>B, Oa<B and OA=B to three output LED's of CDS. Connect pin no 16 and pin no 8 to V_{cc} = 5 V and GND respectively. Connect A_2, A_1, A_0 and B_2, B_1, B_0 to logical 1 or left it unconnected. By varying the five inputs verify the function table – 1 for the 7485 IC and also verify how this 7485 IC can be used as a 4-bit magnitude comparator.

b) ***Use of 7485 IC (a 4 bit digital magnitude comparator) as a 5-bit magnitude comparator:*** For this connect the circuit as shown in Fig c (2). Connect A_4, B_4, A_0, B_0 inputs of 7485 through four input switches and connect the three outputs OA>B, Oa<B and OA=B to three output LED's of CDS. Connect pin no 16 and pin no 8 to V_{cc} = 5 V and GND respectively for 7485 IC and Connect pin no 14 and pin no 7 to V_{cc} = 5 V and GND respectively for the IC 7486 and 7404. By varying the inputs (5 bits of $A_4A_3A_2A_1A_0$ and $B_4B_3B_2B_1B_0$ of which A_4, B_4,

A_0 and B_0 can be varied by varying these four switch position) verify how this 7485 IC can be used as a 5-bit digital magnitude comparator.

D. ***Study of 74180 IC (a 8 bit parity Generator/Checker IC):***

a) ***Use of 74180(a 8 bit parity Generator/Checker IC 74180) as an 8 bit EVEN or ODD parity checker circuit***. For this connect the circuit as shown in Fig d (1). Connect the three inputs F, G, H and two cascading inputs EI and OI through five input switches. Connect the other five inputs A, B, C, D, E to logical 1 (means no connection are made to these 5 inputs). Connect the two outputs EO (Even output) and OO (Odd output) to two output LED's of CDS. Connect pin no 14 and pin no 7 to V_{cc} = 5V and GND respectively for 74180IC. By varying the inputs verify the function table – 2 of 74180 IC.

b) ***Use of 74180(a 8 bit parity Generator/Checker IC 74180) as a 9 bit EVEN or ODD parity checker circuit.*** For this connect the circuit as shown in Fig d (2). The ninth input **(I)** for the 9 bit even parity checker circuit is connected to OI input, thus the nine inputs to the 74180 IC are A, B, C, D, E, F, G, H and I. Connect the five inputs E, F, G, H and I through five input switches. Connect the other four inputs A, B, C and D to logical 1 (means no connections are made to these 4 inputs). Connect the two outputs EO (Even output) and OO (Odd output) to two output LED's of CDS. Connect pin no 14 and pin no 7 to V_{cc} = 5V and GND respectively for 74180 and 7404 IC. By varying 9 (nine) input verify that LED connected to EO output of 74180 IC glows only when the 9 input bits have Even parity and LED connected to OO output of 74180 IC glows only when the 9 input bits have Odd parity. Verify that only one out of two output LED's will glow at a time and when LED at EO glows ⇒ Even parity (for 9 inputs) and when LED at OO glows ⇒ODD parity (for 9 inputs).

c) ***Use of 74180 (a 8 bit parity Generator/Checker IC 74180) as a 10-bit EVEN parity generator circuit.*** For this

Connect the circuit as shown in Fig d (3) The ninth input **(I)** for the 9 bit even parity generator circuit is connected to EI cascading input (as shown in Fig d (3), thus the nine inputs to the 74180 IC are A, B, C, D, E, F, G, H and I. Connect the five inputs E, F, G, H and I through five input switches. Connect the other four inputs A, B, C and D to logical 1 (means no connection are made to these 4 inputs). Connect the output EPGO (the 10 th Even parity generated bit) to one output LED's of CDS. Connect pin no 14 and pin no 7 to V_{cc} = 5V and GND respectively for 74180 and 7404 IC. By varying 9 inputs (of which five inputs at E, F, G, H and I can be varied as they are connected to five input switches) verify that LED connected to EPGO output of 74180 IC glows only when the 9 input bits have odd parity and LED connected to EPGO output of 74180 IC will not glow when the 9 input bits have even parity. This verification ensures that the circuit function as a 10-bit EVEN parity generator.

E. ***How would you theoretically cascade two 7485 IC (a 4 bit digital magnitude comparator) to realise 8 bit digital magnitude comparator? Show the circuit diagram using appropriate pin connections.***

F. ***How would you theoretically use a single 74180 IC to realise 5 bit EVEN / ODD parity checker circuit? Show the circuit diagram using appropriate pin connections.***

G. ***How would you theoretically use a single 74180 IC to realise 10 bits ODD parity generator circuit? Show the circuit diagram using appropriate pin connections.***

J. ***How would you theoretically cascade two 74180 to realise 16 bit EVEN / ODD parity checker circuit using 74180 IC? Show the circuit diagram with appropriate pin connections.***

Function Table – 1 of 7485 IC.

Comparing inputs	Cascading Inputs			Outputs		
	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
A>B	×	×	×	1	0	0
A<B	×	×	×	0	1	0
A=B	0	0	0	1	1	0
A=B	0	0	1	0	0	1
A=B	0	1	0	0	1	0
A=B	0	1	1	0	0	1
A=B	1	0	0	1	0	0
A=B	1	0	1	0	0	1
A=B	1	1	0	0	0	0
A=B	1	1	1	0	0	1

Function Table – 2 of 74180 IC

INPUTS			OUTPUTS	
Parity of inputs A through H (the 8 inputs)	EI/EVEN	OI/ODD	EO / ∑EVEN	OO / ∑ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
×	1	1	0	0
×	0	0	1	1

Note: Connect the three cascading inputs A>B, A<B, A=B and the other two inputs A_3, and B_3 to five input switches from extreme left position. (A>B input switch should be on extreme left and B_0 input switch should be on extreme right. Connect the three outputs $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ to three output LED's of CDS from extreme left to right position i.e. $O_{A>B}$ output LED should be at extreme left and $O_{A=B}$ output LED should be at extreme right position. Any unconnected input or NC at any pin is equivalent to logical 1 input for all TTL IC's. NC ⇒ no Connection.

CIRCUIT DIAGRAMS FOR EXPERIMENT NO -8

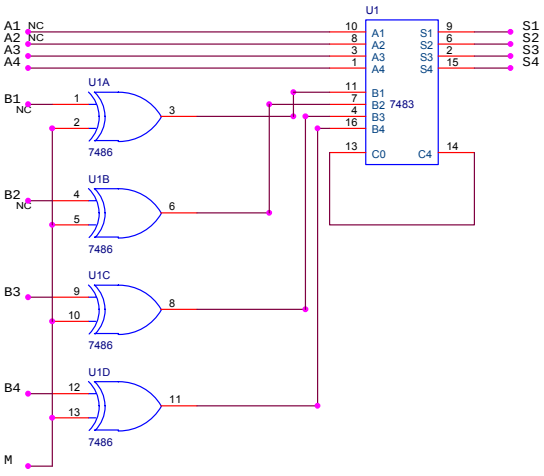


Fig (a) 4 bit 1's Complement Adder/Subtractor circuit

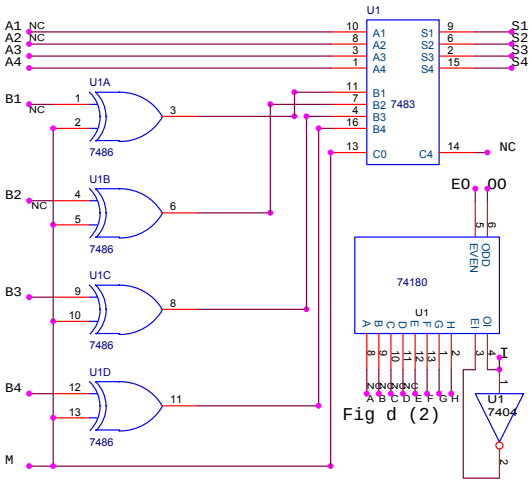


Fig d (2)

Fig (b) 4 bit 2's Complement Adder/Subtractor circuit

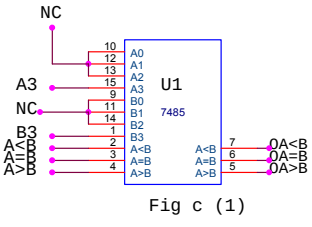


Fig c (1)

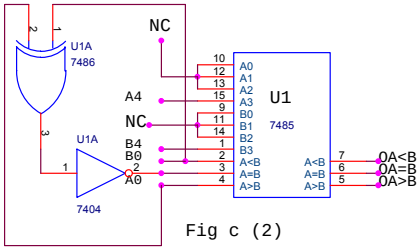


Fig c (2)

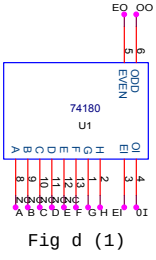


Fig d (1)

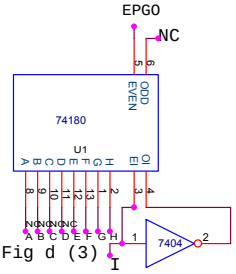


Fig d (3)

EXPERIMENT NO: - 9

A. ***Study of 64-bit Read/Write memory using 74189 IC:*** The 74189 IC is a high speed 64-bit RAM organized as a 16- word by 4- bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is high. The outputs are active only in the Read mode and the output data is the complement of the stored data. For this connect the circuit as shown in Fig (a). Connect $\overline{WE}$, A_0, A_1, A_2 and A_3 to five input switches (where S_5 as MSB and S_1 as LSB switch). Connect the four outputs $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$ and $\overline{O}_4$ to four output LED's of the CDS. Connect the data inputs to $D_4 = 0$, $D_3 = 1$, $D_2 = 1$ and $D_0 = 0$ permanently. Connect pin no 16 and pin no 8 to $V_{cc} = 5V$ and GND respectively for 74189 IC. Connect $\overline{CS}$ input (pin no 2) to GND. Now by varying the combination of five input switches verify the following function Table-1 by observing the status of four output LED's connected at four outputs $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$ and $\overline{O}_4$ respectively. To verify the volatile nature of this memory device first switch off the power to the CDS for some time and again switch on the power to the CDS. Now observe or read the contents of any previous memory location, changes in the contents of any previous memory location proves the volatile nature of this memory device.

Function Table - 1

$\overline{CS}$	$\overline{WE}$	A_3	A_2	A_1	A_0	D_4	D_3	D_2	D_1	$\overline{Q}_4$	$\overline{Q}_3$	$\overline{Q}_2$	$\overline{Q}_1$	Operating Mode
0	0	0	0	0	0	0	1	1	0	NG	NG	NG	NG	⇒ Writing onto memory location 0000. (output inactive)
0	1	0	0	0	0	0	1	1	0	1	0	0	1	⇒Reading from memory location 0000. (output active)
0	0	1	1	1	1	0	1	1	0	NG	NG	NG	NG	⇒ Writing onto memory location 1111. (output inactive)
0	1	1	1	1	1	0	1	1	0	1	0	0	1	⇒Reading from memory location 1111. (output active)
1	×	×	×	×	×	×	×	×	×	NG	NG	NG	NG	⇒ Output tristated i.e. High impedance (Reading / Writing both disabled)

B. ***Study of Schmitt trigger inverter using 7414 IC (a hex Schmitt trigger inverter IC):***

a) **For Schmitt trigger as inverter connect the circuit as shown in Fig b (1).** Connect input (pin no 1) to one input switch and connect the output (pin no 2) to one LED of the CDS. Connect pin no 14 and pin no 7 to $V_{cc} = 5V$ and GND respectively for 7414 IC. Now verify the truth table of NOT gate (or inverter gate) by varying the input switch position and observing the corresponding output LED status.

b) **Study of Schmitt trigger characteristics:** For this connect the circuit as shown in Fig b (2). Connect the input (pin no 1) to a source of input voltage through a 25 K potentiometer and the output (pin no 2) to one output point of the CDS. Now measure the input voltages at pin no 1 (or at the variable point of the potentiometer) and also measure the corresponding output voltages at the output points (to which pin no 2 is connected) by using a digital voltmeter first by varying the input voltage gradually between 0V to 5V and then vary the input voltage between 5V to 0V. Now make a table showing the different input voltages and the corresponding output voltages in two different columns. From this table of data plot the Schmitt trigger characteristics by plotting V_{in} along the X- axis and V_{out} along Y-axis. From this characteristics find the V_{UT} and V_{LT} the upper trip and lower trip point and hence determine the hysterisis voltage is given by: $V_H = V_{UT} - V_{LT}$.

c) **Converting a Sine wave into Square wave by using Schmitt trigger inverter IC 7414:** For this connect the circuit as shown in Fig b (3). Apply the Sine wave from the point marked High on the CDS to pin no 1 and connect the output pin no 2 to one Y input of a CRO. Connect pin no 14 and pin no 7 to Vcc = 5V and GND respectively. If double beam CRO is available then connect the input and output points of 7414 IC to the Y1 and Y2 channel inputs of the double beam CRO. Observe the output waveform on the CRO which will be a square wave, this may require little adjustment of the amplitude of the Sine wave and adjustment of the CRO time base and voltage/ division switch. Observe also the input waveform on the CRO. By observing the input and output on a dual beam CRO it is clear that the input and output frequencies are equal.

C. ***Study of 555 Timer IC:***

a) **Study of 555 Timer IC in astable mode:** For this connect the circuit as shown in Fig c (1). Use $R_A = R_B = 10K\Omega$. Use a dual beam CRO to connect the output pin no 6 and pin no 3 to two different channels of a dual beam CRO. Now at pin no 6 observe the continuous charging and discharging waveform and at pin no 3 observe the unsymmetrical square wave or astable waveform. From this observation verify that when capacitor is charging output at pin 3 is high and when capacitor is discharging the output at pin no 3 is low. By observing the output waveform on a CRO at pin no 3 find the duty cycle and frequency of the unsymmetrical square wave by measuring the T_{ON} and T_{OFF}. Also find the duty cycle and frequency of the unsymmetrical waveform from analytical expressions for the On and Off period of the square wave which are given by: $T_{On} = 0.693(R_A + R_B)\ C$ and $T_{Off} = 0.693R_BC$ respectively. Comment on the difference in the measured values of the duty cycle and frequency of the square wave by the above two methods. How would you modify the circuit of Fig c (1) to get symmetrical square wave at the output pin 3.

b) **Study of 555 Timer IC in monostable mode:** For this connect the circuit as shown in Fig c (2). Use $R = 100K\Omega$ and $C = 100\mu f$. Now connect the TRG (the trigger input) input to one input switch of the CDS. Connect the output (pin no 3) to one LED of the CDS. Now observe that when the trigger input at pin no 2 is high the output LED will not glow which implies that the output remains at low stable state. When the trigger input at pin no 2 is switched from HIGH → LOW → HIGH state the output LED at pin no 3 glows for some time and again becomes off after some specific time until the next negative going trigger comes. The duration over which LED connected at pin no 3 remains glowing is the duration of the quasistable state. Note the duration in seconds of the quasistable state by using your wrist watch. Also observe that how the duration of this quasi stable state can be changed by varying the time constant (RC) of the monostable circuit i.e. either by varying the value of R or C. This verify the function of 555 Timer IC as a monostable multivibrator.

D. ***Study of 4- bit Universal Shift Register IC 74194:***

a) **To verify all basic operations of shift register using 4 –bit Universal shift register IC 74194** connect the circuit as shown in fig d (1). Connect inputs $\overline{CLR}$, S_1, S_0, S_L and S_R to five input switches. Connect four outputs Q_A(LSB output), Q_B, Q_C and Q_D(MSB output) to four output LED's of the CDS. Connect the four parallel inputs A=1(A=LSB), B=0, C=1 and D=1(D=MSB). Connect pin no 16 and pin no 8 to $V_{cc} = 5V$ and GND respectively for all the circuit of Fig d (1) to Fig d (3). Apply clock input to pin no 11 of 74194 from the TTL clock output of CDS. Now varying the five input switch position and observing the status of four output LED's verify the function table- 2 for 74194 IC.

Function Table – 2

$\overline{CLR}$	S_1	S_0	S_L	S_R	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Mode of operation
0	×	×	×	×	×	×	×	×	0	0	0	0	⇒ Master Reset.
1	1	1	×	×	1	0	1	1	1	0	1	1	⇒ Parallel Load.
1	0	1	×	0	×	×	×	×	0	Q_A	Q_B	Q_C	⇒ Right shift operation.
1	0	1	×	1	×	×	×	×	1	0	Q_A	Q_B	⇒ Right shift operation.
1	1	0	0	×	×	×	×	×	Q_B	Q_C	Q_D	0	⇒ Left shift operation.
1	1	0	1	×	×	×	×	×	Q_B	Q_C	0	1	⇒ Left shift operation.
1	0	0	×	×	×	×	×	×	Output at previous state.				⇒ Output Hold i.e. No change.

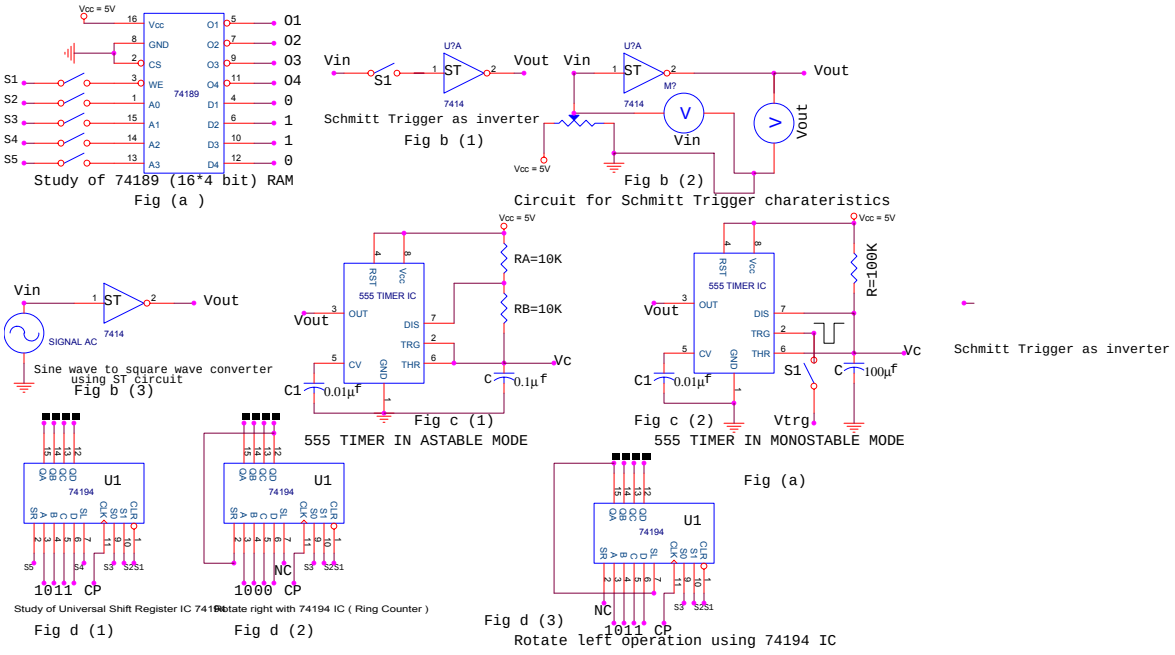
b) **To use 74194 for rotate right operation or to realise 4 bit Ring counter:** For this connect the circuit as shown in Fig d (2). Load initially the four output Q_A (LSB), Q_B, Q_C and Q_D (MSB) as 1000 by

applying A = 1, B = 0, C = 0 and D = 0 at the four parallel inputs of the shift register and use $\overline{CLR} = 1$, $S_1 = 0$ and $S_0 = 1$ for right shift operation and apply the clock from TTL clock output of CDS to the clock input (pin no 11) of 74194 IC. Observing the change in the four output LED's connected to Q_A (LSB), Q_B, Q_C and Q_D (MSB) verify the rotate right operation (from Q_A towards Q_D) or ring counter sequence with the arrival of each clock pulse.

c) **To use 74194 for rotate left operation:** For this connect the circuit as shown in Fig d (3). Load initially the four output Q_A (LSB), Q_B, Q_C and Q_D (MSB) as 1000 by applying A = 1, B = 0, C = 0 and D = 0 at the four parallel inputs of the shift register and use $\overline{CLR} = 1$, $S_1 = 1$ and $S_0 = 0$ for left shift operation and apply the clock from TTL clock output of CDS to the clock input (pin no 11) of 74194 IC. Observing the change in the four output LED's connected to Q_A(LSB), Q_B, Q_C and Q_D(MSB) verify the rotate left operation (from Q_D towards Q_A) with the arrival of each clock pulse.

Note: For experiment with 74194 it is better to use the slower TTL clock pulse (of frequency 0.1 Hz) of the CDS. NG ⇒ LED not glow. CDS ⇒ Component Development System.

CIRCUIT DIAGRAMS FOR EXPERIMENT NO - 9



EXPERIMENT NO: -10

A. ***Study of 4-bit Arithmetic and Logic Unit (Using 74181 IC):*** To realise different logical and arithmetic operations using 74181 IC, (a 4 - bit ALU chip) connect the circuit as shown in Fig (a). Apply the 4 bit number A = $(3)_{10}$ (i.e. connect $A_3 = A_2 = 0$(logical 0) and $A_1 = A_0 = 1$(logical 1 or NC)). Apply the 4 bit number B = $(4)_{10}$ (i.e. connect $B_3 = B_1 = B_0 = 0$(logical 0) and $B_2 = 1$(logical 1 or NC)). Connect the input carry CN0 = 1 or 0 (for testing arithmetic operations). Connect the four select inputs S_3, S_2, S_1, S_0 and M (the mode control input) to five input switches as shown in fig (a). Connect the four function outputs F_3, F_2, F_1, F_0 and the carry output C_{N+4} to five output LED's of the CDS. Now keeping M=1, varying the select inputs verify the different logical operations as given in function table – 1. Note that the output LED connected to C_{N+4} output remains always glowing for all possible values of the select inputs as logical operations between A and B does not produce any carry. Now by making M = 0, and connecting C_N = 1 or 0 verify the different arithmetic operations for different possible values of the select inputs according to the function table – 1. Note the changes in the carry output LED status (connected at C_{N+4} output) for different arithmetic operation with and without carry. Connect pin no 24 and pin no 12 to V_{cc} = 5V and GND respectively.

Function Table – 1 for 74181 ALU chip.

Select inputs				M=1 **(Logical operations)**	**M=0 and C_N = 1 (Arithmetic operations)**		**M = 0 and C_N = 0 (Arithmetic operations)**	
				Function output	**Function output**	C_{N+4}	**Function Output**	C_{N+4}
0	**0**	**0**	**0**	$\overline{A}$	**A**		**A Plus 1**	
0	**0**	**0**	**1**	$\overline{(A+B)}$	**A+B**		**(A + B) Plus 1**	
0	**0**	**1**	**0**	$\overline{A}\cdot B$	**A+** $\overline{B}$		**(A +** $\overline{B}$ **) Plus 1**	
0	**0**	**1**	**1**	**0**	**Minus 1(2's Compl)**		**Zero**	
0	**1**	**0**	**0**	$\overline{A\cdot B}$	**A Plus A·** $\overline{B}$		**A Plus A·** $\overline{B}$ **Plus 1**	
0	**1**	**0**	**1**	$\overline{B}$	**(A+B) Plus A·** $\overline{B}$		**(A+B) Plus A·** $\overline{B}$ **Plus 1**	
0	**1**	**1**	**0**	**A⊕B**	**A Minus B Minus 1**		**A Minus B**	
0	**1**	**1**	**1**	**A** $\overline{B}$	**A·** $\overline{B}$ **Minus 1**		**A·** $\overline{B}$	
1	**0**	**0**	**0**	$\overline{A}$**+B**	**A Plus A·B**		**A Plus A·B Plus 1**	
1	**0**	**0**	**1**	$\overline{A\oplus B}$	**A Plus B**		**A Plus B Plus 1**	
1	**0**	**1**	**0**	**B**	**(A+** $\overline{B}$**) Plus A·B**		**(A+** $\overline{B}$**) Plus A·B Plus 1**	
1	**0**	**1**	**1**	**A·B**	**A·B Minus 1**		**A·B**	
1	**1**	**0**	**0**	**1**	**A Plus A**		**A Plus A Plus 1**	
1	**1**	**0**	**1**	**A+** $\overline{B}$	**(A + B) Plus A**		**(A+B) Plus A Plus 1**	
1	**1**	**1**	**0**	**A+B**	**(A +** $\overline{B}$ **) Plus A**		**(A+** $\overline{B}$**) Plus A Plus 1**	
1	**1**	**1**	**1**	A	**A Minus 1**		***A***	

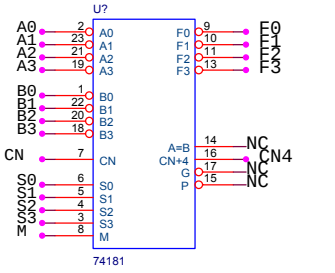
Note: Plus ⇒ Arithmetic addition. Minus ⇒ Arithmetic subtraction.

B. ***Study of 8-bit Microprocessor compatible D/A converter using DAC0800/MC1408 IC in unipolar mode:*** To study the characteristics of 8-bit DAC using DAC0800/MC1408 IC in unipolar mode, connect the circuit as shown in Fig (b). Connect the three MSB inputs D_7, D_6, and D_5 to GND (i.e. pin no 5,6 and 7 are connected to GND) and the remaining five inputs D_4, D_3, D_2, D_1 and D_0 (i.e. pin no 8,9,10,11 and 12) are connected through five input switches. The circuit of Fig (b) gives the unipolar configuration of the D/A converter IC. ***Short circuit the GND point of ± 15V power supply with the GND point of 5V power supply to have a common ground.*** Now by varying the five digital inputs by varying the five

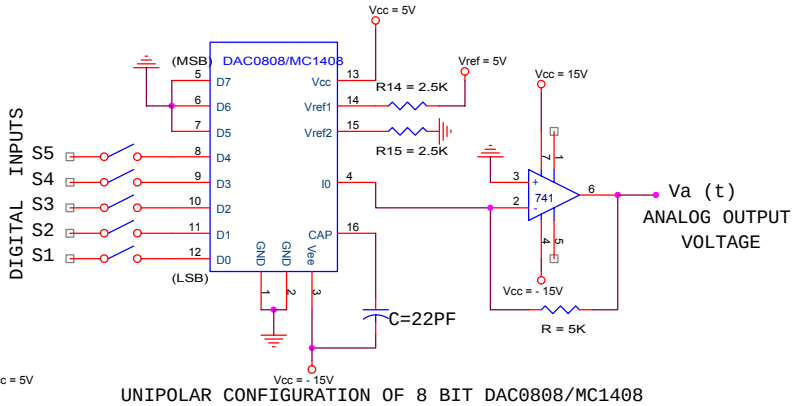
switch position measure the corresponding analog output voltage for each digital input by using a digital voltmeter connected between pin no 6 (the output of op-amp) and the GND. Now by connecting the three MSB inputs to logical 1 voltage (i.e. connecting D_7, D_6, and D_5 to logical 1 voltage) and all five input switch connected to logical 1 position measure the maximum analog output voltage of the DAC0808 between pin no 6 (the output of op-amp) and the GND. Analog voltage $V_a(t)$ so obtained will vary from 0V to 10V i.e. $0V \leq V_a(t) \leq 10V$(in unipolar mode. Now plot a curve between the digital inputs (plotted along x-axis) and the corresponding analog output voltages (plotted along y-axis) to get the D/A converter characteristics for unipolar DAC.

C. ***Study of 8-bit Microprocessor compatible D/A converter using DAC0800/MC1408 IC in bipolar mode:*** To study the characteristics of 8-bit DAC using DAC0800/MC1408 IC in bipolar mode, connect the circuit as shown in Fig (c). By varying the digital inputs in the same manner as above note the corresponding analog output voltage $V_a(t)$ by using a digital voltmeter connected between the output pin 6 of 741 op-amp and the GND. Verify that the analog output voltage for bipolar mode varies between –5V to 5V i.e. $-5V \leq V_a(t) \leq 5V$. Now plot a curve between the digital inputs (plotted along x-axis) and the corresponding analog output voltages (plotted along y-axis) to get the D/A converter characteristics for bipolar DAC.

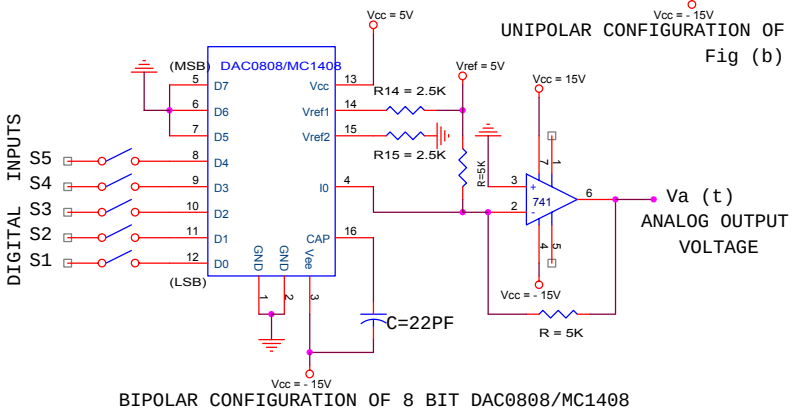
CIRCUIT DIGRAMS FOR EXPERIMENT NO - 10



STUDY OF 4 BIT ALU USING 74181IC
Fig (a)



UNIPOLAR CONFIGURATION OF 8 BIT DAC0808/MC1408
Fig (b)



BIPOLAR CONFIGURATION OF 8 BIT DAC0808/MC1408
Fig (c)