Design of synchronous counters.

- **Step 1. Number of flip-flops:**
  Based on the description of the problem, determine the required number n of the FFs - the smallest value of n is such that the number of states $N \leq 2^n$ and the desired counting sequence.
- **Step 2. State diagram:**
  Draw the state diagram showing all the possible states.
- **Step 3. Choice of flip-flops and excitation table:**
  Select the type of flip-flops to be used and write the excitation table.
  An excitation table is a table that lists the present state (PS), the next state (NS) and the required excitations.
- **Step 4. Minimal expressions for excitations:**
  Obtain the minimal expressions for the excitations of the FFs using K-maps for the excitations of the flip-flops in terms of the present states and inputs.
- **Step 5. Logic Diagram:**
  Draw the logic diagram based on the minimal expressions.
- **Excitation Tables**

PS	NS	Required inputs	
Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

S-R FF

PS	NS	Required inputs	
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

J-K FF

PS	NS	Required inputs
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

D FF

PS	NS	Required inputs
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

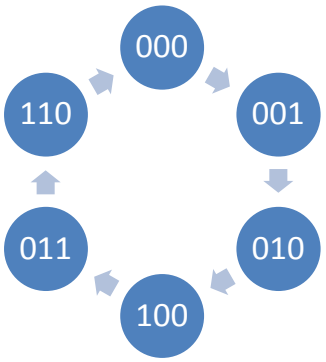
T FF

Design a counter to generate the repetitive sequence 0,1,2,4,3,6.

Step 1. Number of flip-flops:

A counter with repetitive sequence 0, 1, 2, 4, 3, 6 requires 3 flip-flops. The counting sequence is 000, 001, 010, 100, 011, 110, 000 …

Step 2. Draw the state diagram:



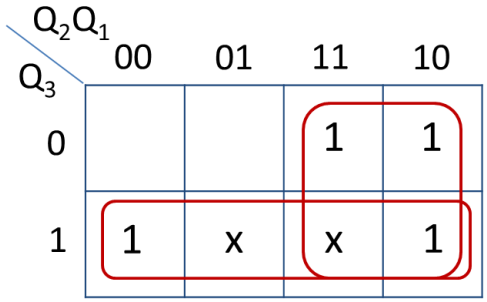
Step 3. Select the type of flip-flops and draw the excitation table:

T flip-flops are selected and the excitation table of a given sequence counter using T flip-flops is shown below.

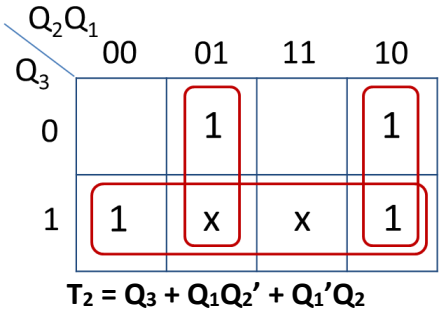
PS			NS			Required excitations		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	1	0	0	1	1	0
1	0	0	0	1	1	1	1	1
0	1	1	1	1	0	1	0	1
1	1	0	0	0	0	1	1	0

Step 4. Obtain the minimal expressions

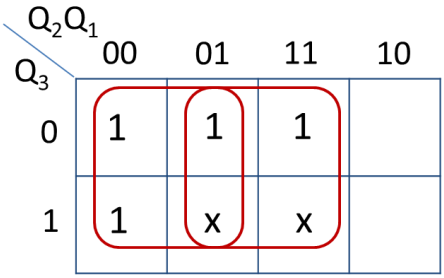
K – Maps for excitations T_3, T_2, and T_1 and their minimized form are as follows:



$T_3 = Q_3 + Q_2$

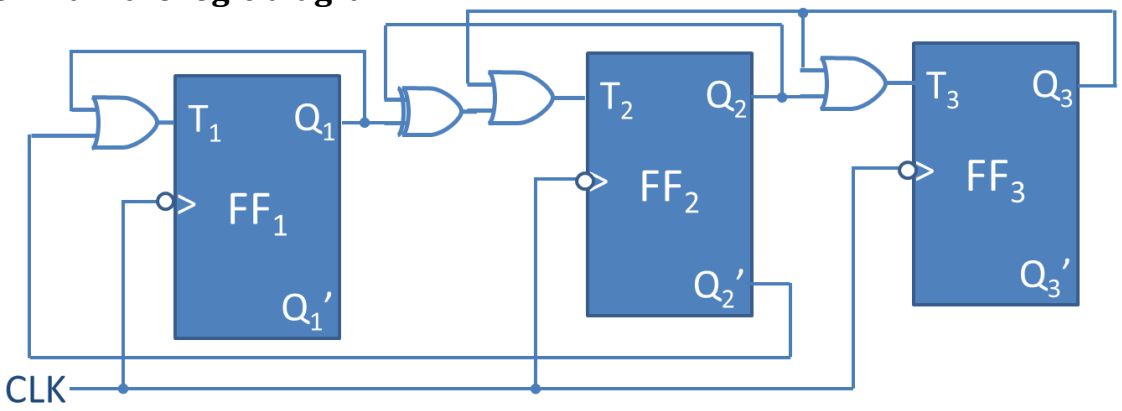


$T_2 = Q_3 + Q_1Q_2' + Q_1'Q_2$



$T_1 = Q_2' + Q_1$

Step 5. Draw the logic diagram

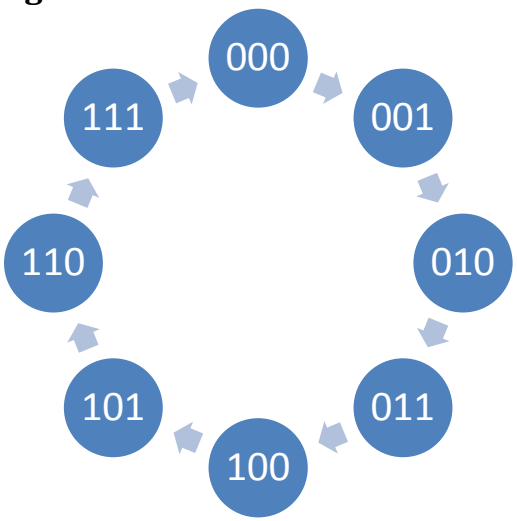


Design 3-bit synchronous up counter using T flip flop.

Step 1. Number of flip-flops:

A 3 bit up counter requires 3 flip-flops. The counting sequence is 000, 001, 010, 011, 100, 101, 110, 111, 000 …

Step 2. Draw the state diagram:



Step 3. Select the type of flip-flops and draw the excitation table:

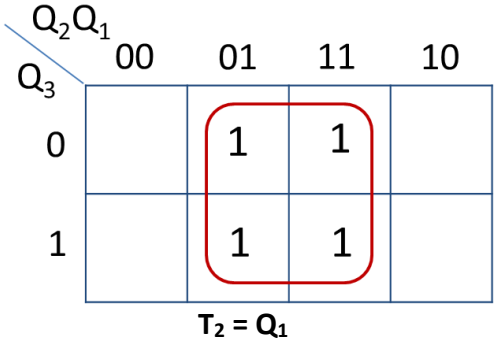
T flip-flops are selected and the excitation table of a given sequence counter using T flip-flops is shown below.

PS			NS			Required excitations		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

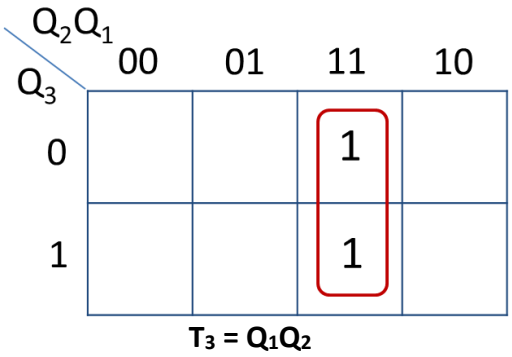
Step 4. Obtain the minimal expressions

From excitation table, $T_1 = 1$.

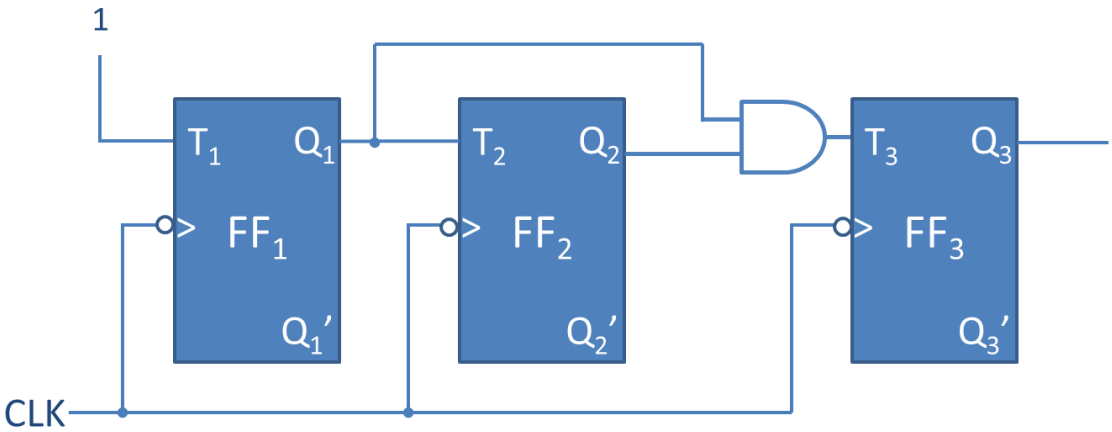
K – Maps for excitations T_3 and T_2 and their minimized form are as follows:



$T_2 = Q_1$



Step 5. Draw the logic diagram

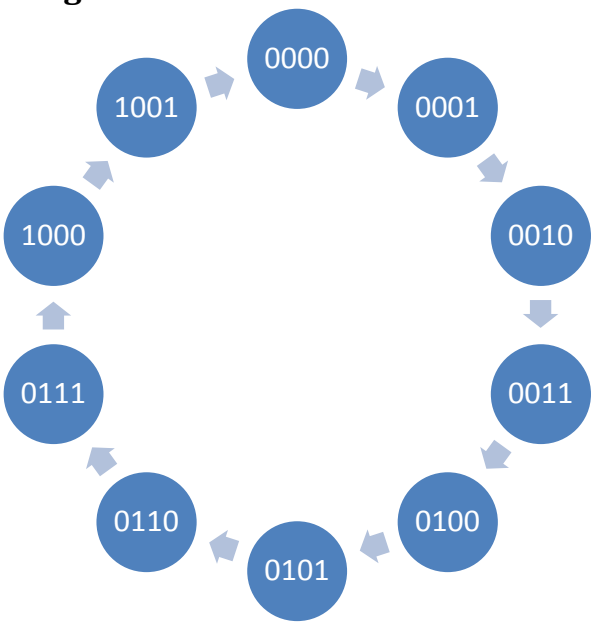


Design a synchronous BCD counter with JK flip-flops.

Step 1. Number of flip-flops:

A BCD counter requires 4 flip-flops. The counting sequence is 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 0000 …

Step 2. Draw the state diagram:



Step 3. Select the type of flip-flops and draw the excitation table:

J-K flip-flops are selected and the excitation table of a given sequence counter using J-K flip-flops is shown below.

PS				NS				Required excitations							
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	J_4	K_4	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	x
0	0	0	1	0	0	1	0	0	x	0	x	1	X	x	1
0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	x
0	0	1	1	0	1	0	0	0	x	1	x	x	1	x	1
0	1	0	0	0	1	0	1	0	x	x	0	0	X	1	x
0	1	0	1	0	1	1	0	0	x	x	0	1	X	x	1
0	1	1	0	0	1	1	1	0	x	x	0	x	0	1	x
0	1	1	1	1	0	0	0	1	x	x	1	x	1	x	1
1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	x
1	0	0	1	0	0	0	0	x	1	0	x	0	x	x	1

Step 4. Obtain the minimal expressions

From excitation table, it is clear that $J_1 = K_1 = 1$

K – Maps for excitations J_4, K_4, J_3, K_3, J_2, K_2, J_1 and K_1 and their minimized form are as follows:

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00				
01			1	
11	x	x	x	x
10	x	x	x	x

$J_4 = Q_3Q_2Q_1$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	x	x	x	x
10		1	x	x

$K_4 = Q_1$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00			1	
01	x	x	x	x
11	x	x	x	x
10			x	x

$J_3 = Q_1Q_2$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	x	x	x	x
01			1	
11	x	x	x	x
10	x	x	x	x

$K_3 = Q_1Q_2$

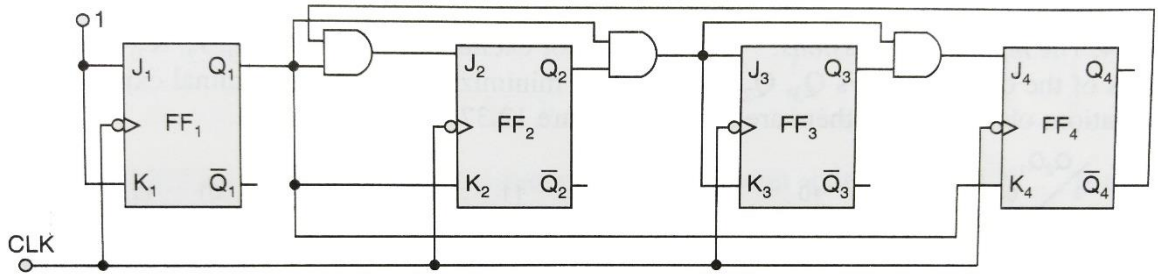
Q_4Q_3 \ Q_2Q_1	00	01	11	10
00		1	x	x
01		1	x	x
11	x	x	x	x
10			x	x

$J_2 = Q_1Q_4'$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	x	x	1	
01	x	x	1	
11	x	x	x	x
10	x	x	x	x

$K_2 = Q_1$

Step 5. Draw the logic diagram

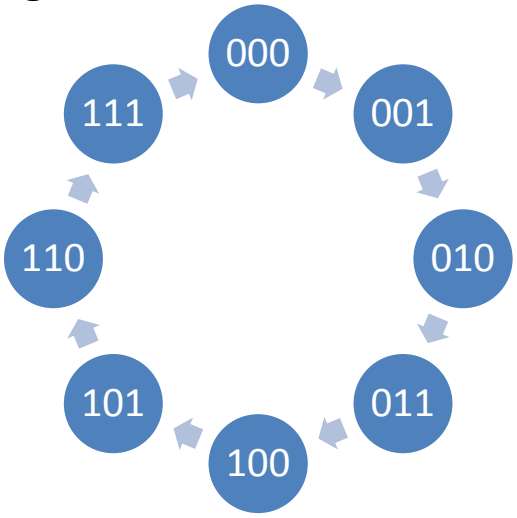


Design a 3-bit synchronous up counter using K-maps and positive edge-triggered JK FFs.

Step 1. Number of flip-flops:

A 3 bit up counter requires 3 flip-flops. The counting sequence is 000, 001, 010, 011, 100, 101, 110, 111, 000 …

Step 2. Draw the state diagram:



Step 3. Select the type of flip-flops and draw the excitation table:

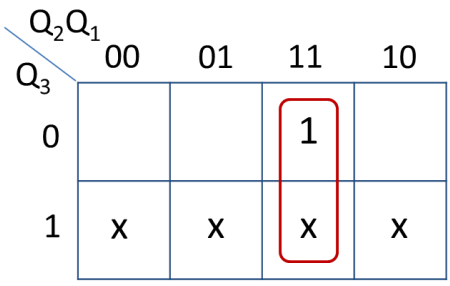
J-K flip-flops are selected and the excitation table of a given sequence counter using J-K flip-flops is shown below.

PS			NS			Required excitations					
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	X	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

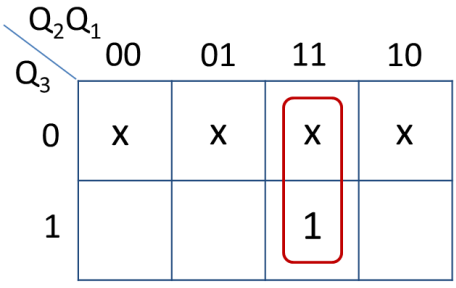
Step 4. Obtain the minimal expressions

From excitation table, $J_1 = K_1 = 1$.

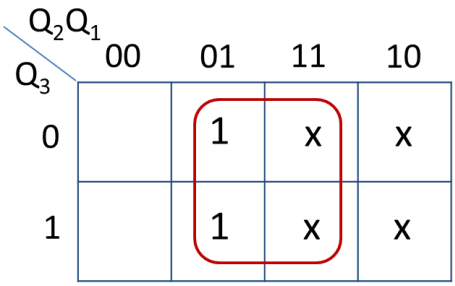
K – Maps for excitations J_3, K_3, J_2 and K_2 and their minimized form are as follows:



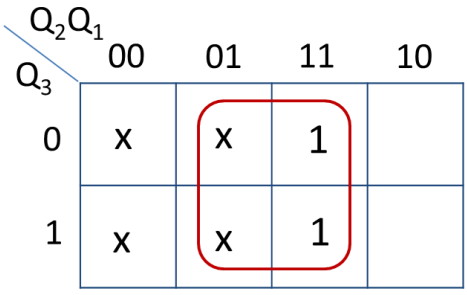
$J_3 = Q_2Q_1$



$K_3 = Q_2Q_1$

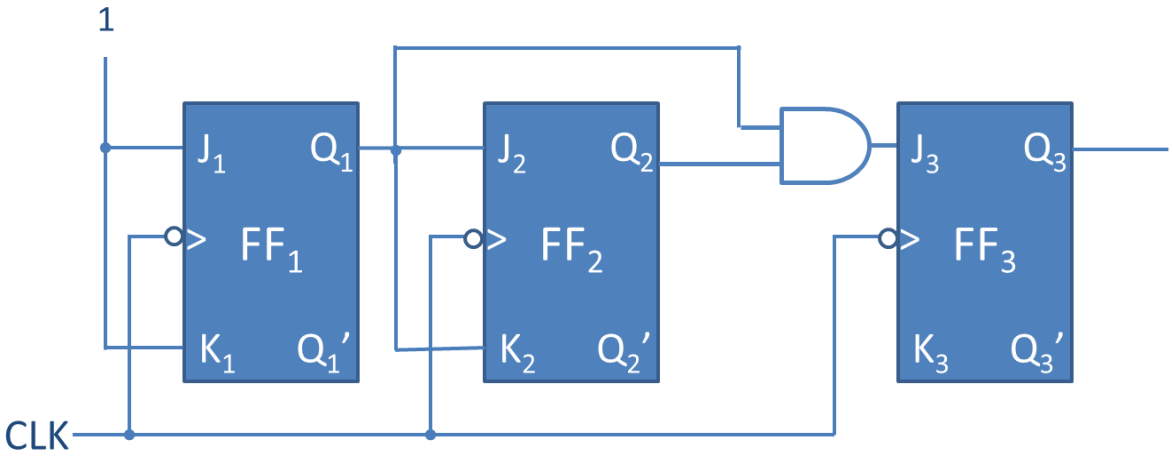


$J_2 = Q_1$



$K_2 = Q_1$

Step 5. Draw the logic diagram

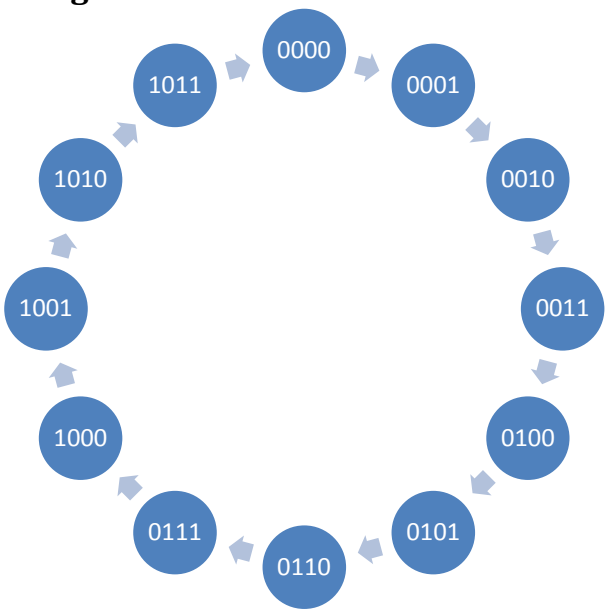


Design a mod-12 Synchronous up counter using D-flipflop.

Step 1. Number of flip-flops:

A mod-12 counter requires 4 flip-flops. The counting sequence is 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 0000 …

Step 2. Draw the state diagram:



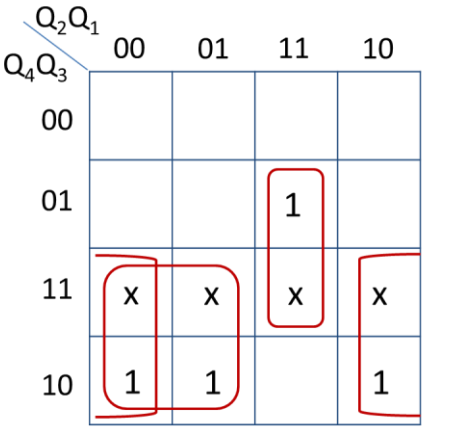
Step 3. Select the type of flip-flops and draw the excitation table:

D flip-flops are selected and the excitation table of a given sequence counter using D flip-flops is shown below.

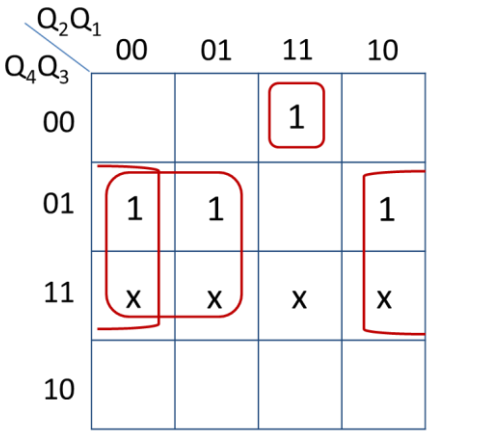
PS				NS				Required excitations			
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	D_4	D_3	D_2	D_1
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	0	0	0	0	0	0	0	0

Step 4. Obtain the minimal expressions

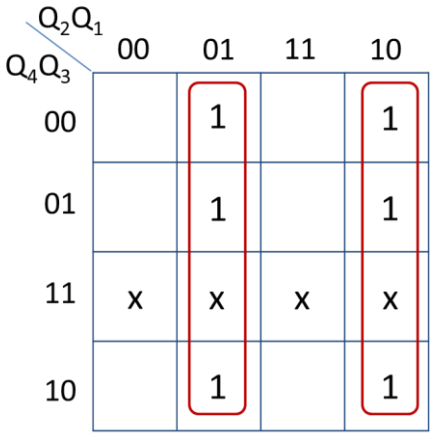
K – Maps for excitations D_4, D_3, D_2, and D_1 and their minimized form are as follows:



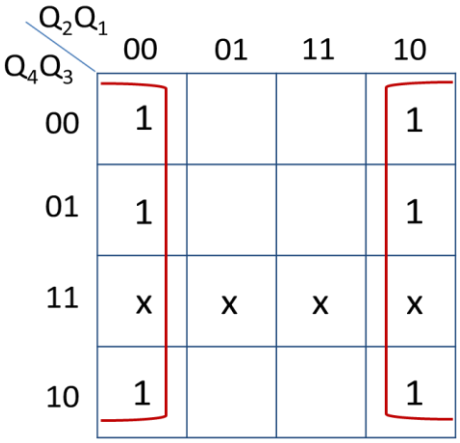
$$D_4 = Q_2'Q_4 + Q_1'Q_4 + Q_1Q_2Q_3$$



$$D_3 = Q_2'Q_3 + Q_1'Q_3 + Q_1Q_2Q_3'Q_4'$$



$$D_2 = Q_2'Q_1 + Q_2Q_1'$$



$$D_1 = Q_1'$$

Step 5. Draw the logic diagram