

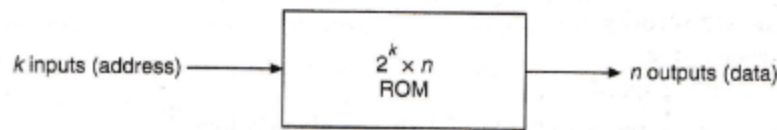
Introduction to Programmable Logic Devices

- A programmable logic device is an IC that is user configurable and is capable of implementing logic functions.
- It is an LSI chip that contains a 'regular' structure and allows the designer to customize it for any specific application, i.e. it is programmed by the user to perform a function required for his application.
- A PLD contains a large number of gates, flip-flops, and registers that are interconnected on the chip. Many of the connections, however, are fusible links that can be broken.
- The IC is said to be programmable because the specific function of the IC for a given application is determined by the selective breaking of some of the interconnections while leaving others intact.
- The 'fuse blowing' process can be done either by the manufacturer in accordance with the customer's instructions, or by the customer himself which is called 'programming' because it produces the desired circuit pattern interconnecting the gates, flip-flops, registers, and so on.
- PLDs can be reprogrammed in a few seconds and hence give more flexibility to experiment with designs.
- The advantages of PLDs over fixed function ICs are as follows:
 1. Low development cost
 2. Less space requirement
 3. Less power requirement
 4. High reliability
 5. Easy circuit testing
 6. Easy design modification
 7. High design security
 8. Less design time
 9. High switching speed

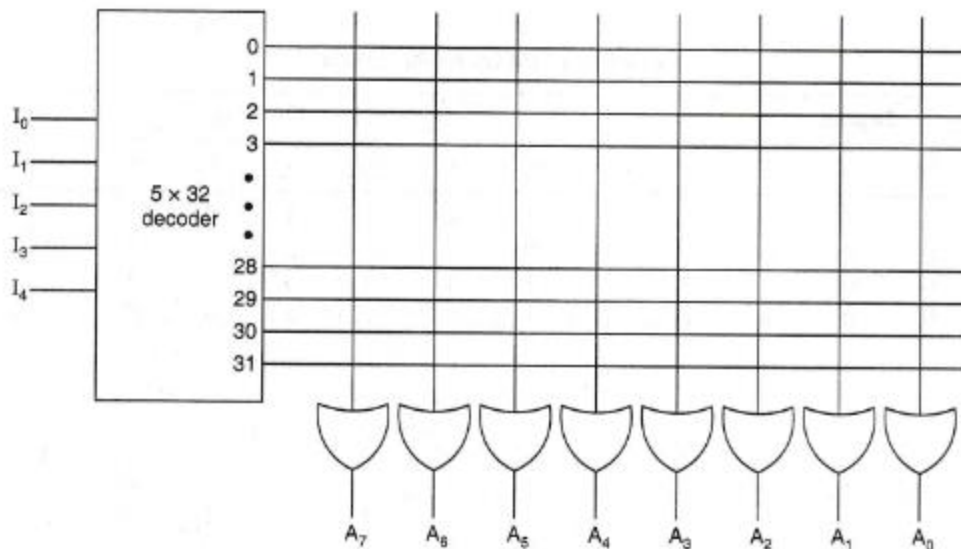
Read Only Memory (ROM)

- A read-only memory (ROM) is essentially a memory device in which permanent binary information is stored.
- Once the pattern is established, it stays within the unit when the power is turned off and on again.
- ROMs are used to store information which is of fixed type, such as tables for various functions, fixed data and instructions.
- The advantages of using a ROM as a PLD are the following:
 1. Ease of design since no simplification or minimization of logic function is required.
 2. Designs can be changed, modified rapidly.
 3. It is usually faster than discrete MSI/SSI circuit.
 4. Cost is reduced.
- There are a few disadvantages also of ROM based circuits, such as:
 1. Non-utilization of complete circuit
 2. Increased power requirement
 3. Enormous increase in size with increase in the number of input variables making it impractical

ROM Organization



- A block diagram of a ROM is shown in the figure. It consists of k inputs and n outputs.
- The inputs provide the address for the memory and the outputs give the data bits of the stored word which is selected by the address.
- The number of words in a ROM is determined from the fact that k address input lines are needed to specify 2^k words.
- Consider, for example, a 32×8 ROM. The unit consists of 32 words of 8 bits each.



- There are five input lines that form the binary numbers from 0 through 31 for the address.
- The five inputs are decoded into 32 distinct outputs by means of a 5×32 decoder.
- ROM is basically a decoder with k inputs and 2^k output lines followed by a bank of OR gates.
- Each output of the decoder represents a memory address.
- The 32 outputs of the decoder are connected to each of the 8 OR gates.
- Each OR gate must be considered as having 32 inputs.
- Since each OR gate has 32 input connections and there are 8 OR gates, the ROM contains $32 \times 8 = 256$ internal connections.
- In general, a $2^k \times n$ ROM will have an internal $k \times 2^k$ decoder and n OR gates.
- Each OR gate has 2^k inputs, which are connected to each of the outputs of the decoder.

Types of ROM

Maskable programmable read-only memory (MROM)

In this type of read-only memory, the user specifies the data to be stored to the manufacturer of the memory. The data pattern specified by the user are programmed as a part of the fabrication process. Once programmed, the data pattern can never be changed. This type of read-only memory is referred to as ROM. ROMs are highly suited for very high volume usage due to their low cost.

Programmable read-only memory (PROM)

This type of memory comes from the manufacturer without any data stored in it, i.e. empty. The data pattern is programmed electrically by the user using a special circuit known as PROM programmer. It can be programmed only once during its life time. Once programmed, the data cannot be altered. This type of memory is known as PROM. These are highly suited for high volume usage due to their low cost of production.

Erasable programmable read-only memory (EPROM)

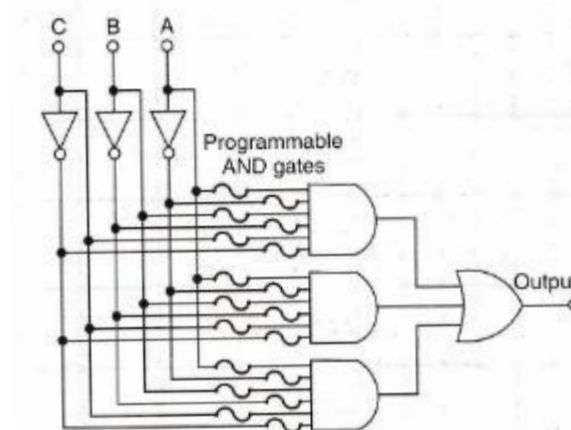
In this type of memory, data can be written any number of times, i.e. they are reprogrammable. Before it is reprogrammed, the contents already stored are erased by exposing the chip to ultraviolet radiation for about 30 minutes. This type of memory is referred to as EPROM. EPROMs are possible only in MOS technology. Programming is done using a PROM programmer.

Electrically erasable and programmable read-only memory (EEPROM or E2PROM)

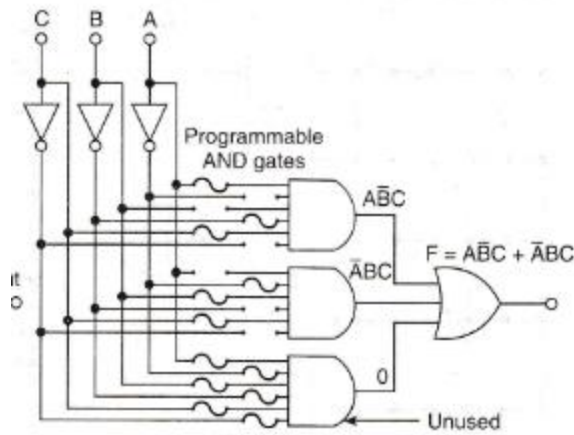
This is another type of reprogrammable memory in which erasing is done electrically rather than exposing the chip to the ultraviolet radiation. It is referred to as EEPROM or electrically alterable ROM (EAROM).

PROGRAMMABLE ARRAY LOGIC (PAL)

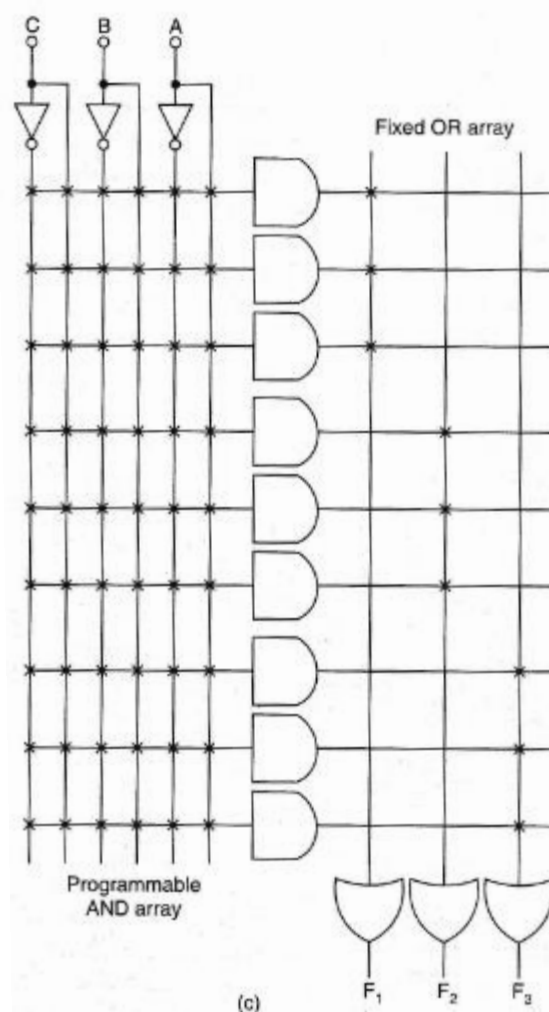
- Programmable array logic (a registered trade mark of Monolithic Memories) is a particular family of programmable logic devices (PLDs) that is widely used and available from a number of manufacturers.
- The PAL circuits consist of a set of AND gates whose inputs can be programmed and whose outputs are connected to an OR gate, i.e. the inputs to the OR gate are hard-wired, i.e. PAL is a PLD with a fixed OR array and a programmable AND array.



- Figure shows a small example of the basic structure. The fuse symbols represent fusible links that can be burned open using equipment similar to a PROM programmer.



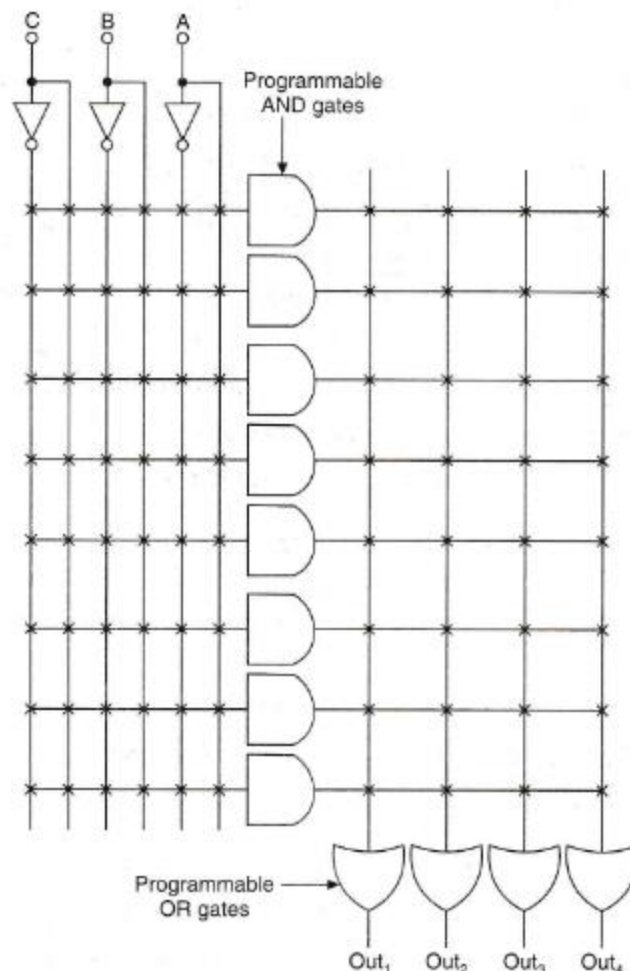
- Figure shows how the circuit is programmed to implement $F = A'BC + AB'C$.
- All input variables and their complements are left connected to the unused AND gate, whose output is, therefore, $AA'BB'CC' = 0$. The 0 has no effect on the output of the OR gate.
- The actual PAL circuits have several groups of AND gates, each group providing inputs to separate OR gates.



- Figure shows an example of how the PAL structure is represented using the abbreviated connections. It is a 3-input 3-wide AND-OR structure.
- Each function can have three minterms or product terms.
- Inputs to the OR gates at the outputs are fixed as shown by 'x' marked on the vertical lines.
- The inputs to the AND gates are marked on the corresponding line by the 'x'.
- Removing the 'x' implies blowing off the corresponding fuse which in turn implies that the corresponding input variable is not applied to the particular AND gate.

Programmable Logic Array (PLA)

- The PLA combines the characteristics of the PROM and the PAL by providing both a programmable OR array and a programmable AND array, i.e. in a PLA both AND gates and OR gates have fuses at the inputs.
- A third set of fuses in the output inverters allows the output function to be inverted if required. Usually X-OR gates are used for controlled inversion.
- However, it has some disadvantages. Because it has two sets of fuses, it is more difficult to manufacture, program and test it than a PROM or a PAL.



- Figure demonstrates the structure of a three-input, four-output PLA with every fusible link intact.
- Like ROM, PLA can be mask programmable or field programmable.

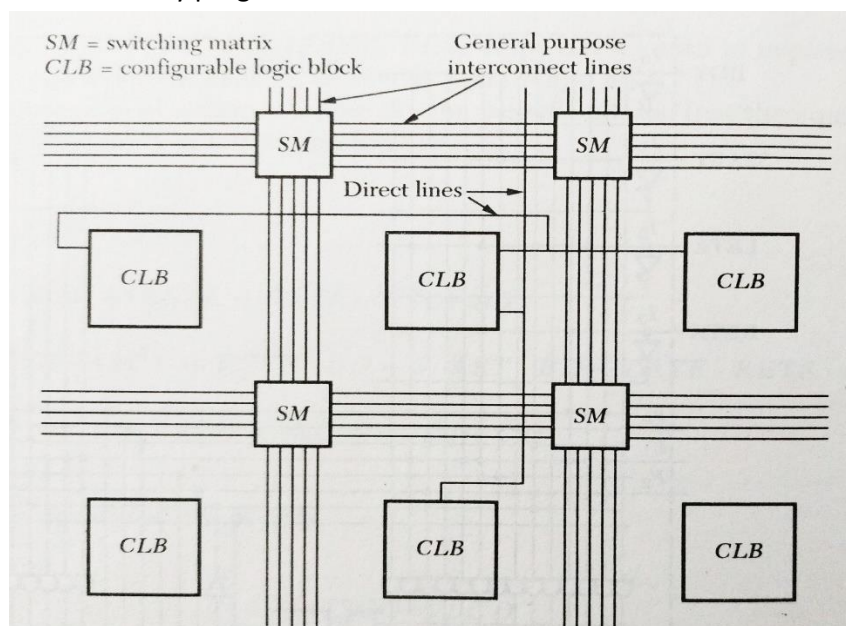
- With a mask programmable PLA, the user must submit a PLA programming table to the manufacturer.
- This table is used by the vendor to produce a user made PLA that has the required internal paths between inputs and outputs.
- A second type of PLA available is called a field programmable logic array or FPLA.
- The FPLA can be programmed by the user by means of certain recommended procedures. FPLAs can be programmed with commercially available programmer units.

Compare ROM, PAL and PLA

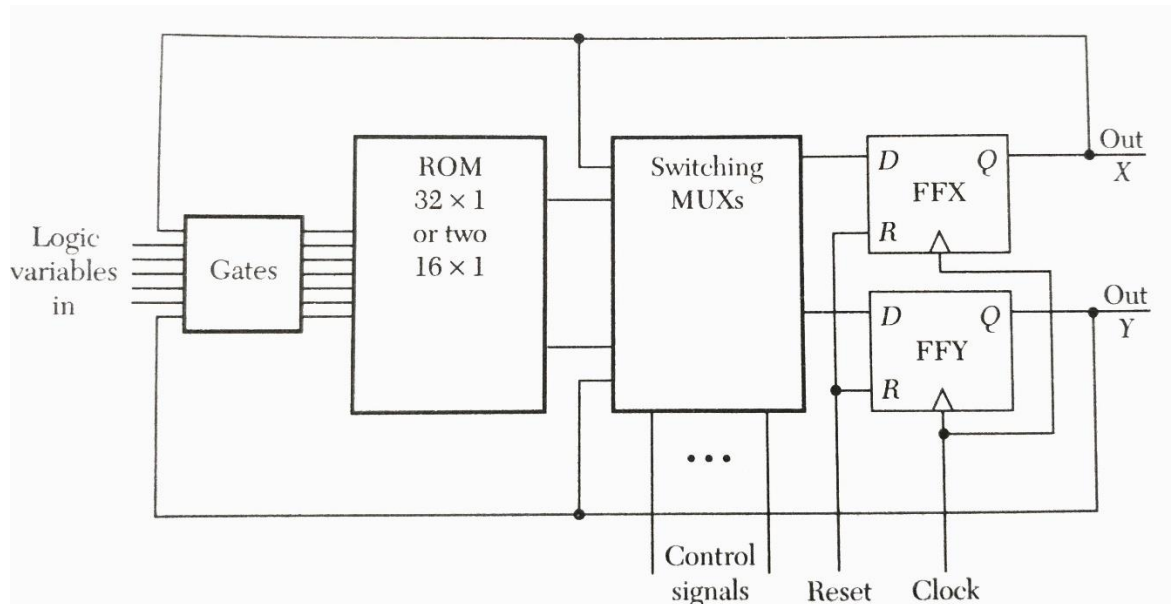
ROM	PAL	PLA
Consist of fixed AND gate array and programmable OR array.	Consist of programmable AND gate array and programmable OR array.	Consist of programmable AND gate array and programmable OR array.
Medium speed	High speed	Slow
Cheap	Intermediate cost	Most expensive
Not flexible	Not flexible	Offering maximum programming flexibility
It is possible to decode any minterms	We can get any desired minterms by programming the AND matrix	We can get any desired minterms by programming the AND & OR matrix
SOP function in the standard form only can be implemented	Any SOP function can be implemented	Any SOP function can be implemented

Xilinx FPGA

- The basic architecture is shown in figure. The logic modules have inputs and outputs that can be connected to metal lines by programmable switches.



- The direct lines allow signals to be sent to or received from adjacent logic modules.
- These direct lines can also be programmed to connect to the general purpose interconnect lines to allow interconnection of nonadjacent logic modules if required.
- In addition, signals can be switched from one path to another at the intersections of rows and columns of the general purpose interconnect lines.
- A simplified diagram of the configurable logic block or CLB is shown in figure.



- This block is similar to a two flip-flop, RAM -controlled state machine.
- The combinational logic is performed by a RAM that can be used as a 32 x 1 or two 16 x 1 RAMs.