Characteristics of Digital IC

Threshold Voltage
The threshold voltage is defined as that voltage at the input of a gate which causes a change in the state of the output from one logic level to the other.

Propagation Delay
A pulse through a gate takes a certain amount of time to propagate from input to output. This interval of time is known as the propagation delay of the gate.

Power dissipation
The power dissipation of a logic gate is the power required by the gate to operate with 50% duty cycle at a specified frequency and is expressed in mill watts.

Fan-in
The fan-in of a logic gate is defined as the number of inputs that the gate is designed to handle.

Fan-out
The fan-out (loading factor) of a logic gate is defined as the maximum number of standard loads that the output of the gate can drive without impairing its normal operation.

Noise Margin
When the digital circuits operate in noisy environment the gates may malfunction if the noise is beyond certain limits. The noise immunity of a logic circuit refers to the circuit's ability to tolerate noise voltages at its input. A quantitative measure of noise immunity is called noise margin.

Operating temperatures
The IC gates and other circuits are temperature sensitive being semiconductor devices. However they are designed to operate satisfactorily over a specified range of temperatures. The range specified for commercial applications is 0 to 70°C, for industrial it is 0 to 85°C and for military applications it is -55°C to 125°C.

Speed Power Product
A common means for measuring and comparing the overall performance of an IC family is the speed power product which is obtained by multiplying the gate propagation delay by the gate power dissipation. The smaller the product, the better the overall performance.

Transistor-Transistor Logic (TTL)

- The TTL is so named because of its independence on transistors alone to perform basic logic operations.
- The TTL uses transistors operating in saturated mode.
- It is the fastest of saturated logic families.
- The basic TTL logic circuit is the NAND gate.
- Good speed, low manufacturing cost, wide range of circuits and the availability in SSI and MSI are its advantages.
- Tight V_{CC} tolerance, relatively high power consumption, moderate packing density, generation of noise spikes and susceptibility to power transients are its disadvantages.
- TTL logic family consists of several subfamilies such as:

  - Standard TTL
  - High Speed TTL
  - Low Power TTL
  - Schottky TTL
  - Low Power Schottky TTL
  - Advanced Schottky TTL
  - Advanced Low Power Schottky TTL
  - F (Fast) TTL
- For standard TTL,
  - Propagation Delay time = 9 ns
  - Power dissipation per = 10 mW
  - Noise Margin = 0.4 mV
  - Fan-in = 8
  - Fan-out = 10
  - Logic '0' = 0 V to 0.8 V
  - Logic '1' = 2 V to 5 V
  - Indeterminate Range = 0.8 V to 2 V

Emitter-Coupled Logic (ECL)

- This logic family is also called Current Mode Logic or Current Steering Logic.
- It is the fastest of all logic families.
- ECL operates on the principle of current switching, whereby a fixed bias current less than IC switched from one transistor's collector to another.
- Because of this mode operation, this logic form is also referred to as Current Mode Logic (CML).
- It is also called Current Steering Logic (CSL), because current is steered from one device to another.
- The ECL family is used in very high frequency applications where its speed is superior.
- The important characteristics of ECL are:
  - Transistors never saturate. So, speed is high
  - Logic Levels are negative, -0.9 V for Logic 1 and -1.7 V for Logic 0.
  - Noise Margin is less, about 250 mV. This makes ECL, unreliable for use in heavy industrial environment.
  - ECL circuits produce the output and its complement, and therefore, eliminate the need for inverters.
  - Fan-out is large because the output impedance is low. It is about 25.
  - Power dissipation per gate is large.
  - The total current flow in ECL is more or less constant. So, no noise spikes will be internally generated.

MOSFET

- MOSFET family are simpler & inexpensive to fabricate, require much less power, have better noise margin, a greater supply voltage range, a higher fan-out and require much less chip area as compared to other bipolar logic families.
- For MOS logic,
  - Propagation Delay, t_{pd} = 50 ns.
  - Noise Margin, NM = 1.5 V.

- Power Dissipation, PD = 0.1 Mw.
- Fan out = 50 for frequencies greater than 100 Hz and it is virtually unlimited for dc or low frequencies.
- The propagation delay associated with MOS gates is large (50 ns) because of their high output resistance (100 k) and capacitive loading presented by the driven gates.

- There are three types of MOSFET:
  - P-channel MOSFET (PMOS)
    - Enhancement Type PMOS
    - Depletion Type PMOS
  - N-channel MOSFET (NMOS)
    - Enhancement Type NMOS
    - Depletion Type NMOS
  - Complementary MOSFET (CMOS)

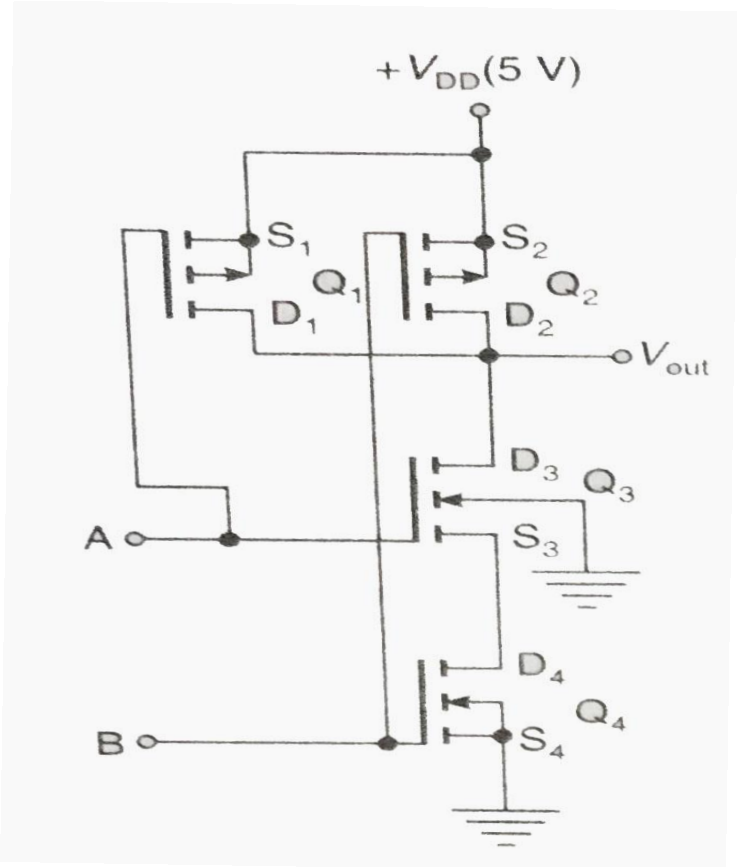
Compare TTL, ECL, & CMOS logic families.

Characteristic	TTL	CMSO	ECL
Power Input	Moderate	Low	Moderate-High
Frequency limit	High	Moderate	Very high
Circuit density	Moderate-high	High-very high	Moderate
Circuit types per family	High	High	Moderate

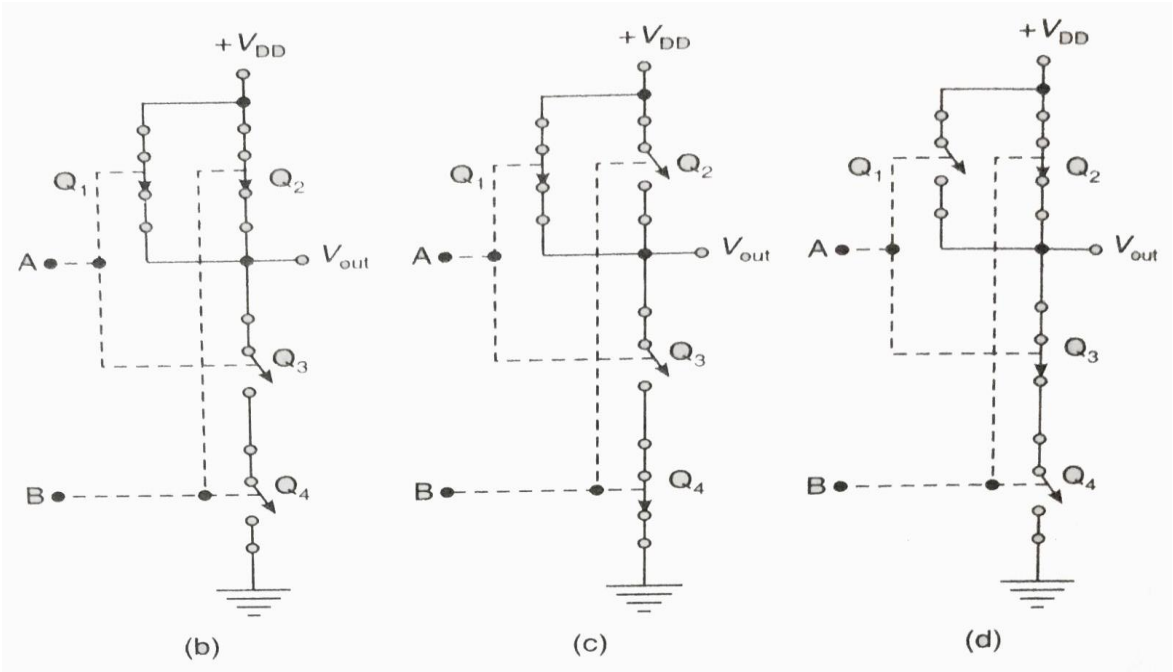
Logic Family	Propagation delay time (ns)	Power dissipation per gate (mW)	Noise Margin (V)	Fan-in	Fan-out	Cost
TTL	9	10	0.4	8	10	Low
CMOS	<50	0.01	5	10	50	Low
ECL	1	50	0.25	5	10	High

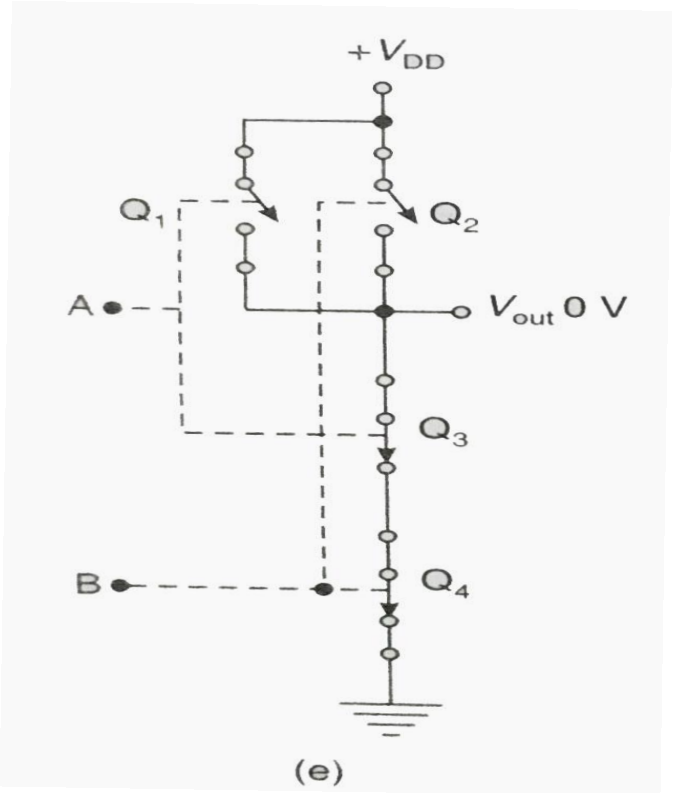
CMOS NAND Gate

- Figure shows a CMOS two-input NAND gate and its equivalent circuits for various input combinations.



- Here Q_1 and Q_2 are parallel-connected PMOS transistors, and Q_3 and Q_4 are series-connected NMOS transistors.





(e)

- When A = 0 V and B = 0 V, $V_{GS1} = V_{GS2} = -5$ V, $V_{GS3} = V_{GS4} = 0$ V. So Q_1 is ON, Q_3 is OFF, Q_2 is ON and Q_4 is OFF. Thus, the switching circuit (b) results with $V_{out} = +5$ V.
- When A = 0 V and B = +5 V, $V_{GS1} = -5$ V, $V_{GS2} = 0$ V, $V_{GS3} = 0$ V, $V_{GS4} = 5$ V. So Q_1 is ON, Q_3 is OFF, Q_2 is OFF and Q_4 is ON. Thus, the switching circuit (c) results with $V_{out} = +5$ V.
- When A = +5 V and B = 0 V, $V_{GS1} = 0$ V, $V_{GS2} = -5$ V, $V_{GS3} = 5$ V, $V_{GS4} = 0$ V. So Q_1 is OFF, Q_3 is ON, Q_2 is ON and Q_4 is OFF. Thus, the switching circuit (d) results with $V_{out} = +5$ V.
- When A = +5 V and B = +5 V, $V_{GS1} = V_{GS2} = 0$ V, $V_{GS3} = V_{GS4} = 5$ V. So Q_1 is OFF, Q_3 is ON, Q_2 is OFF and Q_4 is ON. Thus, the switching circuit (e) results with $V_{out} = 0$ V.