End of Term Project Report
Eliot Nichols
Erik Johnson
Sam Whisler
EE 331 Lab, Spring 2019

1.1 Introduction

This document is a report on the design and implementation of a voltage doubling circuit simulating a battery powered device. While it may not seem obvious, DC to DC voltage multipliers are ubiquitous with modern electronics. Electronic devices are made up of a variety of sub-circuits, many of which require varying voltages, including those higher than the DC voltage output of the battery. Because of how common these circuits are, this project is intended to simulate a portable electronic device, by rectifying an AC source to simulate a battery, and using that as a primary source to create a higher value DC voltage. In Section 2, the design of the circuit is explained including the component values chosen. In Section 3, the results of the design simulation and the observed behavior of the physical circuit are explained. In Section 4, the circuit is analyzed for varying load values and the results are explained. Finally, in Section 5, overall results are discussed and conclusions are made.

1.2 Purpose

As previously mentioned, the purpose of a DC to DC voltage multiplier is to produce a DC voltage independent of the battery voltage that's used to power the device. An example of where this circuit is necessary is the flash in a digital camera. Most digital cameras operate with batteries voltages of 1.5 to 3 volts, but it can require thousands of volts to produce the capacitive flash found on many cameras. By using highly efficient and large magnitude voltage multipliers, the 1.5 volts is able to be augmented to produce a voltage of this scale. Without this circuit type, devices would need to contain many batteries of different voltages to power all components, taking up a large amount of space and complicating the circuitry.

2.1 Circuit Design

First we needed to design a rectifier to convert the 7.5 V AC of the transformer to a DC voltage. We chose to use a half wave rectifier to keep as much of the peak voltage as possible. This is a relatively simple circuit, with a single diode from an AC source, with a resistor and capacitor in parallel for the load, as shown below in Figure 2.1.1.

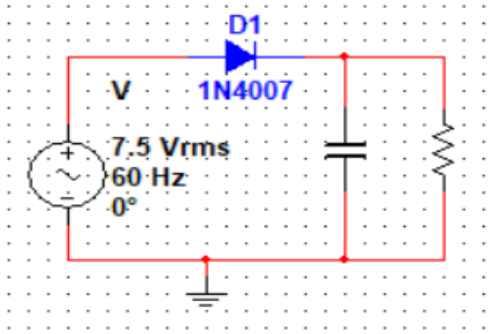

Figure 2.1.1: Circuit diagram for half-wave rectifier with RC load.

For our multiplier circuit, we chose to use the voltage multiplier circuit from Experiment 4 Procedure 12 in our design. To us, this was the best way to multiply our voltage, as it multiplies a DC input voltage. We just needed to create a clocking signal for the transistor and the multiplier to work. Shown below in Figure 2.1.2 is the circuit diagram for the multiplier circuit.

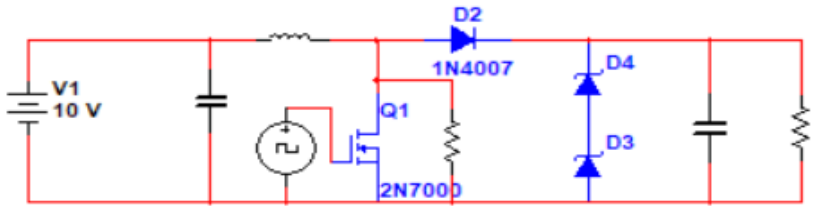

Figure 2.1.2: Circuit design for voltage multiplier with DC input and clocking signal on the transistor.

To create the clocking signal for the transistor, we considered the square wave generator and the ring oscillator, but ultimately settled on using the stable NAND gate oscillator circuit, shown below in Figure 2.1.3. This circuit was well rated for output quality, had adjustable period, and did not require a large capacitor, which is why we chose it.

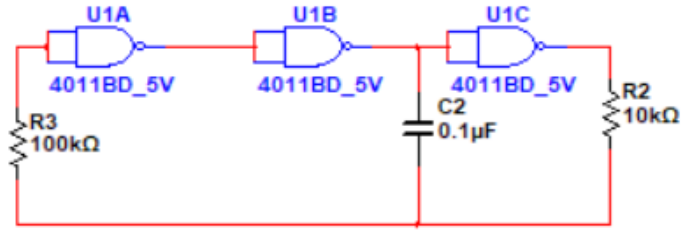

Figure 2.1.3: Stable NAND gate oscillator. Creates a stable square wave so long as $R_3 = 10R_2$. The period is proportional to R_2C.

2.2 Components

In the rectifier design, we were aiming for a ripple voltage of the rectifier to be less than 90 mV. Using the equation for half-wave ripple for the 60 Hz input, we know we need an RC value of 1.82 sec. We chose a 100 kΩ load resistor to lower the current and power dissipation, which means we needed a capacitor of size 18.2 μF or larger. We had two capacitors larger than this in our kit from the previous prerequisite EE courses, a 330 μF and a 1 mF capacitor. We chose the 330 μF because it was more than enough to achieve our ripple voltage, and left the 1 mF for our output. We just used a standard diode to rectify the voltage, which was a N4007 diode.

For the multiplier circuit, we chose to use a 100 mH inductor because it was used in the lab experiment, and was the one provided in our lab kit. We kept the load resistor the same as the example circuit (10 kΩ) and used the 1mF capacitor as it was the only capacitor we had left capable of limiting the output ripple to less than 1%. We did not use a capacitor before the inductor as this is where the rectifier capacitor would connect. We initially chose a JFET transistor, but ended up using an NMOS as it worked with a 50% duty cycle. We also chose to not use the resistor across the transistor unless our output was a problem. For the Zener diodes, we used a N4744A and N4732A because the 4744 has a Zener voltage of 15 V, and the 4732 has a Zener voltage of 4.7, which should regulate our output at 19.7 V.

The NAND gate oscillator uses the CD4011BE chip, and we chose resistor and capacitor values similar to the square wave oscillator from Experiment 5 Procedure 6, as they behave similarly. component values are shown in Figure 2.1.3.

3.1 Spice Design

We essentially combined the 3 circuit elements of our design process into one circuit. First, the rectifier circuit was built and tested in SPICE. The circuit diagram is shown in Figure 3.1.1. We then constructed the voltage multiplier circuit and used the oscillator circuit to drive the switching transistor. We changed components in our rectifier to reduce its ripple when the load was applied because we misread the specifications and thought the ripple needed to be less than 1% with a load. We chose not to change them back as the circuit was only performing better in this case. The final circuit design for SPICE is shown below in Figure 3.1.2. We originally tried using the chip form of NAND gate, but the simulation would not run properly. By using the single gate elements we were able to get a running simulation.

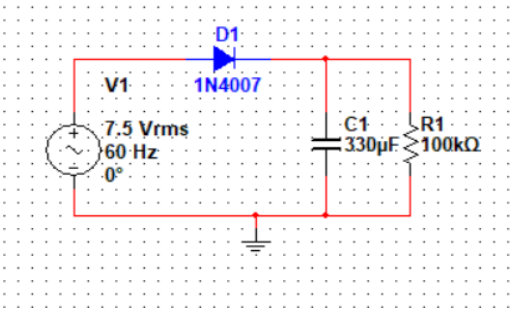

Figure 3.1.1: SPICE design for half-wave rectifier with RC load. R = 100 kΩ and C = 330 µF.

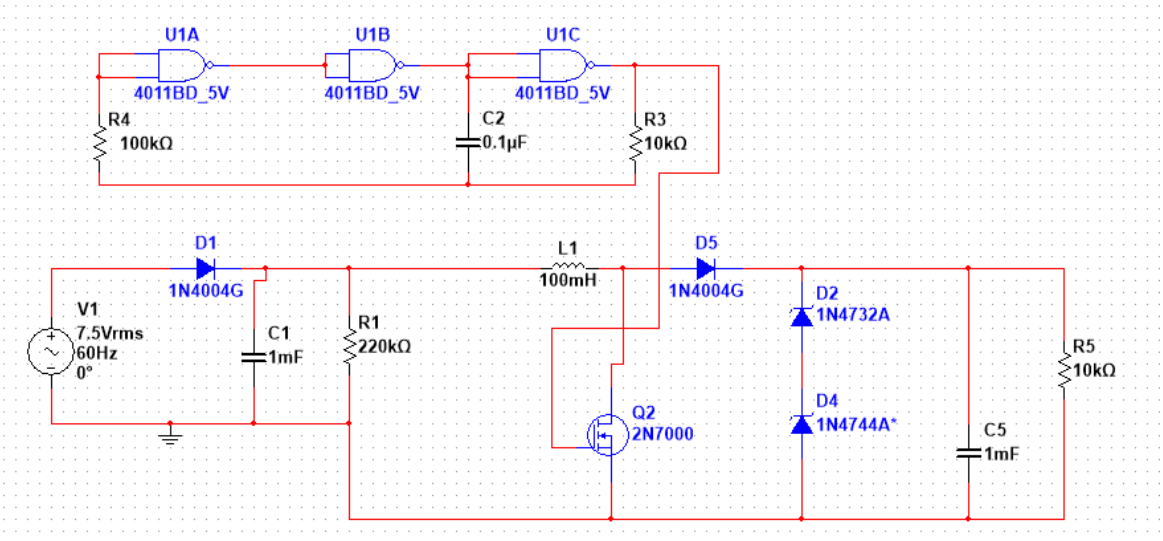

Figure 3.1.2: Complete circuit used to rectify lab transformer voltage and double its magnitude with minimal ripple voltage on the output. A half-wave rectifier is used to create a DC voltage, a boost converter is used to double its magnitude, and a stable NAND gate oscillator is used to drive the switching transistor.

3.2 Spice Results

The implementation of the rectifier went very smoothly. By using the half-wave, our output voltage was about 9.9 V, and we had essentially no ripple. The results of the SPICE simulation are shown below in Figure 3.2.1, and a zoomed in look at the ripple is shown in Figure 3.2.2.

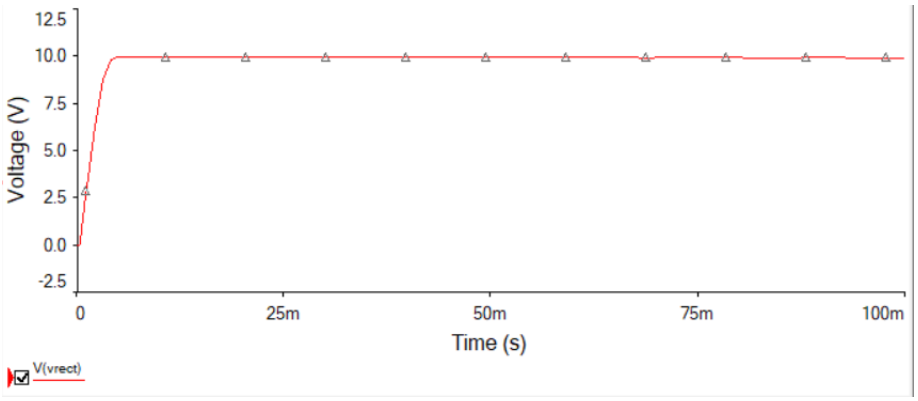

Figure 3.2.1: Rectifier circuit output in SPICE simulation. Output voltage stable just under 10 V.

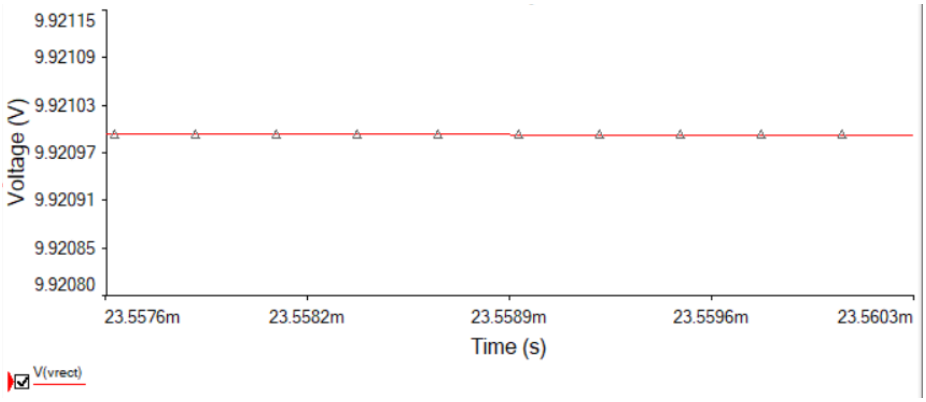

Figure 3.2.2: Zoomed in view of steady-state output voltage. Ripple voltage is essentially zero.

We built the multiplier circuit using our rectified voltage as the DC input, and initially used a square wave generator at the gate of the transistor, just to test that part of the circuit. The output looked like we expected, in the steady state our output remained at 19.7 V, with less than 100 mV of ripple. Creating the clocking signal from the DC source gave us the most trouble during simulation. We tried using the square wave oscillator from lab 5, but would not see a square wave in SPICE, just a solid voltage. We had no luck getting any other results, so we tried using the ring oscillator from lab 5. Again, our SPICE output would not produce the results we expected from our lab 5 experiments. After doing some research, we found a modification of the square wave oscillator that was highly rated for producing a stable square wave. We tried building this circuit using the chip model in SPICE and had no output, it did not seem to work.

We tried using the individual gates in the simulation, as in Figure 3.1.2, and we were finally able to create the entire voltage doubling circuit. The results of the simulation using a 10 kΩ load are shown below with output voltages shown in Figure 3.2.3 and the voltage doubler ripple shown in Figure 3.2.4.

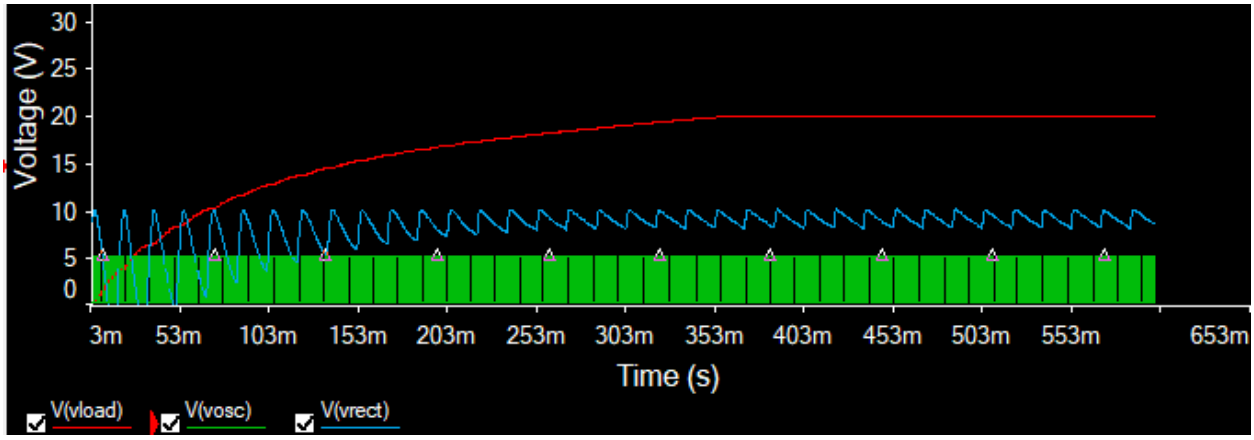

Figure 3.2.3: SPICE simulation results. Output of voltage doubler shown in red, with the rectified voltage shown in blue, and the oscillator voltage shown in green.

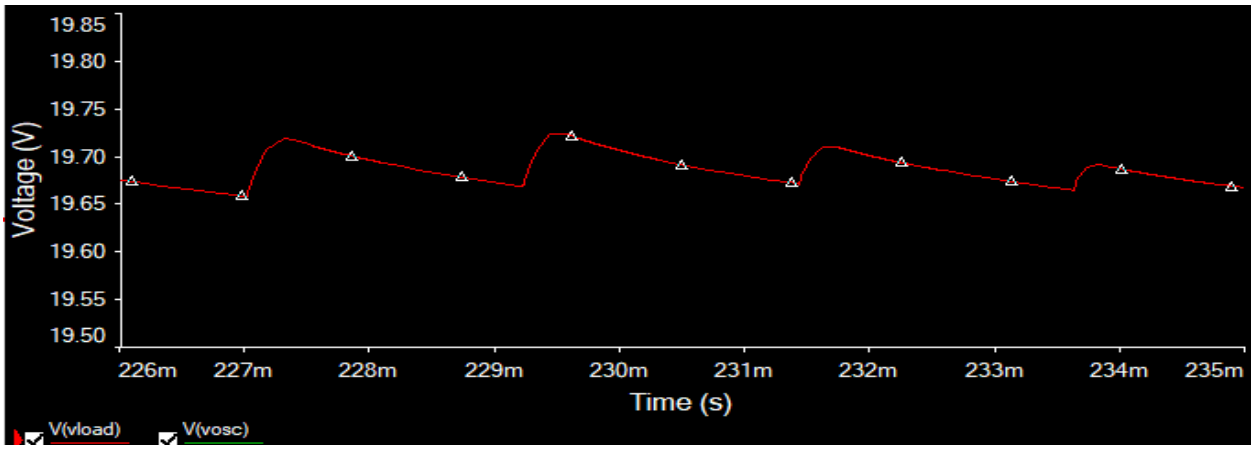

Figure 3.2.4: Zoomed in view of ripple voltage. Simulation shows ripple less than 100 mV.

During simulation, we were not able to reduce the ripple in the rectifier while the doubler circuit was loaded, despite trying larger values of capacitance and resistance for our rectifier load. We decided to build the physical circuit at this point and see if we could replicate our simulation with the actual circuit.

3.3 Implemented Circuit

The design from SPICE was built into a physical circuit. The circuit diagram is shown below in Figure 3.3.1. From the CD4011BE datasheet, we knew the chip could be powered using 10 V as well as 5, so we used the full output of the rectifier to power the chip. The breadboard circuit is shown below in Figure 3.3.2. The rectified DC voltage was used as the boost converter input. The stable NAND gate oscillator was used on the transistor to create a clocking signal with a duty cycle of 50%, which should double the input voltage of the boost converter.

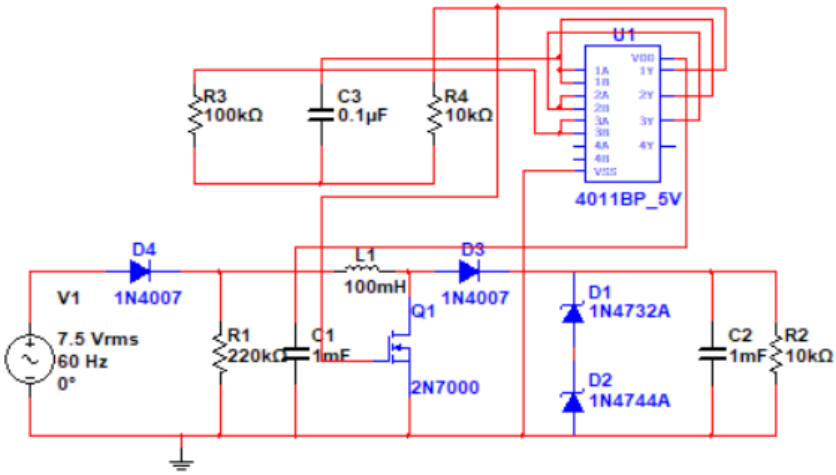

Figure 3.3.1: Circuit diagram for physical implementation of design. Circuit uses a half-wave rectifier, NAND gate chip for oscillator, and a DC boost converter.

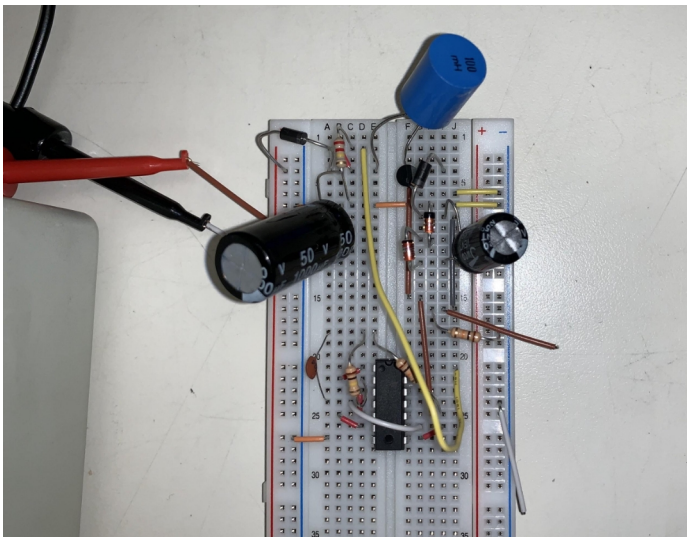

Figure 3.3.2: Physical circuit as it was built on the breadboard.

3.4 Results

The physical circuit was connected to the oscilloscope to observe the output behavior. The testbench DMM was also used to measure the voltage output. Shown below in Figure 3.4.1 are the output voltages measured for the voltage doubler in open circuit.

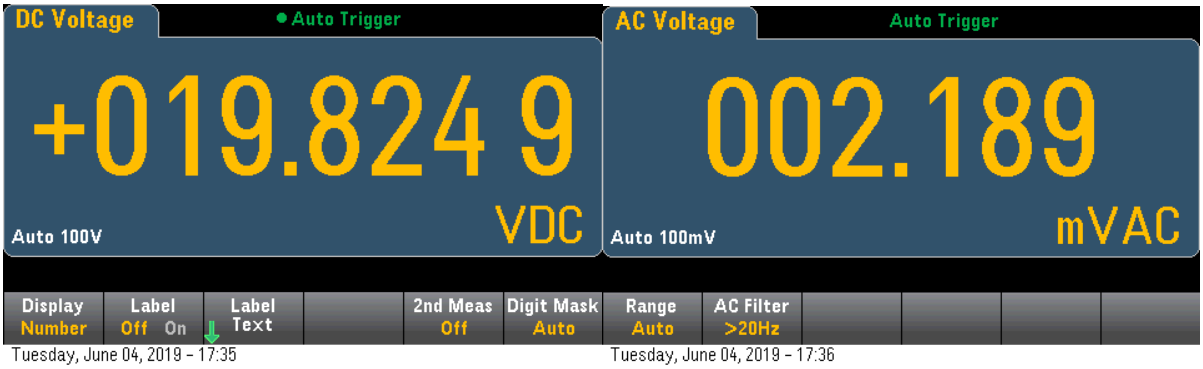

Figure 3.4.1: The left image shows the DMM measurement for the output voltage in open circuit. This voltage needed to fall between 18.5 V and 20 V, with ours being 19.8 V. The right image shows the AC output of our doubler, which is used to determine the ripple voltage produced in our completed circuit. This voltage needed to fall within 1% of the output voltage, with ours being just 0.03%.

Using the AC amplitude, which is given in rms, we can calculate the ripple by multiplying the amplitude by 2 to get peak-to-peak and adjusting for rms by multiplying by $\sqrt{2}$ (Ex: 2.189 * 2 * $\sqrt{2}$ = 6.2 mV). Though this is not exact, it is a good approximation of the actual ripple in the output. Shown below in Table 3.4.1 are the measured output voltages, both magnitude and ripple, as recorded by the oscilloscope and the testbench DMM.

Table 3.4.1: The measured output results using both the oscilloscope and the testbench DMM.

Voltage Measurement	Oscilloscope	Testbench Digital Multimeter
Doubler Magnitude	19.9 V	19.82 V
Doubler Ripple	40 mV	6.2 mV
Rectifier Magnitude	9.7 V	9.57 V
Rectifier Ripple	80 mV	15.8 mV

The oscilloscope only seemed to measure in increments of 40 mV, so we were not very confident in the measurement accuracy. However, using either reading our ripple voltage is below the required 1% threshold. Our overall output ripple was much better than it needed to be, at worst being 0.2% ripple.

4.1 Analysis

After confirming that the circuit produced the proper output specifications, it was time to test the circuit response to varying loads. We recorded the load current for loads varying from 100 Ω to 1 MΩ. The recorded currents are shown below in Table 4.1.1, with the calculated load voltage shown based on measured current.

Table 4.1.1: Measured currents for varying values of load resistance, with voltage calculated based on current.

Load Resistance (Ohms)	Load Current (Amps)	Load Voltage (Volts)
100	2.90E-02	2.90
470	1.85E-02	8.70
1000	1.21E-02	12.14
4700	4.24E-03	19.92
10000	2.01E-03	20.14
20000	1.01E-03	20.18
33000	6.07E-04	20.04
53000	3.80E-04	20.16
100000	2.02E-04	20.25
153000	1.32E-04	20.24
240000	8.35E-05	20.04
480000	4.18E-05	20.05
633000	3.18E-05	20.11
1000000	2.05E-05	20.45

Based on the measured currents, we see that the circuit performs quite well in maintaining a voltage of about 20 V at the output. The voltage was nearly constant for loads of about 5 kΩ and greater. Loads smaller than 5 kΩ require a larger current to reach the 20 V, which was greater than our circuit could provide. In these cases the output voltage is no longer 20 V, so the Zener diodes are not in reverse breakdown, and all the current is going through the load. We have plotted the results in Figure 4.1.1, shown below, with load resistances plotted on a logarithmic scale. The plot shows the effective range of load resistance for which the voltage is regulated, and that the current increases more rapidly at the point the voltage is no longer regulated.

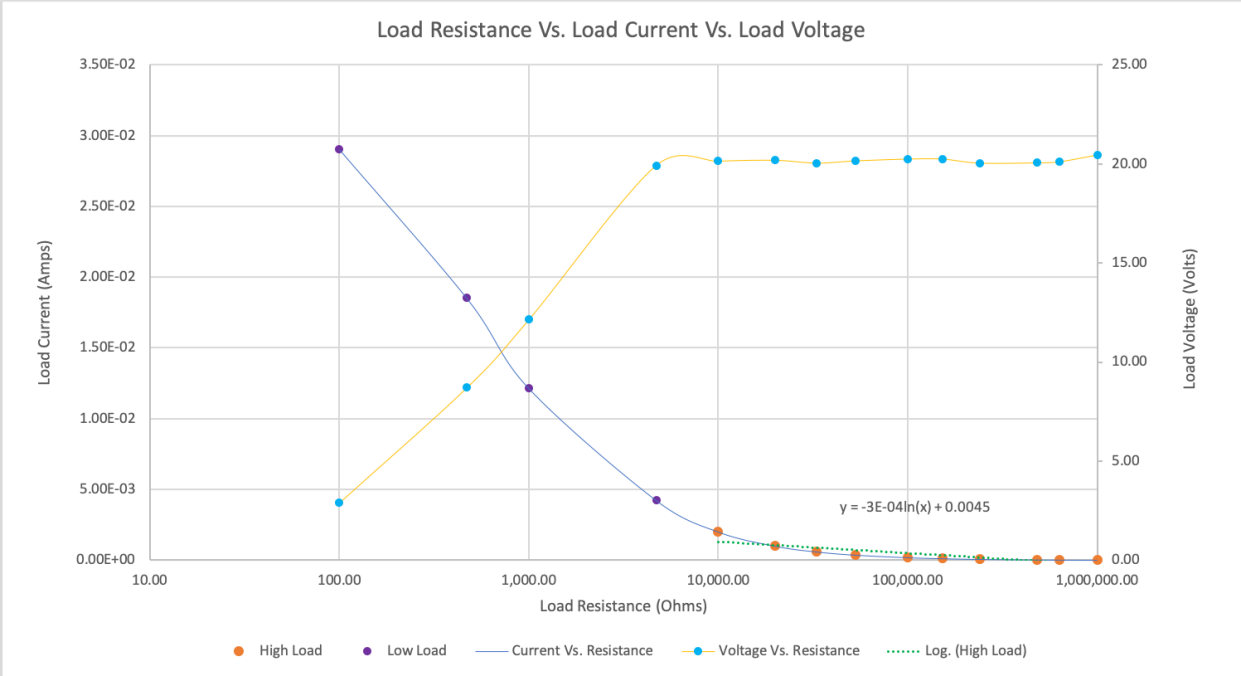

Figure 4.1.1: Current (along the blue line) and voltage (along the yellow line) of load plotted against load resistance. Resistance is shown on a logarithmic scale.

Overall our circuit performed quite well, better than we expected. We felt that perhaps because we designed it with a 10 kΩ load, it performed well for loads as small as 5 kΩ. The overall process was a success, we were able to build a circuit that met the design specifications. For the rectifier and multiplier components of the circuit, both our simulation and physical results were as we expected them to be, with no notable deviations. However, for the oscillator component of our circuit we had several challenges and failures. SPICE was very challenging to work with at times, sometimes producing erroneous results or failing to run at all. We were able to use several versions of oscillators to produce a square wave in SPICE, but only the stable NAND gate oscillator actually worked for us when connected to the transistor gate and only if using the individual gates and not the chip model. This was the largest factor in choosing the oscillator in our design.

We also had some struggles getting the oscillator to work properly in the physical circuit. With 5 V powering our chip, the output wave was very uneven and spiky. It did oscillate between 5 and 0 V, but did not have the profile of a square wave, and did not work with our boost converter. We tried using using the square wave oscillator, but that also had a poor output. We thought maybe it wasn't getting the proper 5 V supply, and then after looking at the datasheet, realized we could power the chip with 10 V as well. At this point we went back to the stable NAND gate oscillator and powered it with the full rectified voltage. The output looked much better, producing a perfect square wave with a 50 % duty cycle. When connected to our boost converter, we began to see the results we expected, and our voltage doubler circuit was complete.

5.1 Conclusion

As mentioned in the purpose of the project report, the goal of this project was to develop an understanding of how the DC-DC voltage multiplier circuit works, as well as understanding how each component and subcircuit affect the final voltage output of the multiplier. In completing the project, we were able determine these relationships. One of the primary observations we made was that any variances in the output of a subcircuit early on would be magnified further into the circuit. Because of this, we sought to reduce the ripple voltage of the rectifier subcircuit to as small as we could reasonably attain, to prevent a larger ripple on the multiplier output. In the process of constructing the multiplier, we also determined that large capacitors were often the most effective way of reducing noise in the voltage throughout the circuit, but come with the tradeoffs of increasingly large time delays and inappropriately large circuit packaging.

Following completion of the entire DC to DC multiplier, we analyzed the circuit output in order determine any constraints that may be placed on the system by external connections. One important external factor, the load resistance, was found to be incredibly important for the proper operation of the multiplier. If the load resistance is too small, the load current can become too large, and the power capabilities of our circuit limit the load current. This causes the voltage regulation of our circuit to fail, and the load voltage is determined by the current our circuit can provide. For our circuit, load resistances less than 10k ohms should be avoided to ensure the desired output voltage is supplied.

The intent of this project was to combine the major concepts of each weekly lab and relate them to a common and applicable circuit. By successfully completing and understanding the prior labs and topics discussed in lecture, we were able combine circuit elements of completed experiments and build a circuit to produce our target specifications.