Lecture 14 - Mon Mar 2

Test Stats

1. ½ of you got it done in ½ the time - so not too long.
2. Everybody managed to answer in the space given - so enough paper.
3. Averag 264.3 out of 300 (so high B).
4. Low 141, high 300 out of 300.
5. It is graded - but I can't return it - I still have a couple of people that have yet to take it. So hopefully by Wednesday.

Homework

1. Homework 2 is nearly done getting graded - and will soon be return.
2. Homework 3 . Hm..
3. Homework 4 - Build a MARIA emulator.

In the News

Tesla (using to-silicon AI chip): https://asia.nikkei.com/Business/Automobiles/Tesla-teardown-finds-electronics-6-years-ahead-of-Toyota-and-VW2

Googles Overview of TPU: https://cloud.google.com/blog/products/gcp/an-in-depth-look-at-googles-first-tensor-processing-unit-tpu

History of of the von Neumann architecture

From 1945 - first published. From his 1945 description:

MAR	Memory Address Register	Holds the memory location of data that needs to be accessed
MDR	Memory Data Register	Holds data that is being transferred to or from memory
AC	Accumulator	Where intermediate arithmetic and logic results are stored
PC	Program Counter	Contains the address of the next instruction to be executed
CIR	Current Instruction	Contains the current instruction during processing

	Register	

We are calling the CIR the IR.

The Fetch-Execute cycle is the process where we get an instruction from memory into the IR, decode it in the control system, move and process data (the ALU or just movement) and then apply this to Input and Output.

Used in Testing (For more complicated tests). PostgreSQL (141281 tests), SQLite, Linux Network Stack, Ethereum.

Used For Building interpreters. Example:

Overview of Fetch/Execute.

TPU's - non fetch-execute

How Tesla's processor and Google TPU works.

What is a Tensor and how do they flow?

What is a Neural Network?

Copyright