Name: Student ID: Signature:

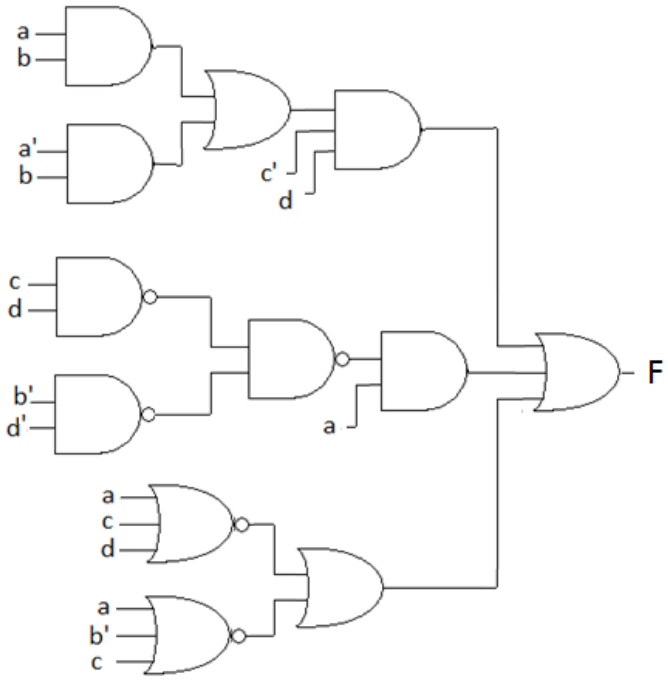
Fall 2015 BSM 203 Logic Circuits Midterm Exam

Instructions:

- The duration of this exam is 90 mins.
- Note that there are 3 main questions and 2 bonus questions in this exam.
- Bonus questions will not be evaluated unless you work on all main questions.
- Be clear in your answers. You can use as many answer sheets as you need.
- If you write in Turkish, there will be a penalty for each sentence/word that you wrote.
- Please put your name and your number, and sign for both exam paper and answer sheets.

Questions:

1) [40points] Consider the following circuit.



a) Specify each gate output on the figure. You ***can*** simplify while writing the gate outputs whenever it is possible. Please write expression for F below.

b) Simplify the expression of F (without Karnaugh maps), you can use Appendix A.

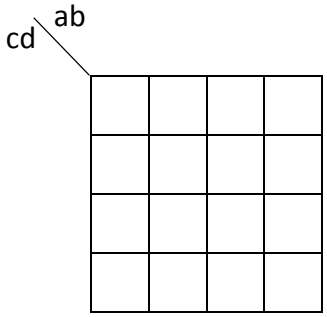
c) Complete the truth table below.

a	b	c	d	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

d) Express F in minterm expansion.

F =

e) Show F on Karnaugh map.



i) Specify the essential implicants.

ii) Write the simplest form of F below.

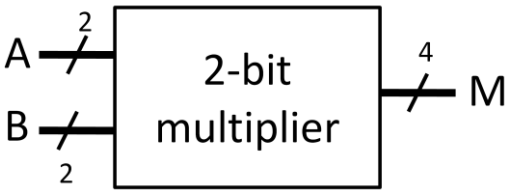
iii) Is there any static-1 hazard? If yes, write the hazard-free expression of F.

f) Now consider m_2, m_{12} and m_{14} are don't cares. Simplify F in

i) sum-of-product form

ii) product-of-sum form.

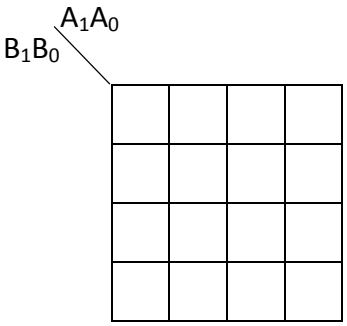
2) [60 points] Consider a circuit which has two 2-bit unsigned integers as inputs, A and B. Bits of A is shown as A_1A_0 and bits of B is shown as B_1B_0. The circuit multiplies these two numbers and the output M is a 4-bit number ($M_3M_2M_1M_0$).



a) Complete the truth table below.

A_1	A_0	B_1	B_0	M_3	M_2	M_1	M_0
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

b) Show the output M_1 on the Karnaugh map below.



c) Specify M_1 in sum-of-product (AND-OR) form below.

d) Design the circuit if number of inputs is limited to 3.

e) Redesign the circuit with only NAND gates (you can add inverters if needed).

f) The gate prices are shown Table I. Based on the table, which design is the cheapest?

BONUS A [30 pts]: Can you find a cheaper design?

BONUS B [30 pts]: Design the full circuit with minimum number of gates.

BONUS C [20 pts]: Can you design the full circuit by using a PLA?

Tablo 1

Gate	2-input	3-input	4-input
AND	3	5	8
OR	2	4	9
NAND	1.5	5	6
NOR	1.75	3	7
XOR	2	6	10
Inverter	1		

APPENDIX A

$X + 0 = X$

$X + 1 = 1$

$X + X = X$

$X + X' = 1$

$XY = YX$

$(XY)Z = X(YZ)=XYZ$

$X(Y + Z) = XY + XZ$

$XY + XY' = X$

$X + XY = X$

$(X + Y')Y = XY$

$(X + Y)' = X'Y'$

$(X + Y)(X' + Z) = XZ + X'Y$

$X \oplus 0 = X$

$X \oplus 1 = X'$

$X \oplus X = 0$

$X \oplus X' = 1$

$(X \oplus Y)' = X \equiv Y$

$XY + X'Z + YZ = XY + X'Z$

$X.1 = X$

$X .0 = 0$

$X . X = X$

$X . X' = 0$

$X + Y = Y + X$

$(X+Y)+Z = X+(Y+Z)=X+Y+Z$

$X +YZ = (X + Y)(X + Z)$

$(X + Y)(X + Y') = X$

$X(X + Y) = X$

$XY' + Y = X + Y$

$(XY)' = X' + Y'$

$XY + X'Z = (X + Z)(X' + Y)$

$X \equiv 1 = X$

$X \equiv 0 = X'$

$X \equiv X = 1$

$X \equiv X' = 0$

$(X \equiv Y)' = X \oplus Y$

$(X + Y)(X' + Z)(Y + Z)=(X + Y)(X' + Z)$