Fall 2016

BSM 203 Logic Circuits

Homework #2

Instructions:

- The due date for this homework is ***November, 10 at 3:00 pm***.
- You can hand in your homework before the class starts, drop it to room 1153, or send it via e-mail (saubsm203@gmail.com) with a subject line "BSM 203 – Homework 2 - <student name> - <student number>"with condition of handing in the hardcopies later.
    - Only the e-mail with proper subject line will be accepted
    - Student is responsible to check the attachment to emails. Instructor may not notice no-attachment e-mails and therefore cannot be hold responsible for warning student in time.
    - You can send photos of a handwritten homework, but have to hand in the hardcopies. Without hardcopies, homeworks will not be evaluated from photos. This is also valid for other types of e-mailed homeworks. Please write the following statement on to your late handed-in homework: "A softcopy of this homework is submitted before the deadline."
- Note that there are 4 questions in this homework.
- Homework will not be accepted after due date unless instructor suggested otherwise.
- All students are expected to work individually. Discussions among students are encouraged, but homework must be prepared, written, and submitted individually.
- Do not waste your time by googling the homework questions. Solving may take much shorter time.
- If the hardcopy homework has more than one paper sheet, then you should staple the sheets close to upper left corner such that no writings is blocked.

Honor code:
As student(s) who has/have signature(s) below, I/We pledge that I/we follow the rules of honor code below and directions above while doing the homework.

1-) Students can only share information (especially answers) within the group (if it is a group homework), but not with other students in class or in other programs. However methods can be discussed.
3-) Sharing questions or answers outside of institution, on social media, on homework websites, or any other similar medium is strictly forbidden.
4-) If honor code and directions are not followed, the instructor has right to pursue any legal actions specified in university regulations.
5-) Homeworks without signatures will not be accepted.

Student Number	Name and Surname	Signature	Date

Questions:

1) [15 points] [Karnaugh Maps] Find F and F' in minimum sum-of-product form and F in minimum product-of-sum for each question below.

a)

x	y	z	F
0	0	0	X
0	0	1	X
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

b) $F(a, b, c, d) = \sum m(1, 3, 5, 7, 9, 11, 13, 15) + \sum d(0, 4, 6)$

c) $F(a, b, c, d) = \prod M(4, 5, 6, 8, 9, 10) + \prod D(11, 12, 14)$

d) $F = PQSR + P'QR + QSR' + PSR + PQS' + P'QR' + Q'SR$

2) [25 points] [Karnaugh Maps] For each function below, list all prime implicants, underline (or circle) the essential prime implicant on the list, and find minimum sum-of-product solution.

a) $F(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 6, 7, 8, 10, 13, 15)$

b) $F(w, x, y, z) = \sum m(0, 2, 3, 4, 7, 8, 9, 14)$

3) [35 points] [Multi-level gate circuits] Truth table for three functions is given on the right. Please answer the following questions based on this truth table.

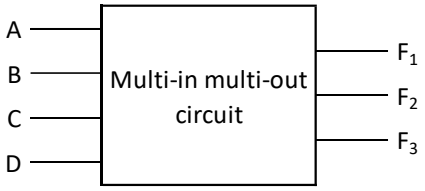
A	B	C	D	F_1	F_2	F_3
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	1
0	0	1	1	1	0	1
0	1	0	0	0	0	0
0	1	0	1	1	0	1
0	1	1	0	0	1	1
0	1	1	1	1	1	1
1	0	0	0	1	1	0
1	0	0	1	1	1	0
1	0	1	0	1	0	1
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	1	1	0
1	1	1	0	0	1	1
1	1	1	1	1	1	1

a) If the number of inputs for each gate is limited to 2, find F_1 with minimum number of gates.

b) Draw the circuit for F_2 in OR-AND, NOR-NOR, AND-NOR, and NAND-AND structure.

c) Draw the circuit for F_3 in AND-OR, NAND-NAND, OR-NAND, and NOR-OR structure.

d) For the multiple-input, multiple-output circuit (shown below), implement the circuit by using minimum number of gates with only AND, OR gates, and inverters.



e) Re-implement the circuit that you implemented in (d)
   i) by using only NAND gates
   ii) by using only NOR gates

f) [**Bonus 20 pts**] For the price table given below, what would be the minimum-cost solution for the circuit in (d)?

Nuber of inouts	NAND	NOR	AND	OR	XOR
2	1	1	2	2	2
3	2	3	4	4	2
4	3	4	6	5	7

4) [25 points] [Multi-level gate circuits and Combinational Circuit Design] Answer the questions below based on the truth table given in previous question.

a) Find the minimum sum-of-product solution for F_1.
   i) Draw the circuit.
   ii) Assume that delays in inverters are 10 ns and, in gates, delays are 20 ns. If A =1, B = 0, and C =1, draw the timing diagram for 120 ns where initially D = 0, input B becomes 1 at time 40ns and becomes 0 again at 80 ns, and input D becomes 1 at time 60 ns and becomes 0 at 100 ns. (The rest of the inputs stay unchanged).
   iii) Show 1-Hazards on Karnaugh Map. How can the hazards be eliminated (re-write the expression in sum-of-product from)?

b) Find the minimum product-of-sum solution for F_2.
   i) Draw the circuit.
   ii) Assume that delays in inverters are 10 ns and in gates, delay are 20 ns. If A =1, B = 0, and C =1, draw the timing diagram for 120 ns where initially D = 0, and input C becomes 0 at time 40ns and becomes 1 again at 80 ns.
   iii) Show 0-Hazards on Karnaugh Map. How can the hazards be eliminated (re-write the expression in product-of-sum from)?