

Fall 2014

BSM 203 Logic Circuits

Final

Name:

Student ID:

I. Education ☐ II. Education ☐

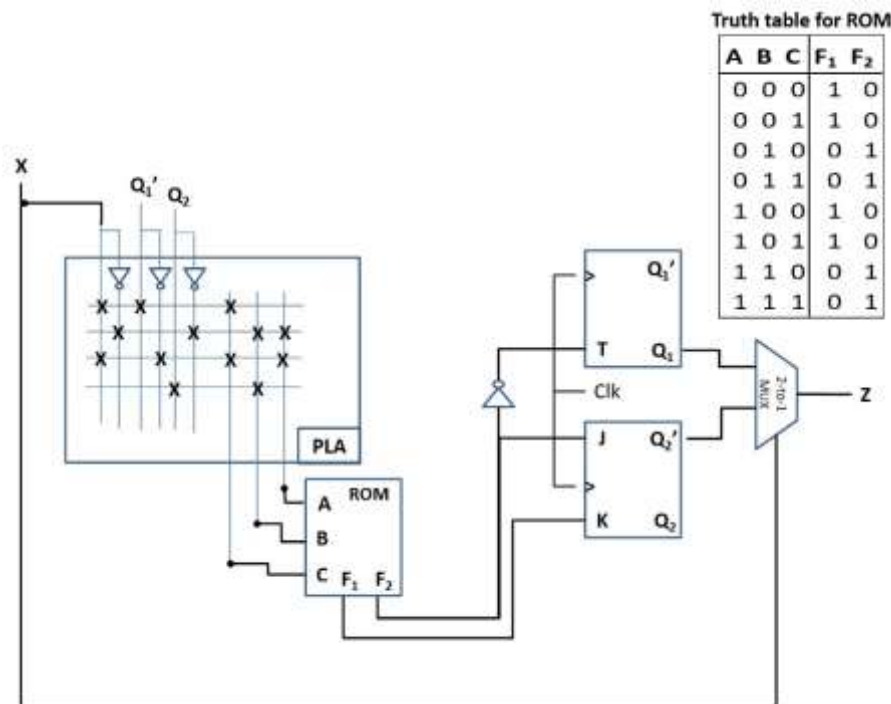
Signature:

Instructions:

- The duration of this exam is 90 mins.
- Note that there are 2 questions in this exam.
- Be clear in your answers. You can use as many answer sheets as you need.
- If you write in Turkish, there will be a penalty for each sentence/word that you wrote.
- Please put your name and your number, mark your class, and sign for both exam paper and answer sheets.

Questions:

1) [40 points] [Analysis of Clocked Sequential Circuits] Consider the circuit shown below.



(a) Derive the FF input equations (J, K, T), FF next state equations (Q_1^+ and Q_2^+), and output equation (Z).

T =

J =

K =

Q_1^+ =

Q_2^+ =

Z =

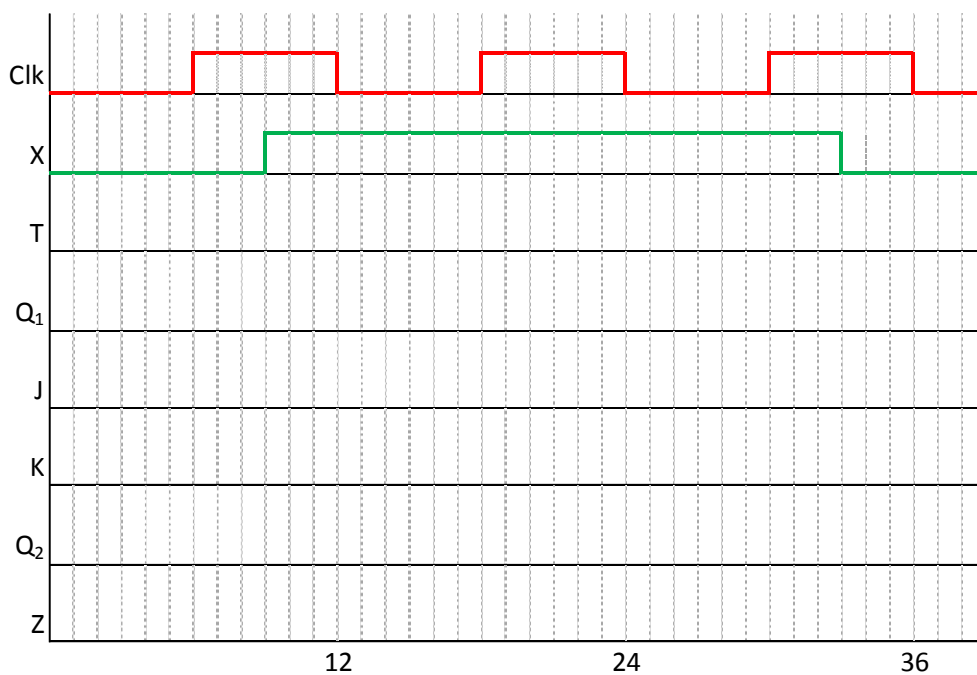
(b) Is this a Mealy Machine or Moore Machine? Explain your answer in one sentence below.

(c) Construct a state table and graph below.

Transition Table			Next State Table		
Q_1Q_2	$Q_1^+Q_2^+$		Present State	Next State	
	$X=0$	$X=1$		$X=0$	$X=1$

State Graph

(d) Complete the timing chart shown below for the circuit for an input sequence $X=010011$ and the clock period 12ns. Assume that FF is falling-edge triggered, that initially $Q1 = Q2 = 0$, and that X changes midway between the rising and falling clock edges. The delays in ROM, PLA, and MUX are 1 ns for each and delay in each FF is 2 ns. The delay in OR gate is negligible.



2)

- a)

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Hint:

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X

$$Z:$$

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Next State Table			
Present State	Next State		Output
	X = 0	X = 1	

State Graph

S.

	X = 0	X = 1	Z

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For Mealy Machine:

Step 1: Derive the state graph and the state table.

Next State Table		
Present State	Next State	
	X = 0	X = 1

State Graph

Step 2: Decide how many FFs you need and, based on your decision, derive the transition table.

Transition Table		
	X	
	X = 0	X = 1

Step 3: Decide the type of FF you want to use and, derive FF input equations.