HELLO... CACHE CONTROLLER HERE...!

CLOCK NUMBER 00000101

@echo: Variables Are Properly Initiated.

FIRST WRITE REQUEST --> ADDR:16, DATA:12 DATA WRITE REQUESTED SUCCESSFULLY...!

CLOCK NUMBER 00000110

@echo: CPU can proceed to the next instruction from here.

LOADING THE SAME DATA (ADDR: 16)

LOADED SUCCESSFULLY...!
CLOCK NUMBER 00001100

CPU DATA IN LINE: 000000000000000000000000001100

@echo: Observe that the data is only available after five more clock cycles from

Write Request.

@echo: This is because controller will consider the line valid only after

neighbouring elements are fetched from Main Memory

CACHE LINE: 1
TAG: 0000000

VALIDITY: 1

DIRTY: 1

WRITE REQUEST ON THE SAME LINE...! --> ADDR: 2064, DATA: 23

DATA WRITE REQUESTED SUCCESSFULLY...!

CLOCK NUMBER 00001101

-----ANALYZING THE MEMORY CONTENT-----

CLOCK NUMBER 00010011

@echo: Overiding the cache line, forced the content in the first primary cache line to a line in the victim cache.

CACHE LINE: 1 TAG: 0000001

VALIDITY: 1

DIRTY: 1

VICTIM LINE: 0

TAG: 0000000000001

VALIDITY: 1

DIRTY: 1 NMRU: 11

```
READING THE EARLIER DATA AGAIN(ADDR: 16)
LOADED SUCCESSFULLY...!
CLOCK NUMBER 00010110
    16:
CPU DATA IN LINE:
              0000000000000000000000000000001100
-----ANALYZING THE MEMORY CONTENT------
CLOCK NUMBER 00010111
@echo: Victim Hit: Data will be swapped between primary cache and victim cache.
CACHE LINE:
         1
TAG:
    0000000
VALIDITY:
DIRTY: 1
VICTIM LINE: 0
TAG: 00000010000001
DATA:
    00: 0000000000000000000000000000010111
                             VALIDITY:
DIRTY: 1
NMRU:
    11
FILLING THE VICTIM...!
DATA WRITE REQUESTED SUCCESSFULLY...!
CLOCK NUMBER 00011000
DATA WRITE REQUESTED SUCCESSFULLY...!
CLOCK NUMBER 00011110
LOADED SUCCESSFULLY...!
CLOCK NUMBER 00101010
DATA WRITE REQUESTED SUCCESSFULLY...!
CLOCK NUMBER 00101011
DATA WRITE REQUESTED SUCCESSFULLY...!
CLOCK NUMBER 00110001
DATA WRITE REQUESTED SUCCESSFULLY...!
CLOCK NUMBER 00110111
DATA WRITE REQUESTED SUCCESSFULLY...!
CLOCK NUMBER 00111101
@echo: Victim is filled while leaving a line clean(Load Instruction).
MEMORY LINE:
         3586
    DATA:
```

VICTIM LINE: 0

TAG: 00000010000001

VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 1

TAG: 00000000000001

VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 2

TAG: 00011000000001

VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 3

TAG: 00000110000001

VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 4

TAG: 00011100000001

VALIDITY: 1

DIRTY: 0 NMRU: 00

VICTIM LINE: 5

TAG: 00000100000001

VALIDITY: 1

DIRTY: 1

NMRU: 01

VICTIM LINE: 6

TAG: 00010100000001

VALIDITY: 1

DIRTY: 1 NMRU: 10

VICTIM LINE: 7

TAG: 00010000000001

VALIDITY: 1

DIRTY: 1 NMRU: 11

WRITING ONE MORE DATA ON THE SAME LINE. DATA WRITE REQUESTED SUCCESSFULLY...!

CLOCK NUMBER 01001101

@echo: Controller will choose the dirty less line and Override it(Best option since

no need for a WRITE_BACK stage)

-----VIEWING THE VICTIM CONTENT-----

VICTIM LINE: 0

TAG: 00000010000001

VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 1

TAG: 00000000000001

VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 2

TAG: 00011000000001

 VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 3

TAG: 00000110000001

VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 4

TAG: 01111110000001

VALIDITY: 1

DIRTY: 1 NMRU: 11

VICTIM LINE: 5

TAG: 00000100000001

VALIDITY: 1

DIRTY: 1 NMRU: 00

VICTIM LINE: 6

TAG: 00010100000001

VALIDITY: 1

DIRTY: 1 NMRU: 01

VICTIM LINE: 7

TAG: 00010000000001

VALIDITY: 1

DIRTY: 1 NMRU: 10

------ VICTIM END ------