A 1.67 GHz 32-bit Pipelined Carry-Select Adder Using the Complementary Scheme

Youngjoon Kim, Ki-Hyuk Sung, and Lee-Sup Kim

Department of EECS, KAIST,
373-1 Kusong-dong, Yusong-gu, Taejon,
Korea

ABSTRACT

Using carry-select adder scheme, an adder with small number of stages can operate as fast as an adder with large number of stages. In this paper, a 4-block 5-stage 32-bit pipelined carry-select adder is designed and implemented. The proposed adder operates as fast as a conventional 16-stage 32-bit pipelined ripple-carry adder while number of registers required is nearly same as a conventional 4-stage pipelined adder. This adder is operated at 1.67 GHz clock frequency in a standard 0.25um CMOS technology with 2.5 V supply voltage.

1. INTRODUCTION

The objective for adders in some special purpose computing systems (e.g. some signal and image processing applications) is different from general-purpose applications. Since they operate on large stream of data and computations must be much faster to achieve high data rate, pipelining is needed to increase throughputs of the computational units and the clock rates [4-7].
In the conventional pipelined circuit, a potential speed up of *n* can be achieved when *n* pipeline stages are used. Thus, for a 32-bit adder, 32 or more stages would be the optimal solution for achieving the fastest operation. However, like any design, choosing architecture for a computation unit involves trade off among speed, size, and power consumption. Each pipeline stage requires insertion of registers and global clock lines. To increase one stage, more than *n* registers are required where *n* is the total number of bits. A 32-stage 32-bit pipelined adder requires more than a thousand registers. This excessively large number of registers result high power consumption, large area, and large latency. Thus, it is important to set number of stages such that the maximum performance can be achieved without too much power consumption and area overhead.
In this paper, a pipelined carry-select adder scheme is proposed to achieve a high operating frequency without adding a huge number of registers. A 4-block 4-stage 32-bit pipelined carry-select adder can operate as fast as a 16-stage 32-bit pipelined adder. Compare to near six hundred registers in a conventional 16-stage 32-bit adder, proposed 4-block 4-stage 32-bit pipelined carry-select adder requires only 276 registers with some additional circuits.
This paper is organized as follows. In section 2, we examine the conventional pipelined adder architecture. In section 3, we look at architecture of the proposed pipelined adder including the *carry-select adder scheme*. In section 4, analysis, SPICE simulation results, and comparisons are discussed. Finally, we finish this paper with conclusion.

2. CONVENIONAL ADDER ARCHITECTURE

As mentioned previously, increasing pipelined stages would cost too much area and power consumption. Therefore, eight or fewer stages are used in most 32-bit pipelined adders. Fig. 1 shows the conventional 4-stage 32-bit pipelined adder. An 8-bit ripple-carry adder (RCA) is inserted in each stage and carry out signal propagates into carry input of RCA in the next stage at the next cycle. The maximum clock frequency depends on speed of an 8-bit RCA and speed of a register. 148 registers and 32 full adders are used in this circuit.

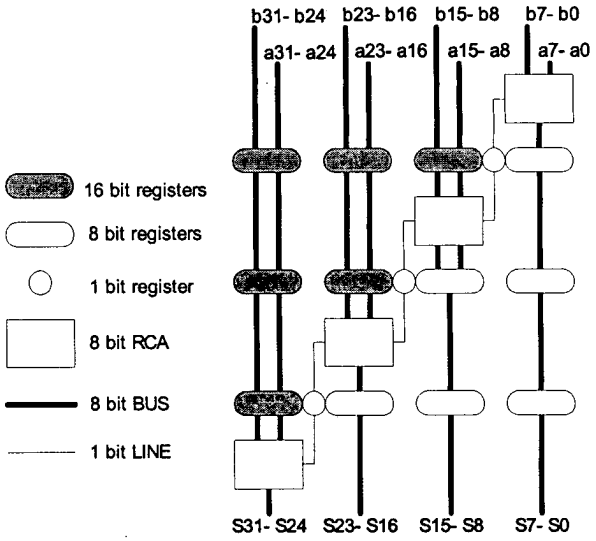

Figure 1. Conventional 4-stage 32-bit pipelined adder.

Designing a pipelined adder as shown in Fig. 2 reduces number of registers. Four independent 8-bit RCAs operate in parallel in the first stage. In the next stage, a 9-bit RCA or a 9-bit add-one circuit is required to add carryout from the first RCA to the sums and carryout from the second RCA. Then, the maximum clock frequency is same as the previous pipelined adder shown in Fig. 1. In this design, 102 pipeline registers, 32 full adders and three 9-bit add-one circuits are required. Therefore, near 15% fewer

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transistors are used to implement a 32-bit adder compare to the previous pipelined adder scheme.

Operating clock cycles of these two 4-stage pipeline adders are approximately eight times longer than clock cycle of a 32-stage pipelined adder which operating clock cycle involves delays of a full adder and a register.

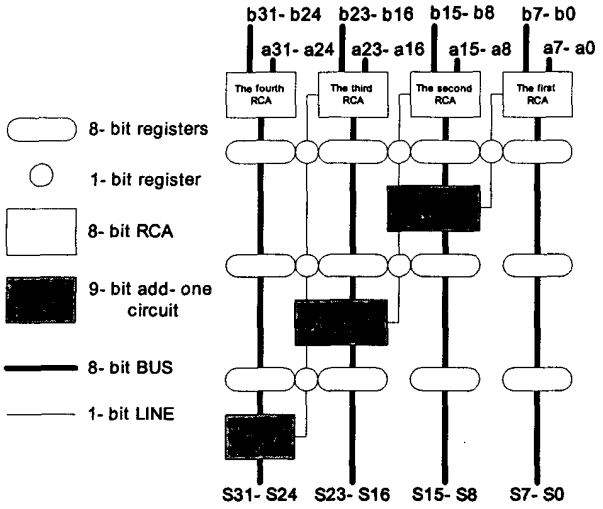

Figure 2. Conventional 4-stage 32-bit pipelined adder with reduced register scheme.

3. PROPOSED PIPELINE ADDER ARCHITECTURE USING CARRY-SELECT ADDER SCHEME

In order to increase clock frequency of the pipelined adder without adding a huge number of registers, a carry-select adder scheme using the complementary scheme is adapted. Before getting into the actual proposed adder architecture, the complementary scheme is discussed.

3.1 The single ripple carry carry-select adder

The carry-select adder scheme that we used in our pipelined adder architecture is based on the complement scheme. The complement scheme by Chang [1] was used for getting results of Cin = 1 from the results of Cin = 0. Assume (S^0_{n-1}, S^0_{n-2}, ..., S^0_0) and (S^1_{n-1}, S^1_{n-2}, ..., S^1_0) are the results of two RCAs with Cin=0 and Cin=1 respectively. Then, the complement scheme states that adding-one generates S^1_n bit by inverting each S^0_n bit starting from the least significant bit until the first zero is found. Two examples of the complementary scheme are shown in Fig. 3.

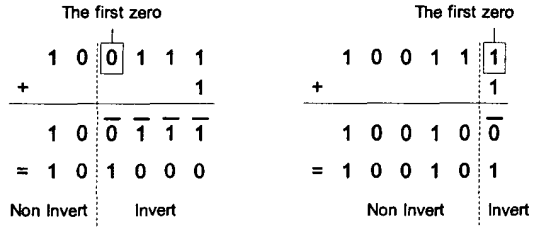

Figure 3. Two examples of the complement scheme.

This complement scheme can be implemented using multiplexers [2]. The multiplexer-based carry-select block is shown in the Fig. 4. Inverters are used to generate the complement of each sum and multiplexers are used to selects either S_k or complement of S_k according to the control signal where S_k is the sum at *kth* node. Control signal of the multiplexer is from the first zero finding circuit. The first zero finding circuit is the upper shaded area shown Fig. 4. The first zero finding circuit propagates GND up to the *kth* node if sums from the least significant bit are all one to the *kth* node. If the first zero is found at a *kth* sum, VDD will propagate from the *kth* node up to the most significant bit regardless of sum values after *kth* bits. Therefore, circuit shown in Fig. 4 generates sums for cin=1 from sums for cin=0 by adding one.

In the first zero finding circuit, a NMOS is used where only zero passes through. A PMOS is used where only VDD passes through. If both one and zero pass through, a transmission gate is used. In this way, Vt loss, which causes serious power loss due to the leakage current, can be avoided.

Carry out for a block can be chosen between carry out for the RCA and carry out for the add-one circuit. Carry out for the add-one circuit is one if and only if all sums from the RCA are equal to one.

Critical path for this circuit involves delays of a NMOS transistor, n-1 transmission gates, an inverter, and some buffers. In this circuit, total delay time is proportional to n.

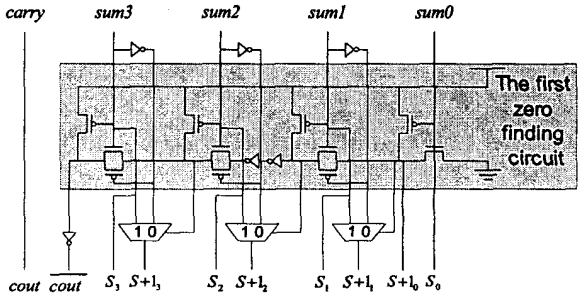

Figure 4. Circuit for generating add-one sums.

3.2 The proposed adder architecture

The proposed pipelined adder is shown in Fig. 5. Using the carry-select adder scheme introduced previously, the 32-bit pipelined adder can be constructed hierarchically by combining four smaller "block" adders that can be operated in parallel. Each block operates independently and is pipelined five stages. At the last stage, multiplexers were inserted to choose between sums for cin=0 and sums for cin=1 depending on carryin signal into the block.

Add-one circuit shown in Fig. 4 is inserted each block to generate results of C=1 from results of C=0. Since the worst-case delay for the add-one circuit is bigger than the 2-bit adder delay, we need to break down the circuit into the several sub circuits as shown in Fig. 6. Then, delay of the sub circuit is smaller than delay of the 2-bit RCA. Since the sub circuit and 2-bit RCA operated in parallel, delay of the sub circuit does not affect the operation frequency.

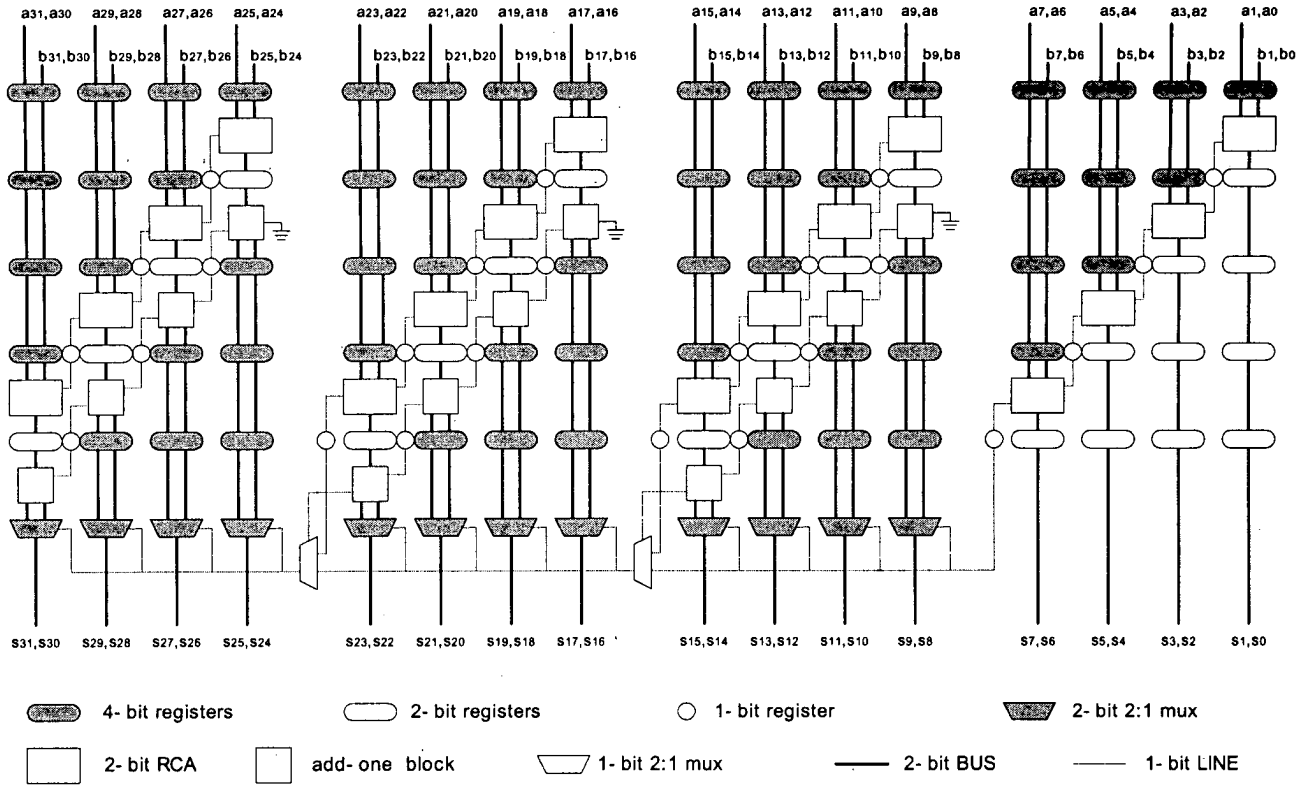

Figure 5. Proposed pipeline architecture.

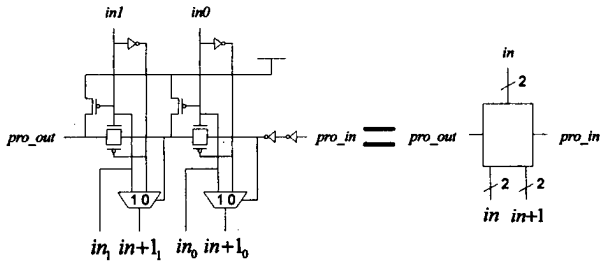

Figure 6. 2-bit add-one sum generation block.

Also, the delay time for the last stage does not affect the operational frequency since the delay is also smaller than the 2-bit RCA. Critical path for the last stage involves only three multiplexers. Therefore, the slowest combinational unit is 2-bit RCA. Compare with 8-bit RCA in the conventional 4-stage adder, the proposed carry-select pipelined adder can operate approximately 4 times faster. In other words, frequency of the proposed 5-stage pipelined adder is about same as the frequency of the conventional 16-stage pipelined adder. Nevertheless, the proposed adder requires only 276 registers.

Fig. 7 shows the D-flip-flop adapted in this proposed adder. This static D-flip-flop, mainly used in PowerPC 603, has a good performance on the power consumption and the speed [3]. This flipflop operates on negative edges.

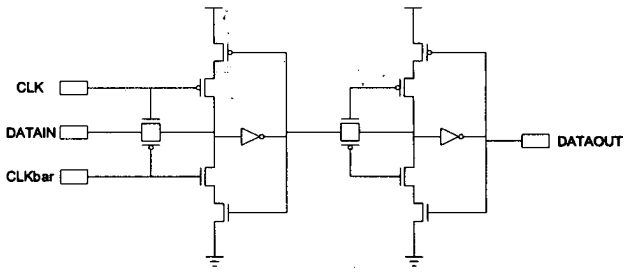

Figure 7. D-flip-flop used in the proposed adder.

For the full adder, the optimized area TG adder with 18 transistors is adapted [5]. This adder is stable and operates faster than other static CMOS full adders. More importantly, the delay times for the sum and the carryout are very close [4]. Since both carry and sum delays would affect the operating cycle time, it would be an appropriate choice.

4. Simulated Results and Comparison

Numbers of transistors required in the various stages and blocks of adders are analyzed. Number of transistors in the full adder and the D-flip-flop in this analysis are 18 and 16 respectively. Fig. 8 shows results of the analysis. As seen from Fig. 8, the number of transistors in the same-stage adders is just slightly increased as number of blocks increase. It does not depend much on the number of blocks. On the other hand, the number of

transistors becomes nearly doubled as the number of stages is doubled.

Fig. 9 shows the estimated operating delay time of various stages and blocks of adders. The estimation is based on the actual delay time of basic gates shown in Table 1. It shows the SPICE simulated delay time for each basic gate on our 0.25um CMOS technology with 2.5V supply voltage.

From Fig. 8 and Fig. 9, number of required registers does not change much when number of blocks increase, but operating frequency is nearly doubled when number of blocks is doubled. Therefore, constructing a pipelined adder by combining smaller blocks provides faster speed at fewer number of transistors.

Table 1. Simulated actual delay time and normalized delay of basic gates.

Basic gates	Delay
Inverter	0.08ns
NAND	0.13ns
Multiplexer(sel)	0.11ns
Multiplexer(thru)	0.05ns
XOR	0.11ns
D-flipflop	0.20ns
Sum(Full Adder)	0.21ns
Cout(Full Adder)	0.21ns

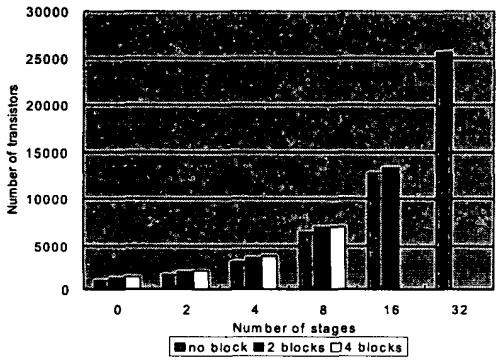

Figure 8. Number of transistors for different number of blocks and stages.

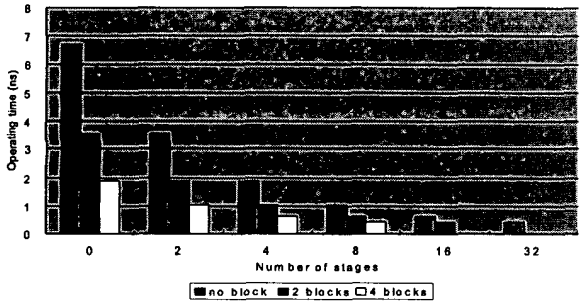

Figure 9. Adder operating delay time for different number of blocks and stages.

In this paper, we implemented 4-block 5-stage 32-bit adder in a 0.25um CMOS technology. Fig. 10 shows the HSPICE simulation of the proposed adder. We set b0-b31 to VDD and all other bits to zero. Then, we inserted two-rectagular signal at a24 and observe the sum bit at 24th node. As shown in Fig.10, the adder is operating properly at 1.67 GHz.

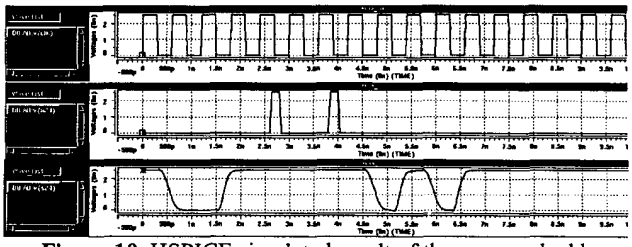

Figure 10. HSPICE simulated result of the proposed adder.

5. CONCLUSIONS

Using carry-select adder scheme, 5-stage pipelined adder can operate as fast as a conventional 16-stage pipelined adder. Compared to near six hundred registers for designing a conventional 16-stage pipelined adder, the proposed adder required only 276 registers to operate in the same frequency. Since it requires fewer registers, it results less area and less power. The proposed adder is operated at 1.67GHz with 2.5V power supply using a 0.25um CMOS technology.

6. ACKNOWLEDGMENT

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7. REFERENCES

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