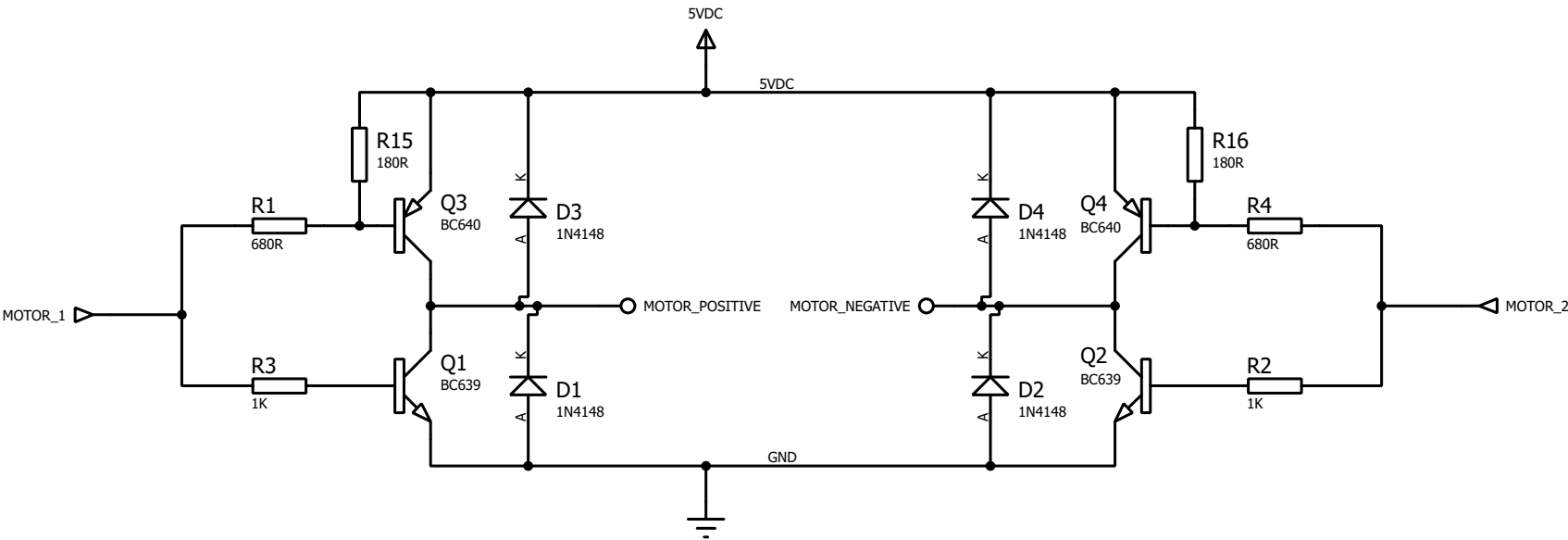
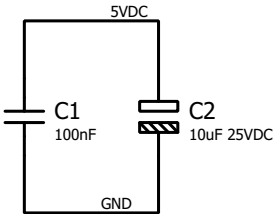




Title. FPGA DE0 LCD and H-Bridge	Document No. 1	Rev. No. 1v1	Sheet. 1/2
Sheet Title. Interconnect	Created. 20/11/2018@09:02:11	Modified. 27/11/2018@09:22:51	
Author. M. R. Simpson UOP	File. ELEC241_LCD_Motor_Inter_1_3.pds		

MOTOR_1	MOTOR_2	MOTOR
L	L	BRAKE
L	H	CLOCKWISE
H	L	ANTI-CLOCKWISE
H	H	BRAKE



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Title. FPGA DE0 LCD and H-Bridge	Document No. 1		Rev. No. 1v1	Sheet. 2/2
Sheet Title. H-Bridge	Created. 20/11/2018@09:02:11	Modified. 27/11/2018@09:22:51		
Author. M. R. Simpson UOP	File. ELEC241_LCD_Motor_Inter_1_3.pdsc			