UNIVERSITY OF INFOMATION TECHNOLOGY. **FINAL TEST – SEM. I (2023-2024)**

DEPARTMENT OF COMPUTER ENGINEERING

COMPUTER SYSTEM

DURATION: 90 minutes

*(Student are **not allowed** to use documents and resources.*

***The reference figure is shown in last page**.*

STUDENT NAME: ..... …….**STUDENT ID:**..... …….	
Score:	**Proctor Signature 1:**
	Proctor Signature 2:

PART 1. MULTIPLE CHOICE QUESTIONS (5 POINTS)

Answered Table ☑: selected ☒: unselected ●: reselected

	A	*B*	*C*	*D*
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				

	A	*B*	*C*	*D*
11.				
12.				
13.				
14.				
15.				
16.				
17.				
18.				
19.				
20.				

Note: Data Memory and Instruction Memory are separated memories for any questions which are related to Pipeline.

1. Given the following sequence of instructions (**For question 1, 2, 3**):

```
sub $t2,$t1,$t0
and $s2,$t2,$t5
or  $s3,$t6,$t2
add $s4,$t2,$t2
sw  $s4,100($t2)
```

If the pipeline is performed, which problem does occur?

A. data hazard B. structural hazard C. control hazard D. all of them

2. Assume there is no forwarding in this pipelined processor. How many cycles does the processor need to execute above sequence of instructions?

A. 9 B. 10 C. 11 D. 12

3. Assume there is full forwarding in this pipelined processor. How many cycles does the processor save to execute above sequence of instructions?

A. 1 B. 2 C. 3 D. 4

4. Which module is not used to execute the R-type instructions?

A. ALU B. Register file C. Instruction memory D. Data Memory

5. Which instruction is not used the signal RegWrite?

A. lw B. sw C. andi D. or

6. Which instruction does need the signal ALUSrc = 1 when it is executed?

A. addi B. beq C. or D. add

Given following sequence of instructions (**For question 7, 8**):

```
add $1, $5, $3
sw $1, 0($2)
lw $1,4($2)
add $5, $5, $1
sw $1, 0($2)
```

7. Assume there is no forwarding in this pipelined processor. How many NOP instructions are added to eliminate the hazards ?

A. 4 B. 5 C. 6 D. 7

8. Assume there is full forwarding in this pipelined processor. How many NOP instructions are added to eliminate the hazards ?

A. 1 B. 2 C. 3 D. 4

9. What are values of RegDst, ALUSrc, MemtoReg, RegWrite, MemRead, MemWrite signals when executing the R-type instructions:

A. 1,0,0,0,1,0 B. 1,0,1,0,1,0 C. 0,0,0,0,1,0 D. 0,0,1,0,1,0

10. What are values of RegWrite, MemRead, MemWrite, Branch, ALUOp1, ALUOp0 signals when executing the instructions: sw rt, offs(rs)

A. 1,0,1,0,0,0 B. 1,1,1,0,0,0 C. 0,0,0,0,0,0 D. 0,0,1,0,0,0

11. What are values of RegWrite, MemRead, MemWrite, Branch, ALUOp1, ALUOp0 signals when executing the instructions: beq rs, rt, BranchAdd

A. 0,0,0,0,0,1 B. 1,0,0,1,0,1 C. 0,0,0,1,0,1 D. x,0,x,1,0,1

Assume that each instruction needs 5 stages and the execution time of each stage is as below table (**For question 12, 13**)

IF	ID	EX	MEM	WB
350ps	300ps	300ps	600ps	150ps

12. How long is clock cycle if processor is pipeline and non-pipeline, respectively.
A. 600 and 1650 B. 150 and 1650 C. 600 and 1700 D. 300 and 1700

13. Give an instruction:
sw $s1, 32($s4)

How long does it take to execute this instruction if the processor is pipeline and non-pipeline?
A. 2400 and 1700 B. 2400 and 1550 C. 3000 and 1700 D. 3000 and 1550

14. Assume that instructions executed by the processor are broken down as follows:

ALU	beq	lw	sw
40%	30%	20%	10%

Assuming there are no stalls or hazards, what are the ultilization of the data memory (MEM) and write-register (WB)?

A. 30 and 60 B. 30 and 70 C. 50 and 50 D. 40 and 60

15. ……occurs when the pipeline makes wrong decisions on branch prediction, resulting in instructions entering the pipeline that must be discarded.
A. Structural hazard
B. Data hazard
C. Input hazard
D. Control hazard

16. What does the instruction "*jal 400*" execute?

A. $ra = PC + 4 và PC = 400
B. $ra = PC và PC = PC + 400
C. $ra = PC + 4 và PC = 1600
D. $ra = PC và PC = PC + 1600

17. Assume that the execution time of each stage is as below table (the execution time of blocks which is not shown in table is 0). Calculate the longest delay path to execute *'lw'*

I-Mem	Add	Mux	ALU	Regs	D-Mem	Control
400ps	100ps	30ps	120ps	200ps	350ps	100ps

A. 1260 B. 1530 C. 1560 D. 1360

18. Given a below program starting at the address 0x04000024:

```
        slt     $t2, $t0, $t1
        beq     $t2, $zero, ELSE
        add     $t2, $t2, $t0
        j       DONE
ELSE:   add     $t2, $t2, $t1
DONE:
```

where, $t0 = 0000 0000 0000 0000 0000 0000 1011 1111;
$t1 = 0000 0000 0000 0000 0000 0000 1100 0000;
What is the value of $t2 after this program is executed?

A. 0x00000000 B.0x00000001 C. 0x000000C1 D. 0x000000C0

19. What is the 2-complement number of -20 ?

A. 00010100 B. 11101011 C. 11101100 D. 11111100

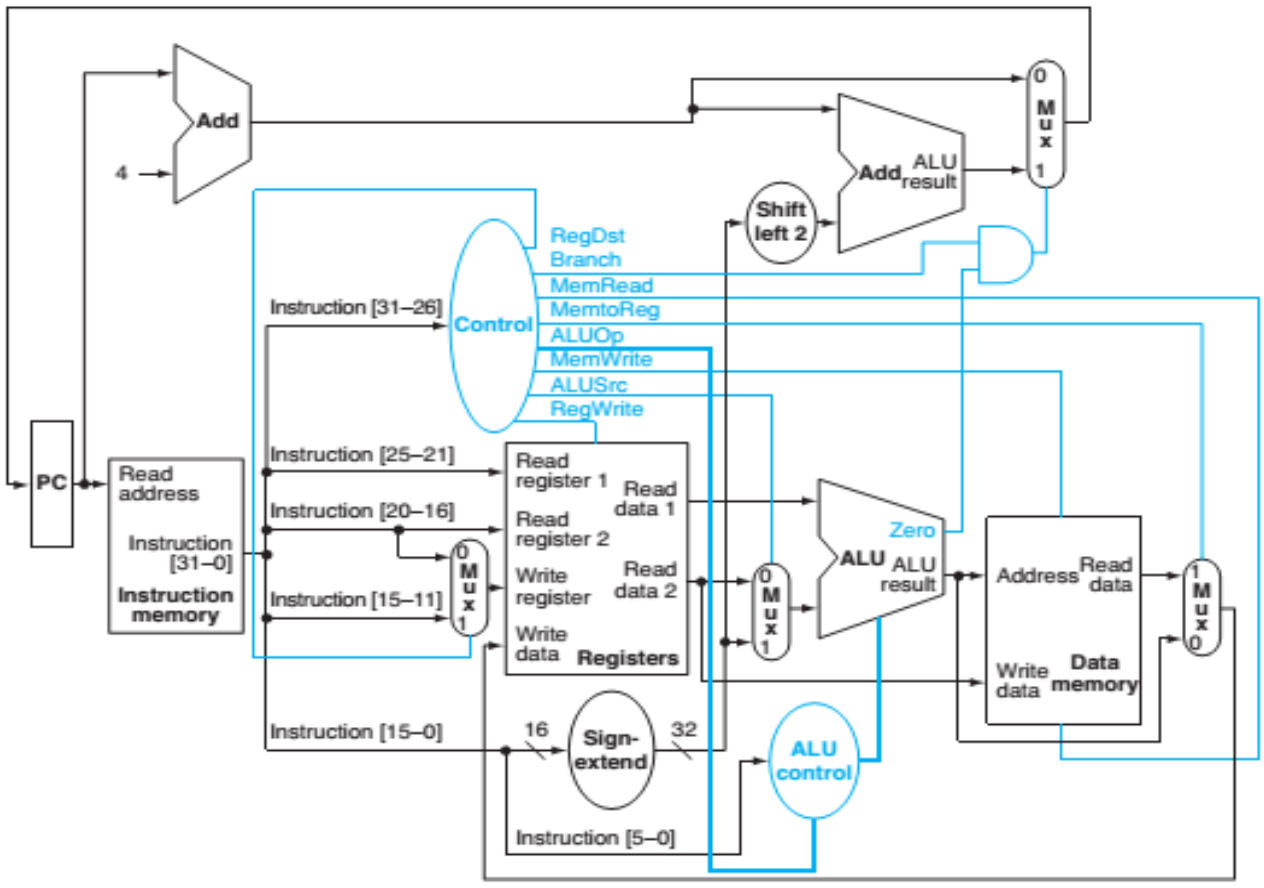
20. How many cycles does the pipeline MIPS processor take to execute one instruction?

A. 1 B. 4 C. 3 D. 5

==========**END**==========

Approved by Facl. Dean or Head of Dept **Designed by**

Lam Duc Khai



Reference Figure