AMBA AXI4Lite Protocol

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Key Features

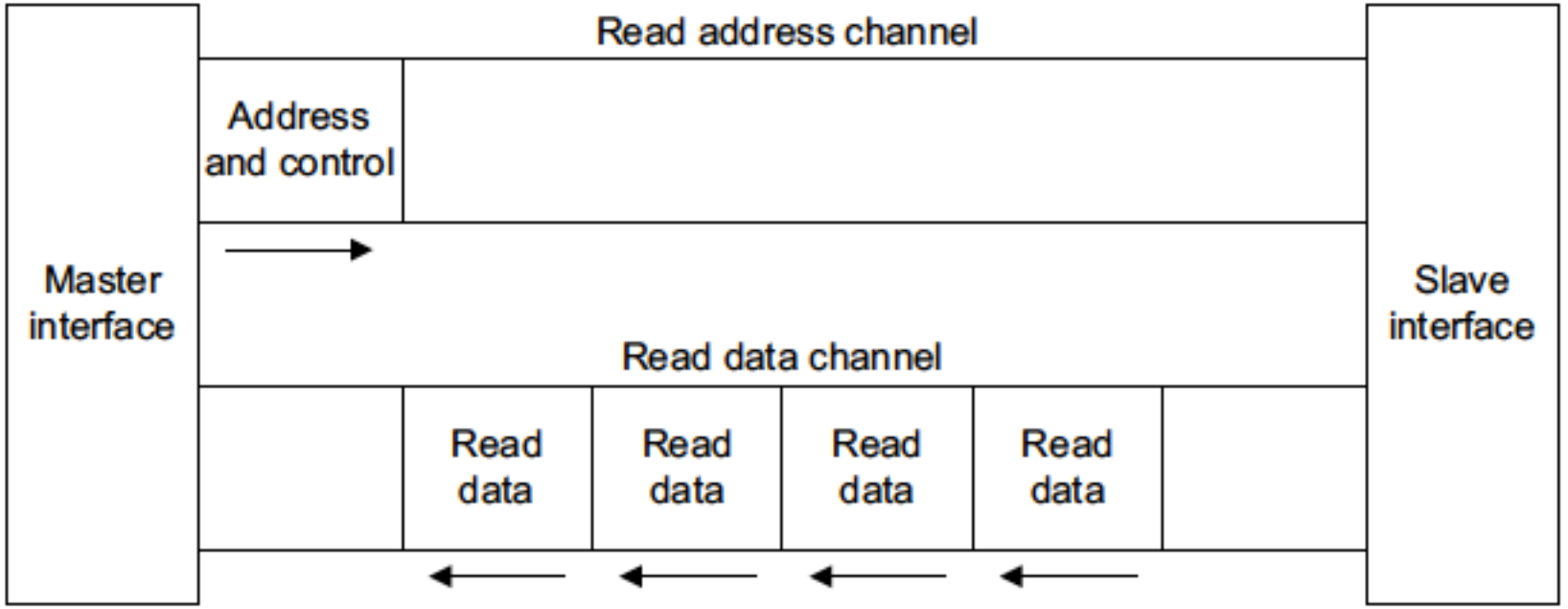
- separate address/control and data phases
- separate read and write data channels
- support for unaligned data transfers, using byte strobes
- permission to issue address information ahead of the actual data transfer

Architecture

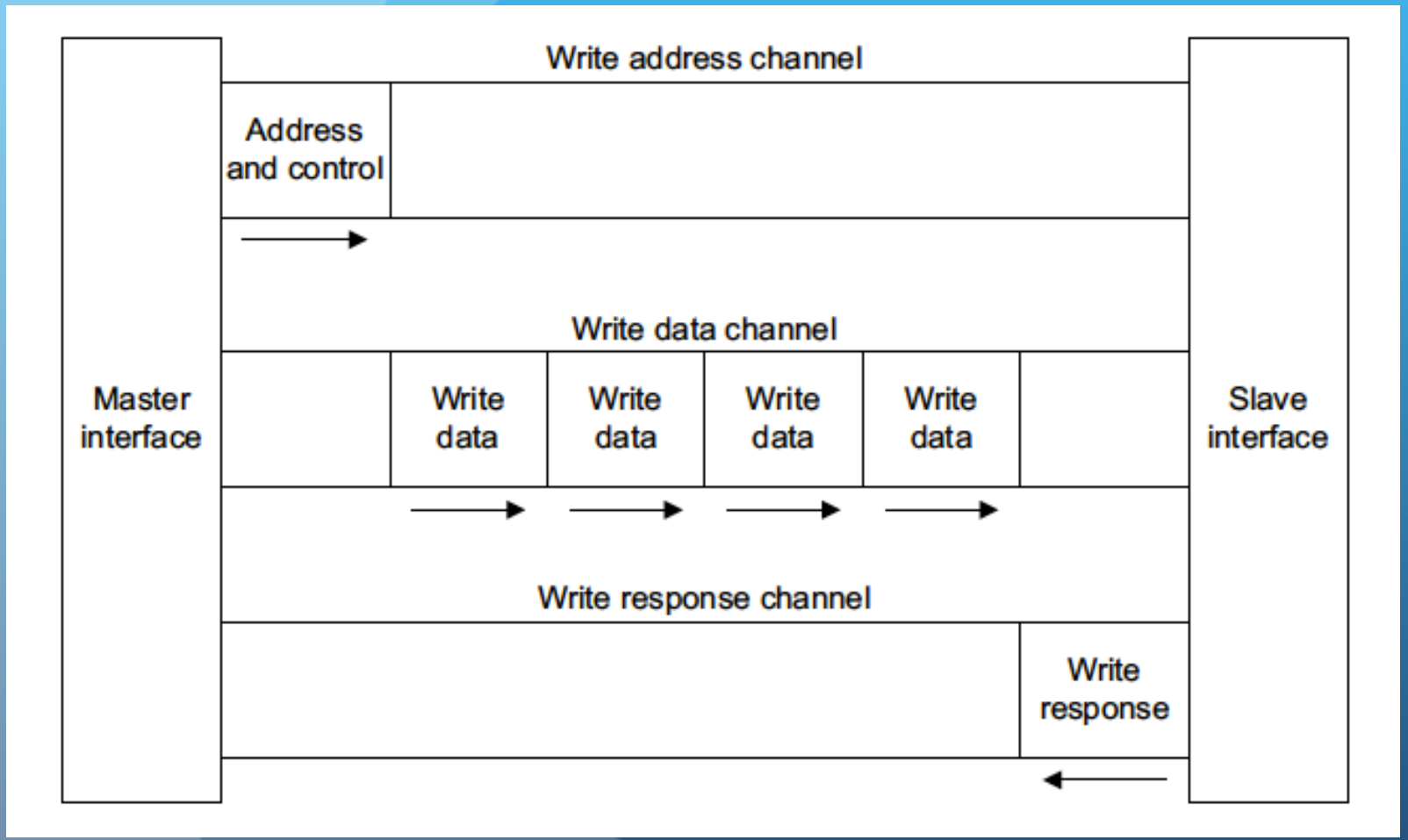
Five independent transaction channels:

- read address (Master -> Slave) “AR” prefix
- read data (Slave -> Master) “R” prefix
- write address (Master -> Slave) “AW” prefix
- write data (Master -> Slave) “W” prefix
- write response (Slave -> Master) “B” prefix

To Read…


Read address channel
Address and control
Master interface
Slave interface
Read data channel
Read data
Read data
Read data
Read data

To Write…


Write address channel
Address and control
Write data channel
Master interface
Write data
Write data
Write data
Write data
Slave interface
Write response channel
Write response

Two-way Handshake

Each of the five independent channels consists of:

- a set of information signals;
- VALID and READY signals.

The master uses the VALID signal to show when the information (address, data or control) is available and valid on the channel.

The slave uses the READY signal to show when it can accept the information.

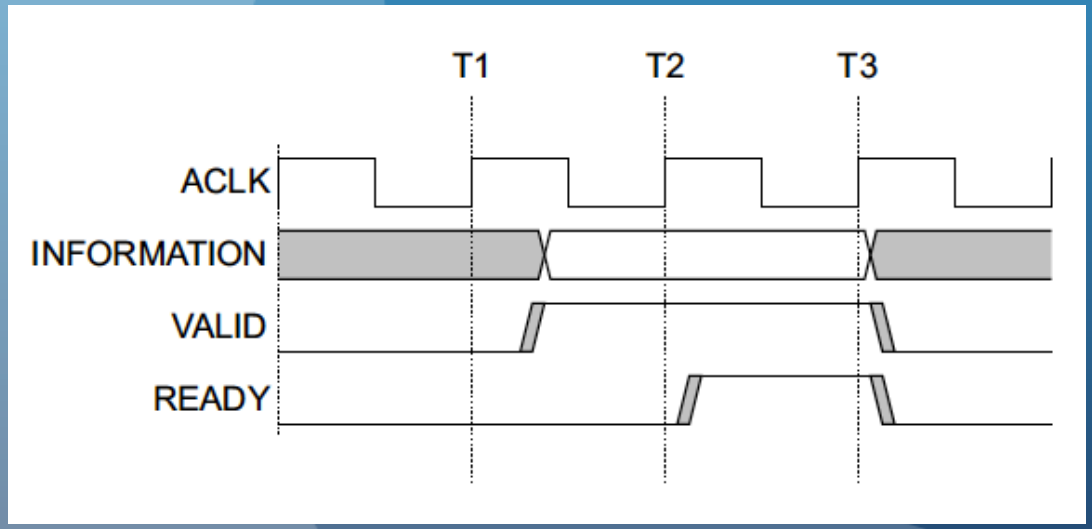
A transfer occurs only when both the VALID and READY signals are HIGH. (!!!)

Handshake Example #1

The source presents the address, data or control information after T1 and asserts the VALID signal.

The destination asserts the READY signal after T2.

Once VALID is asserted it must remain asserted until the handshake occurs, at a rising clock edge at which VALID and READY are both asserted.

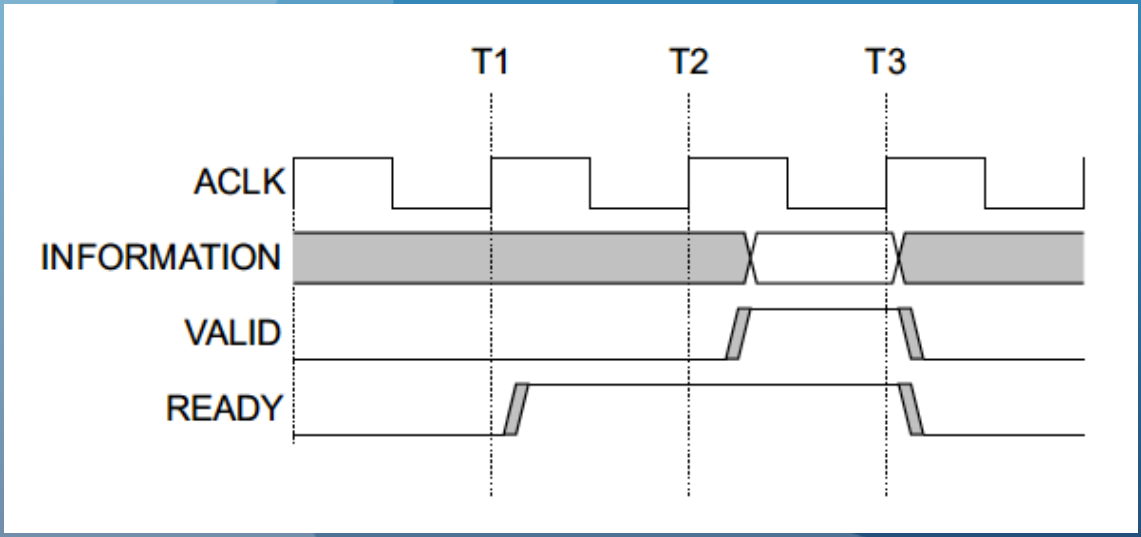


At what time does the transfer occur??

Handshake Example #2

The destination asserts READY, after T1, before the address, data or control information is valid, indicating that it can accept the information.

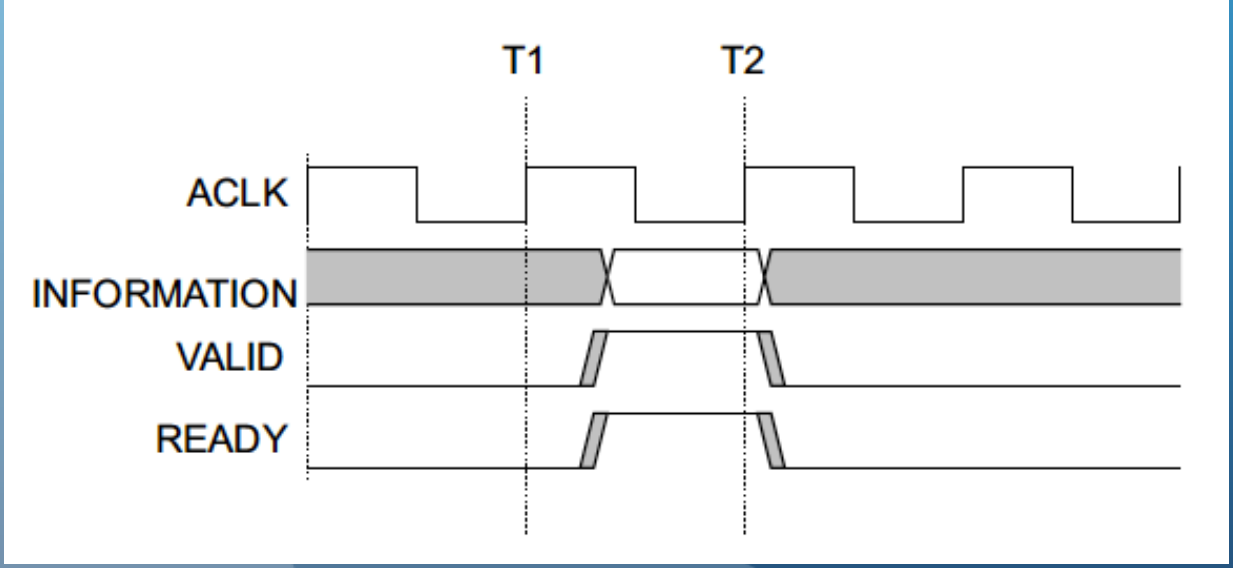
The source presents the information and asserts VALID, after T2.



At what time does the transfer occur??

Handshake Example #3

Both the source and destination happen to indicate, after T1, that they can transfer the address, data or control information.



At what time does the transfer occur??

Global Signals

- ACLK: global signal clock
- ARESETn: global reset signal, active LOW

Write Address Channel

- AWVALID : write address valid

This signal indicates that the channel is signaling valid write address and control information

- AWREADY : write address ready

This signal indicates that the slave is ready to accept an address and the associated control signals

- AWADDR[n-1:0] : write address
- AWPROT[2:0] : protection type

This signal indicates the privilege level of the transaction, and whether the transaction is a data access or an instruction access

Write Data Channel

- WVALID : write valid

This signal indicates that valid write data and strobes are available

- WREADY : write ready

This signal indicates that the slave can accept the write data

- WDATA[d-1:0] : write data

AXI4Lite supports a data bus width of 32-bit or 64-bit

- WSTRB[d/8-1:0] : write strobe

Write Strobe

There is one write strobe bit for each eight bits of the write data bus

Example:

Data bus: 64 bits

Write Strobe: 8 bits

The WSTRB signals, when HIGH, specify the bytes of the data bus that contain valid information

Example:

Write Strobe: 11000011

Valid data bus bytes: MSB, MSB-1, LSB+1, LSB

Write Response Channel

- BVALID : write response valid

This signal indicates that the channel is signaling a valid write response

- BREADY : response ready

This signal indicates that the master can accept a write response

- BRESP[1:0] : write response

Write Response

BRESP[1:0]	RESPONSE
0b00	OKAY: a normal access has been successful
0b01	EXOKAY: an exclusive access has been successful; the EXOKAY response is not supported in AXI4Lite
0b10	SLVERR: the access has reached the slave successfully, but the slave wishes to return an error condition to the originating master
0b11	DECERR: there is no slave at the transaction address

Read Address Channel

- ARVALID : read address valid

This signal indicates that the channel is signaling valid read address and control information

- ARREADY : read address ready

This signal indicates that the slave is ready to accept an address and associated control signals

- ARADDR[n-1:0] : read address
- ARPROT[2:0] : protection type

This signal indicates the privilege level of the transaction, and whether the transaction is a data access or an instruction access

Read Data Channel

- RVALID : read valid

This signal indicates that valid read data are available

- RREADY : read ready

This signal indicates that the slave can accept the read data and response information

- RDATA[d-1:0] : read data

AXI4Lite supports a data bus width of 32-bit or 64-bit

- RRESP[1:0] : read response