

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7W74F, TC7W74FU, TC7W74FK

D-TYPE FLIP FLOP WITH PRESET AND CLEAR

The TC7W74 is a high speed C²MOS D FLIP FLOP fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

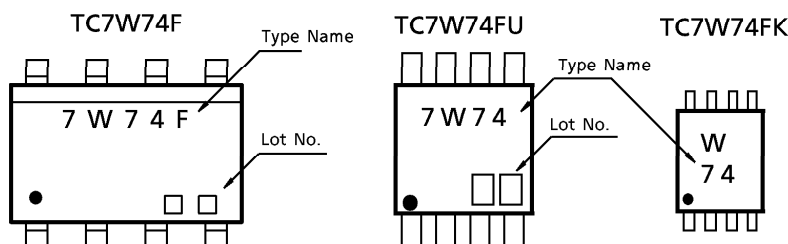
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse. CLEAR and PRESET are independent of the CLOCK and are accomplished by setting the appropriate input to an "L" level. Input is equipped with protection circuits against static discharge or transient excess voltage.

Weight SOP8-P-1.27 : 0.05g (Typ.)
SSOP8-P-0.65 : 0.02g (Typ.)

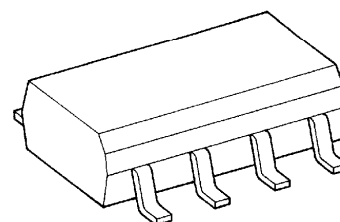
FEATURES

- High Speed $f_{MAX} = 77\text{MHz}$ (Typ.) at $V_{CC} = 5\text{V}$
- Low Power Dissipation $I_{CC} = 2\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL} = 4\text{mA}$ (Min.)
- Balanced Propagation Delays $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range ... $V_{CC}(\text{opr}) = 2 \sim 6\text{V}$

MARKING

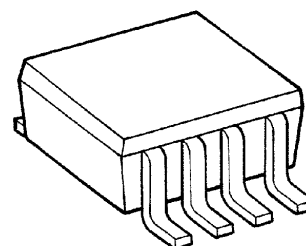


TC7W74F



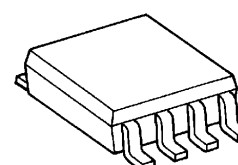
SOP8-P-1.27

TC7W74FU



SSOP8-P-0.65

TC7W74FK



SSOP8-P-0.50A

Weight
SOP8-P-1.27 : 0.05g (Typ.)
SSOP8-P-0.65 : 0.02g (Typ.)
SSOP8-P-0.50A : 0.01g (Typ.)

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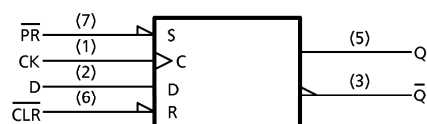
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● The information contained herein is subject to change without notice.

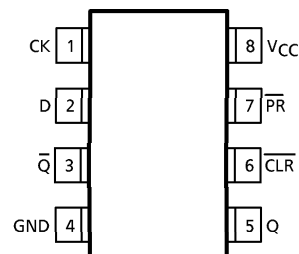
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V _{CC}	-0.5~7	V
DC Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} /Ground Current	I _{CC}	±25	mA
Power Dissipation	P _D	300	mW
Storage Temperature	T _{stg}	-65~150	°C
Lead Temperature (10s)	T _L	260	°C

LOGIC DIAGRAM



PIN ASSIGNMENT (TOP VIEW)



TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
CLR	PR	D	CK	Q	Q̄	
L	H	x	x	L	H	CLEAR
H	L	x	x	H	L	PRESET
L	L	x	x	H	H	—
H	H	L		L	H	—
H	H	H		H	L	—
H	H	x		Qn	Q̄n	NO CHANGE

x : Don't care

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	2~6	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	t _r , t _f	0~1000 (V _{CC} = 2.0V) 0~ 500 (V _{CC} = 4.5V) 0~ 400 (V _{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION		V _{CC}	Ta = 25°C			Ta = - 40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{IH}	—		2.0 4.5 6.0	1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	V
Low-Level Input Voltage	V _{IL}	—		2.0 4.5 6.0	— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
High-Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 20μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I _{OH} = - 4mA I _{OH} = - 5.2mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low-Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I _{OL} = 4mA I _{OL} = 5.2mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	—	—	±0.1	—	± 1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	2.0	—	20.0	μA

TIMING REQUIREMENTS (Input t_r = t_f = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC}	Ta = 25°C		Ta = - 40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	t _W (L) t _W (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLR, PR)	t _W (L)	—	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time	t _s	—	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time	t _h	—	2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time (CLR, PR)	t _{rem}	—	2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	4	5	
Clock Frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	—	—	6	12	ns
Propagation Delay Time (CLOCK-Q, Q)	t_{pLH} t_{pHL}	—	—	13	26	
Propagation Delay Time ($\overline{\text{CLR}}$, $\overline{\text{PR-Q}}$, Q)	t_{pLH} t_{pHL}	—	—	14	26	
Maximum Clock Frequency	f_{MAX}	—	36	77	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

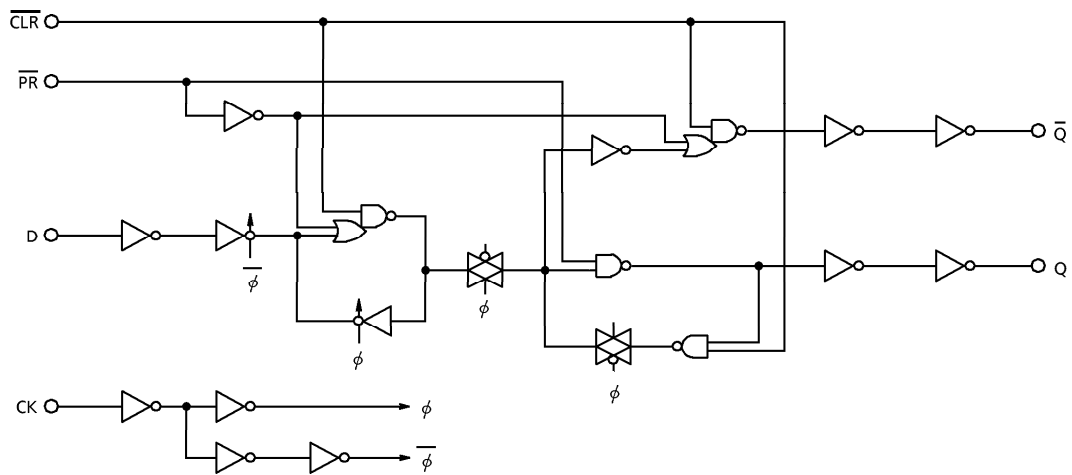
PARAMETER	SYMBOL	TEST CONDITION	V _{CC}	Ta = 25°C			Ta = −40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t _{TLH} t _{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (CLOCK-Q, $\overline{\text{Q}}$)	t _{pLH} t _{pHL}	—	2.0	—	48	150	—	190	
			4.5	—	16	30	—	38	
			6.0	—	13	26	—	32	
Propagation Delay Time ($\overline{\text{CLR}}$, $\overline{\text{PR-Q}}$, $\overline{\text{Q}}$)	t _{pLH} t _{pHL}	—	2.0	—	51	150	—	190	
			4.5	—	17	30	—	38	
			6.0	—	15	26	—	32	
Maximum Clock Frequency	f _{MAX}	—	2.0	6	21	—	5	—	MHz
			4.5	31	63	—	25	—	
			6.0	36	67	—	29	—	
Input Capacitance	C _{IN}	—		—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 1)		—	34	—	—	—	

Note 1 : C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation.

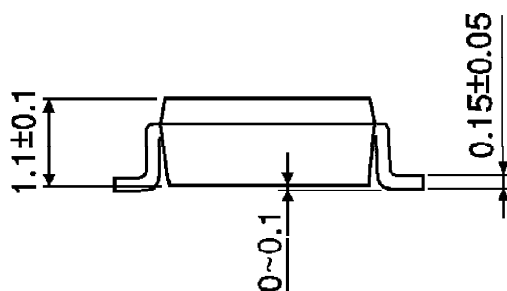
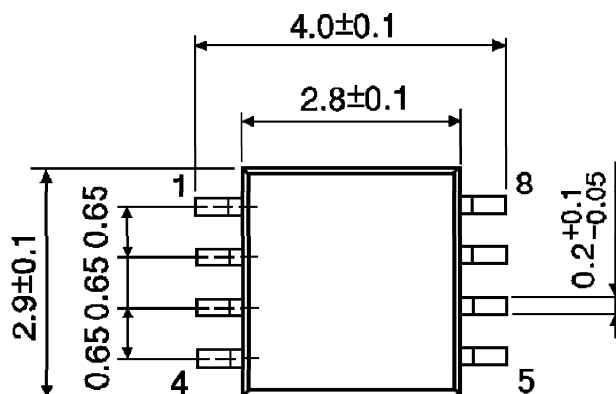
$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

SYSTEM DIAGRAM



OUTLINE DRAWING
SSOP8-P-0.65

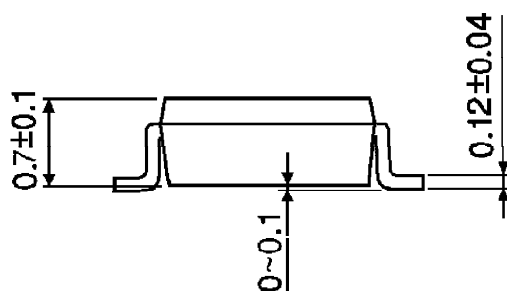
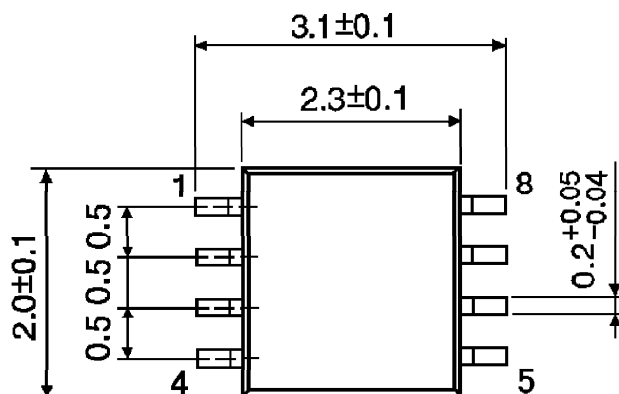
Unit : mm



Weight : 0.02g (Typ.)

OUTLINE DRAWING
SSOP8-P-0.50A

Unit : mm



Weight : 0.01g (Typ.)