

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

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- '90A, 'LS90 . . . Decade Counters
- '92A, 'LS92 . . . Divide By-Twelve Counters
- '93A, 'LS93 . . . 4-Bit Binary Counters

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'92A, '93A	130 mW
'LS90, 'LS92, 'LS93	45 mW

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

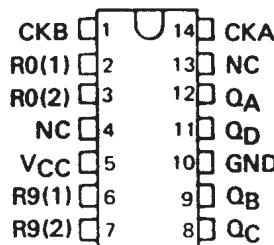
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the QA output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the QD output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output QA.

SN5490A, SN54LS90 . . . J OR W PACKAGE

SN7490A . . . N PACKAGE

SN74LS90 . . . D OR N PACKAGE

(TOP VIEW)

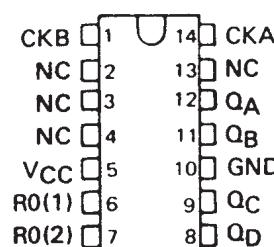


SN5492A, SN54LS92 . . . J OR W PACKAGE

SN7492A . . . N PACKAGE

SN74LS92 . . . D OR N PACKAGE

(TOP VIEW)

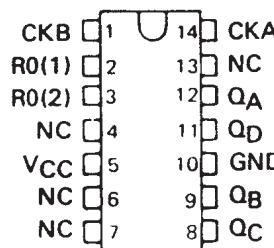


SN5493A, SN54LS93 . . . J OR W PACKAGE

SN7493 . . . N PACKAGE

SN74LS93 . . . D OR N PACKAGE

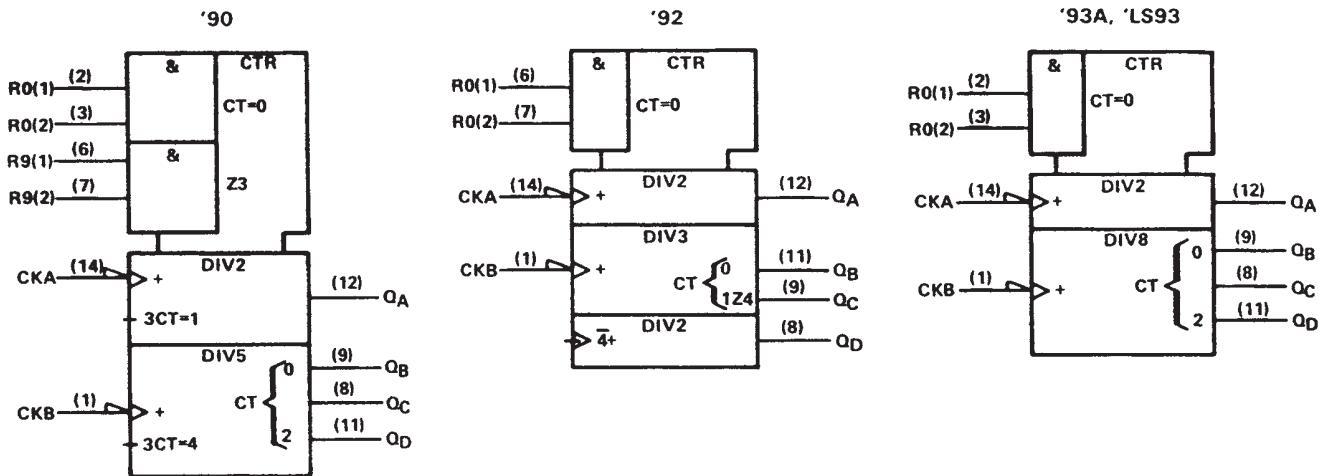
(TOP VIEW)



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
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logic symbols[†]



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

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'90A, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'90A, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT
R ₀₍₁₎	R ₀₍₂₎	R ₉₍₁₎	R ₉₍₂₎	Q _D Q _C Q _B Q _A
H	H	L	X	L L L L
H	H	X	L	L L L L
X	X	H	H	H L L H
X	L	X	L	COUNT
L	X	L	X	COUNT
L	X	X	L	COUNT
X	L	L	X	COUNT

'92A, 'LS92, '93A, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT
R ₀₍₁₎	R ₀₍₂₎	Q _D Q _C Q _B Q _A
H	H	L L L L
L	X	COUNT
X	L	COUNT

- NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.
C. Output Q_A is connected to input CKB.
D. H = high level, L = low level, X = irrelevant

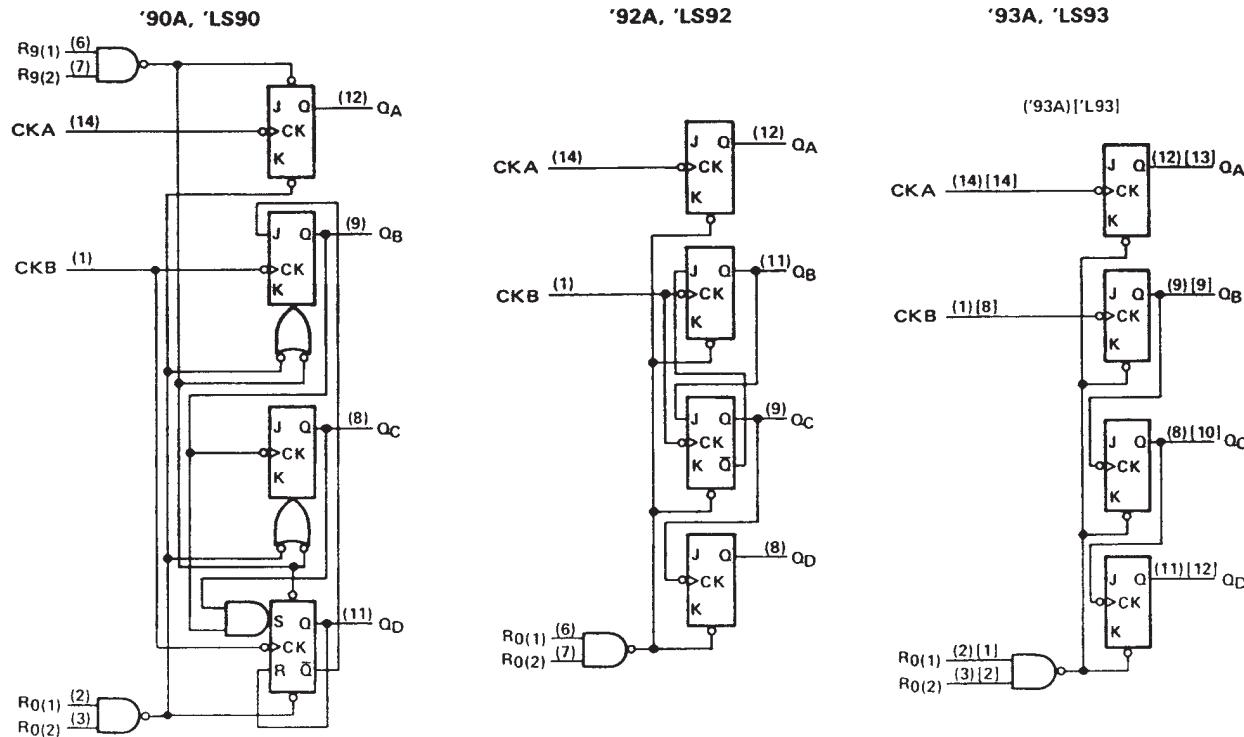
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
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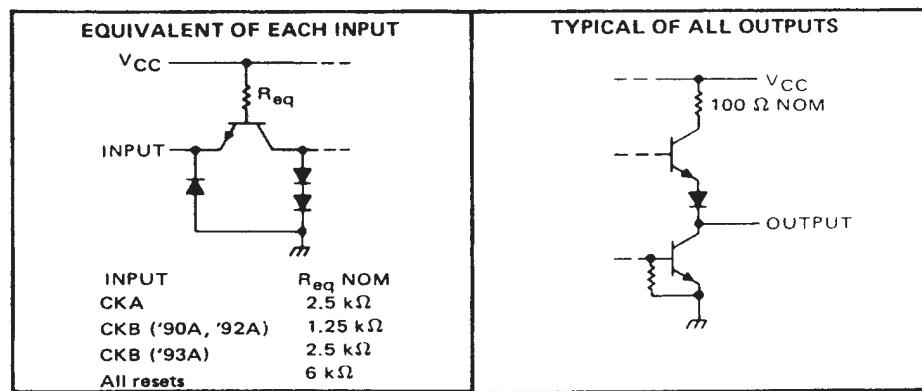
logic diagrams (positive logic)



The J and K inputs shown without connection are for reference only and are functionally at a high level.
Pin numbers shown in () are for the 'LS93 and '93A and pin numbers shown in [] are for the 54L93.

schematics of inputs and outputs

'90A, '92A, '93A

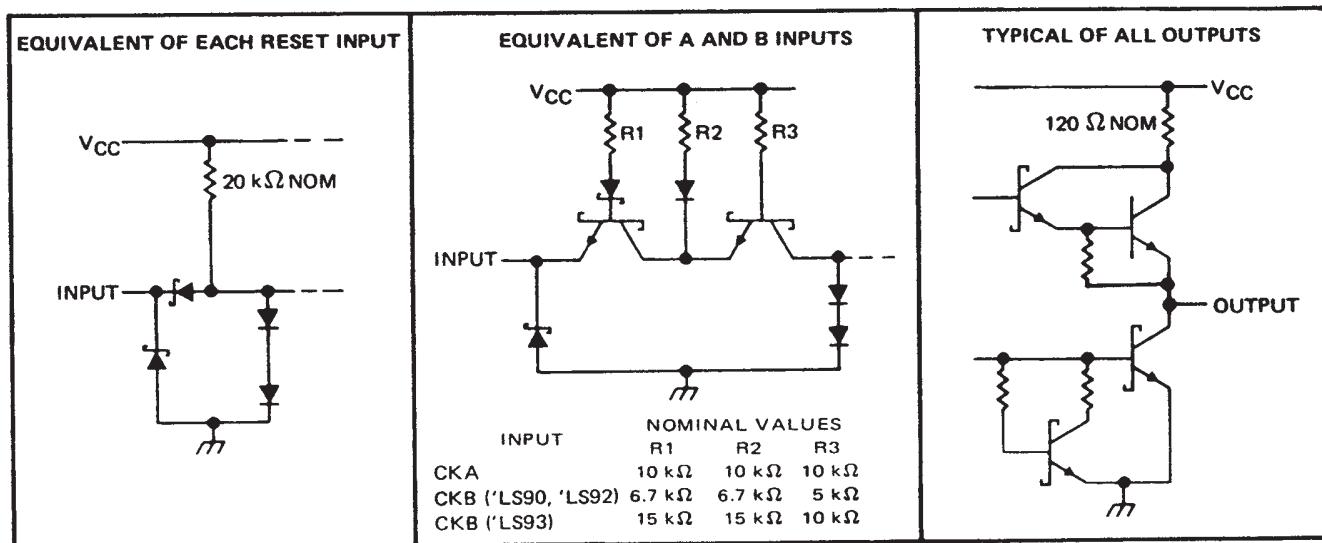


**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
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schematics of inputs and outputs (continued)

'LS90, 'LS92, 'LS93



SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to ground.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_O inputs, and for the '90A circuit, it also applies between the two R_g inputs.

recommended operating conditions

	SN5490A, SN5492A			SN7490A, SN7492A			UNIT	
	SN5493A			SN7493A				
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}			-800			-800	μA	
Low-level output current, I_{OL}			16			16	mA	
Count frequency, f_{count} (see Figure 1)	A input	0	32	0	32		MHz	
	B input	0	16	0	16			
Pulse width, t_W	A input	15		15			ns	
	B input	30		30				
	Reset inputs	15		15				
Reset inactive-state setup time, t_{SU}		25		25			ns	
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER ¹	TEST CONDITIONS [†]	'90A			'92A			'93A			UNIT	
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V _{IH} High-level input voltage		2			2			2			V	
V _{IL} Low-level input voltage		0.8			0.8			0.8			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA	-1.5			-1.5			-1.5			V	
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.4		2.4	3.4		2.4	3.4		V	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA [§]	0.2	0.4		0.2	0.4		0.2	0.4		V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1			1			1			mA	
I _{IH} High-level input current	Any reset	V _{CC} = MAX, V _I = 2.4 V			40			40			40	
	CKA				80			80			80	
	CKB				120			120			80	
I _{IIL} Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V			-1.6			-1.6			-1.6	
	CKA				-3.2			-3.2			-3.2	
	CKB				-4.8			-4.8			-3.2	
I _{OS} Short-circuit output current [§]	V _{CC} = MAX		SN54'	-20	-57	-20	-57	-20	-57	-20	mA	
			SN74'	-18	-57	-18	-57	-18	-57	-18	mA	
I _{CC} Supply current	V _{CC} = MAX, See Note 3			29	42		26	39		26	39	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[†]All typical values are at V_{CC} = 5 V, TA = 25°C.
[§]Not more than one output should be shorted at a time.

Q_A outputs are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



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switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CKA	Q _A	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q _B		16			16			16			
	t _{PLH}	CKA		10	16		10	16		10	16		ns
	t _{PHL}	CKA		12	18		12	18		12	18		
	t _{PLH}	CKA		32	48		32	48		46	70		ns
	t _{PHL}	CKA		34	50		34	50		46	70		
	t _{PLH}	CKB		10	16		10	16		10	16		ns
	t _{PHL}	CKB		14	21		14	21		14	21		
	t _{PLH}	CKB		21	32		10	16		21	32		ns
	t _{PHL}	CKB		23	35		14	21		23	35		
t_{PLH}	CKB	Q _D		21	32		21	32		34	51		ns
	t _{PHL}	CKB		23	35		23	35		34	51		
	t _{PLH}	Set-to-0	Any	26	40		26	40		26	40		ns
	t _{PHL}	Set-to-9	Q _A , Q _D	20	30								ns
t _{PHL}			Q _B , Q _C	26	40								ns

[†] f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output



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SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS' Circuits	-55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS90			SN74LS90			UNIT	
	SN54LS92			SN74LS92				
	SN54LS93			SN74LS93				
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}				-400			μA	
Low-level output current, I_{OL}				4			mA	
Count frequency, f_{count} (see Figure 1)	A input	0	32	0	32		MHz	
	B input	0	16	0	16			
Pulse width, t_W	A input	15		15			ns	
	B input	30		30				
	Reset inputs	30		30				
Reset inactive-state setup time, t_{SU}	25			25			ns	
Operating free-air temperature, T_A	-55	125	0	70			$^{\circ}C$	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS90			SN74LS90			UNIT	
		SN54LS92			SN74LS92				
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH} High-level input voltage				2	2			V	
V _{IL} Low-level input voltage				0.7	0.8			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5	-1.5			V	
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA			2.5 3.4	2.7 3.4			V	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max,			I _{OL} = 4 mA¶	0.25 0.4	0.25 0.4		V	
				I _{OL} = 8 mA¶	0.35 0.5			V	
I _I Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V			0.1	0.1			
	CKA	V _{CC} = MAX, V _I = 5.5 V			0.2	0.2			
	CKB				0.4	0.4			
I _{IIH} High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V			20	20			
	CKA				40	40			
	CKB				80	80			
I _{IIL} Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V			-0.4	-0.4			
	CKA				-2.4	-2.4			
	CKB				-3.2	-3.2			
I _{OS} Short-circuit output current§	V _{CC} = MAX			-20	-100	-20	-100	mA	
I _{ICC} Supply current	V _{CC} = MAX, See Note 3		'LS90	9 15	9 15			mA	
			'LS92	9 15	9 15				

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[#]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

8 Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS93			SN74LS93			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.7			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 μA	2.5	3.4		2.7	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA [§]	0.25	0.4	0.25	0.4		V
		I _{OL} = 8 mA [§]			0.35	0.5		
I _I Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA
	CKA or CKB	V _{CC} = MAX, V _I = 5.5 V			0.2		0.2	
I _{IH} High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V			20		20	μA
	CKA or CKB				40		80	
I _{IIL} Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA
	CKA				-2.4		-2.4	
	CKB				-1.6		-1.6	
I _{OS} Short-circuit output current [§]	V _{CC} = MAX		-20	-100	-20	-100		mA
I _{CC} Supply current	V _{CC} = MAX, See Note 3		9	15	9	15		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

[¶]Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IIL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER [#]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90			'LS92			'LS93			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
f _{max}	CKA	Q _A	C _L = 15 pF, R _L = 2 kΩ See Figure 1	32	42		32	42		32	42		MHz	
	CKB	Q _B		16			16			16				
	CKA	Q _A		10	16		10	16		10	16		ns	
				12	18		12	18		12	18			
	CKA	Q _D		32	48		32	48		46	70		ns	
				34	50		34	50		46	70			
	CKB	Q _B		10	16		10	16		10	16		ns	
				14	21		14	21		14	21			
	CKB	Q _C		21	32		10	16		21	32		ns	
				23	35		14	21		23	35			
t _{PLH}	CKB	Q _D		21	32		21	32		34	51		ns	
				23	35		23	35		34	51			
	Set-to-0	Any		26	40		26	40		26	40		ns	
		Q _A , Q _D		20	30								ns	
t _{PHL}	Set-to-9	Q _B , Q _C		26	40									

#f_{max} = maximum count frequency

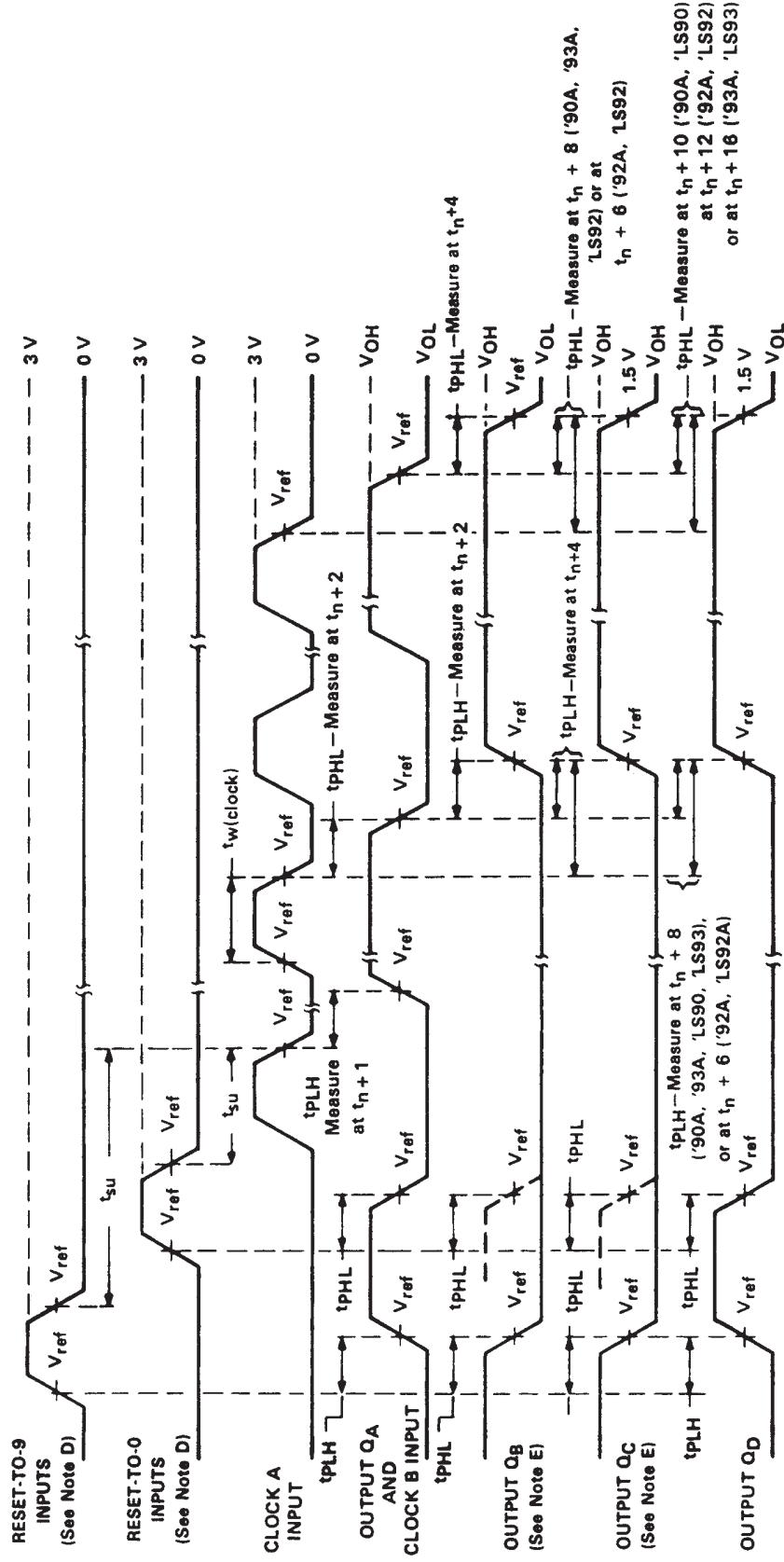
t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

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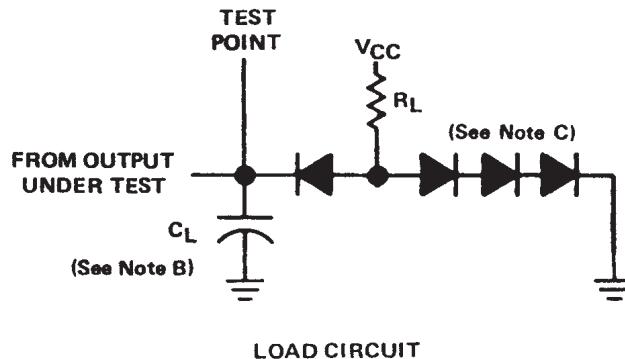
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by a generator having the following characteristics:
 for '90A, '92A, '93A, 'LS90, 'LS92, 'LS93, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
 for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.
 D. Each reset input is tested separately with the other reset at 4.5 V.
 E. Reference waveforms are shown with dashed lines.
 F. For '90A, '92A, and '93A; $V_{ref} = 1.5$ V. For 'LS90, 'LS92, and 'LS93; $V_{ref} = 1.3$ V.

FIGURE 1A

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. Input pulses are supplied by a generator having the following characteristics:
 for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
 for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are 1N3064 or equivalent.
 - D. Each reset input is tested separately with the other reset at 4.5 V.
 - E. Reference waveforms are shown with dashed lines.
 - F. For '90A, '92A, and '93A; $V_{ref} = 1.5$ V. For 'LS90, 'LS92, and 'LS93; $V_{ref} = 1.3$ V.

FIGURE 1B

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
7603201CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J
7700101CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101CA SNJ54LS93J
7700101DA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101DA SNJ54LS93W
JM38510/31501BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31501BCA
JM38510/31501BCA.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31501BCA
JM38510/31502BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31502BCA
JM38510/31502BCA.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31502BCA
JM38510/31502BDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31502BDA
JM38510/31502BDA.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31502BDA
M38510/31501BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31501BCA
M38510/31502BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31502BCA
M38510/31502BDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31502BDA
SN54LS90J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS90J
SN54LS90J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS90J
SN54LS93J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS93J
SN54LS93J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS93J
SN74LS90D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	LS90
SN74LS90DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90
SN74LS90DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90
SN74LS90N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS90N

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS90N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS90N
SN74LS90NE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS90N
SN74LS92D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS92
SN74LS92D.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS92
SN74LS92N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS92N
SN74LS92N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS92N
SN74LS92NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS92
SN74LS92NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS92
SN74LS93D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS93
SN74LS93D.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS93
SN74LS93N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS93N
SN74LS93N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS93N
SNJ54LS90J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J
SNJ54LS90J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J
SNJ54LS93J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101CA SNJ54LS93J
SNJ54LS93J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101CA SNJ54LS93J
SNJ54LS93W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101DA SNJ54LS93W
SNJ54LS93W.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101DA SNJ54LS93W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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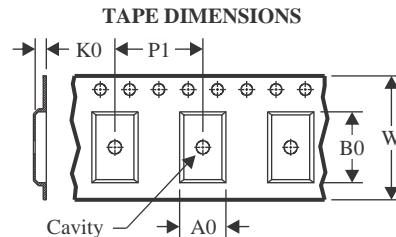
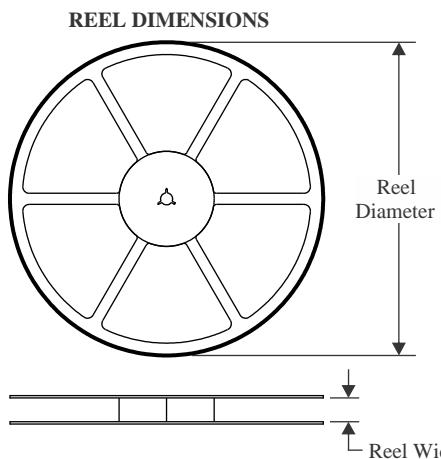
OTHER QUALIFIED VERSIONS OF SN54LS90, SN54LS93, SN74LS90, SN74LS93 :

- Catalog : [SN74LS90](#), [SN74LS93](#)
- Military : [SN54LS90](#), [SN54LS93](#)

NOTE: Qualified Version Definitions:

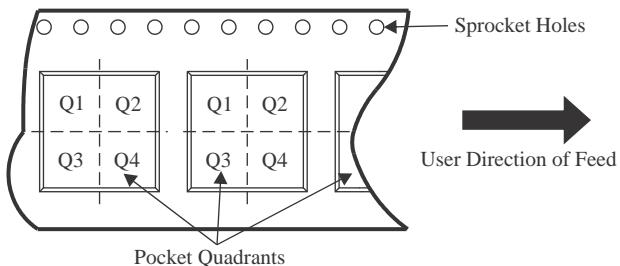
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



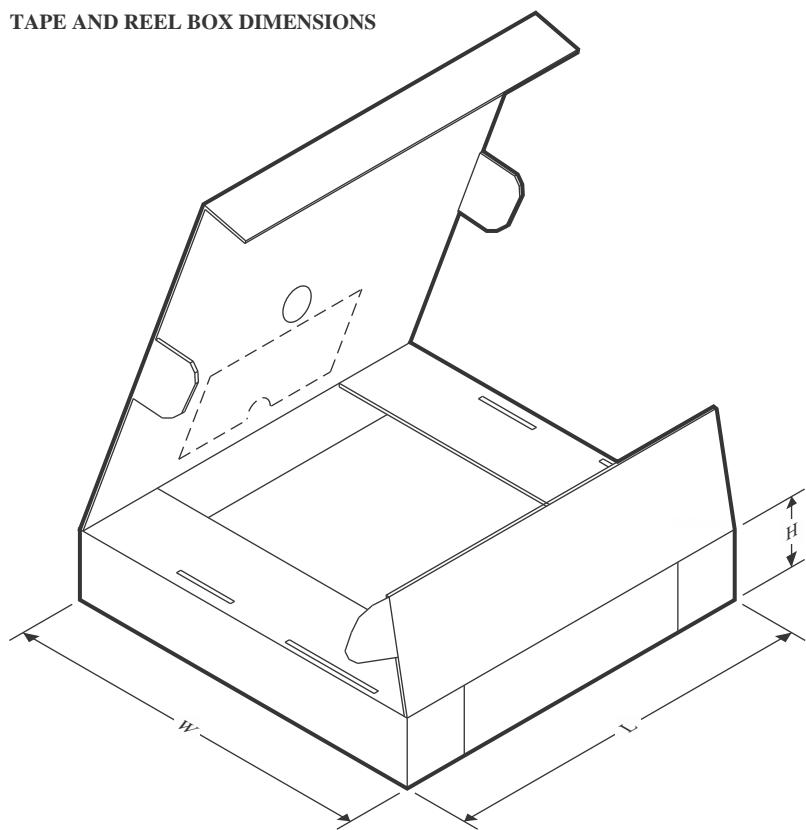
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

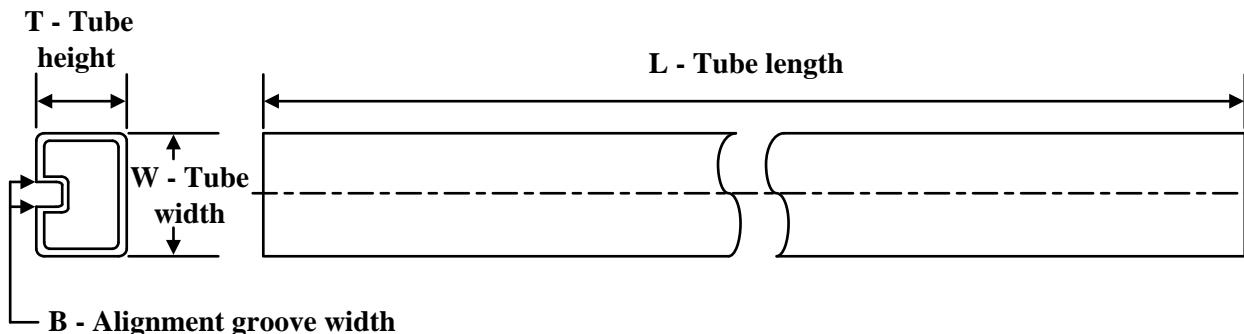
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS90DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS92NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS90DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LS92NSR	SOP	NS	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

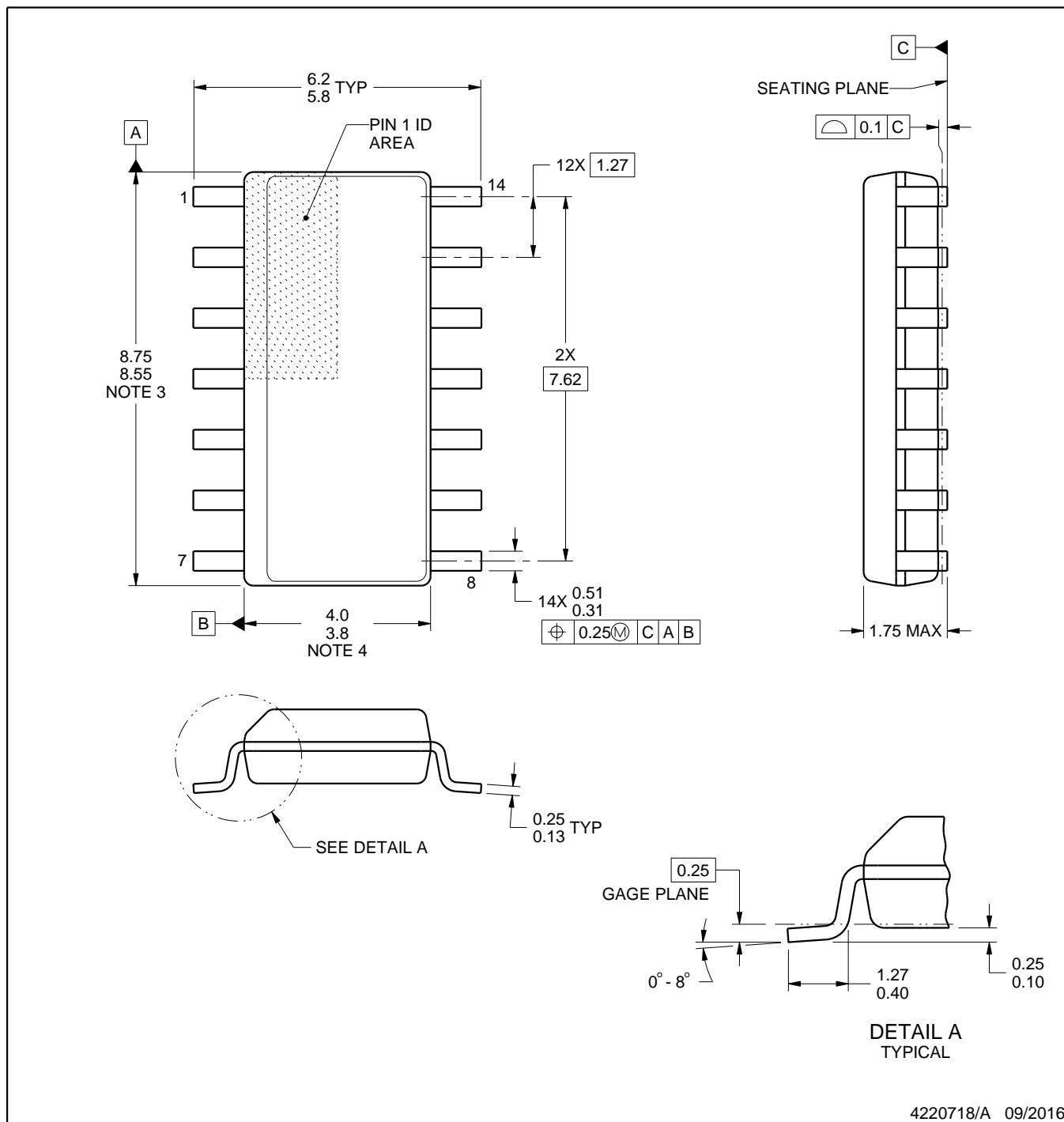
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
7700101DA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/31502BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/31502BDA.A	W	CFP	14	25	506.98	26.16	6220	NA
M38510/31502BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS90N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS92D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS92D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS92N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS92N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS92N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS92N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS93D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS93D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS93N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS93N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS93N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS93N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS93W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54LS93W.A	W	CFP	14	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

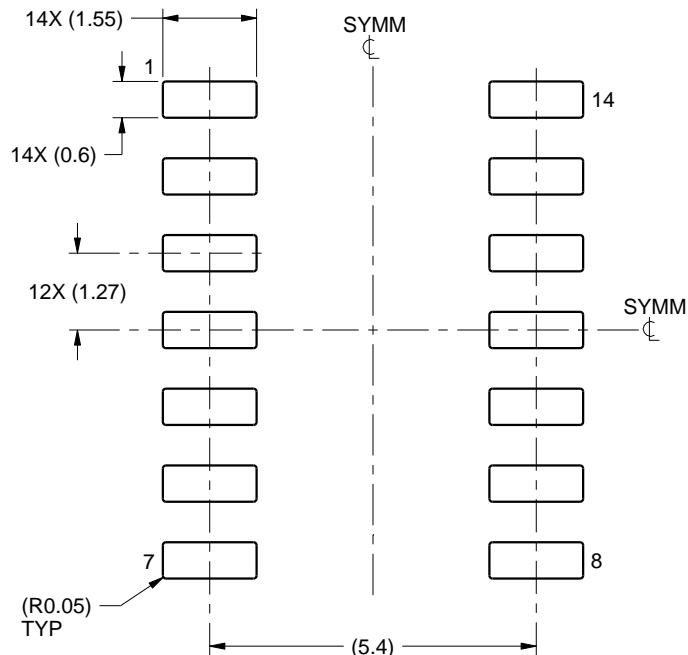
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

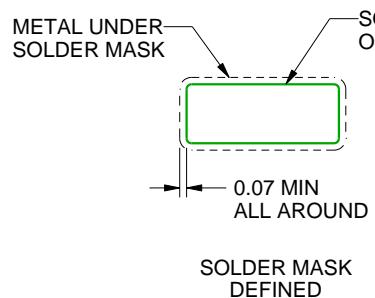
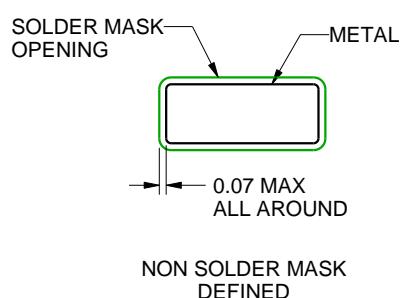
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

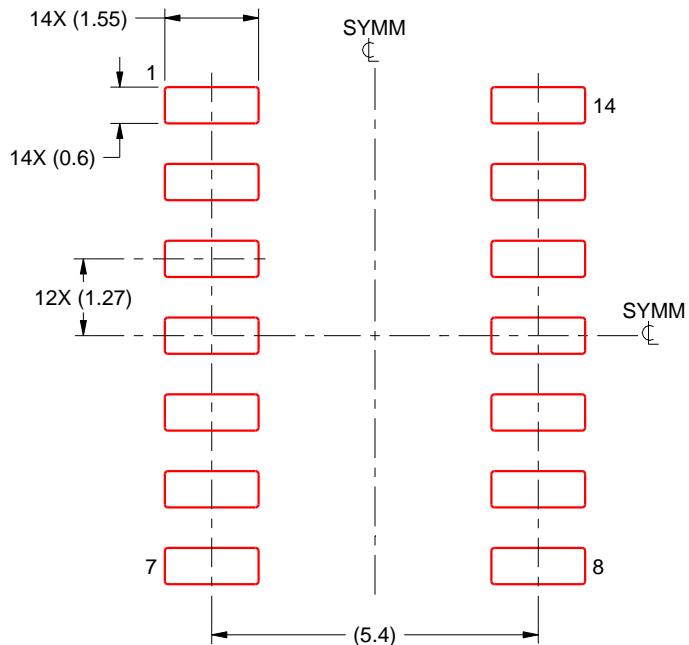
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

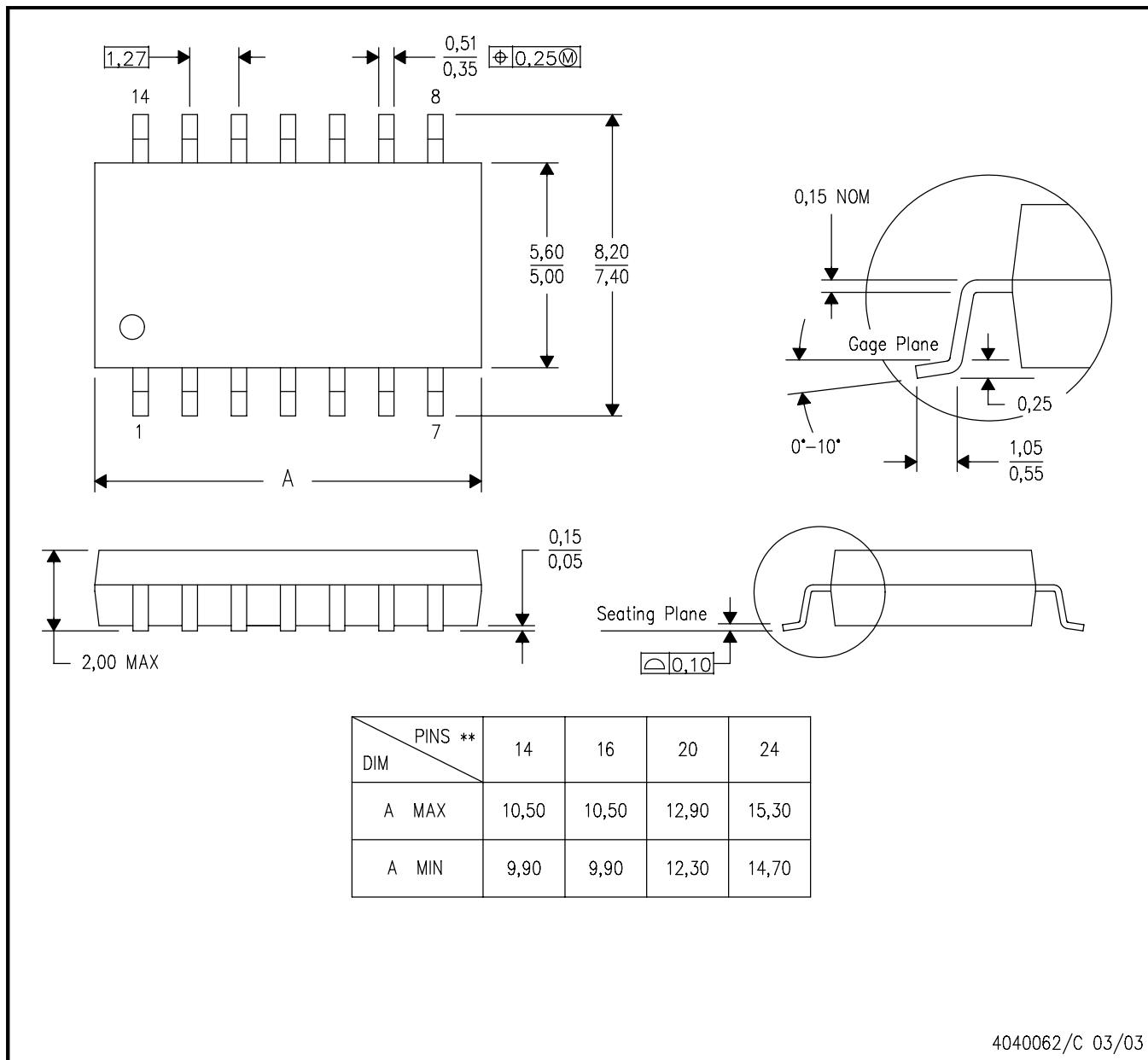
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

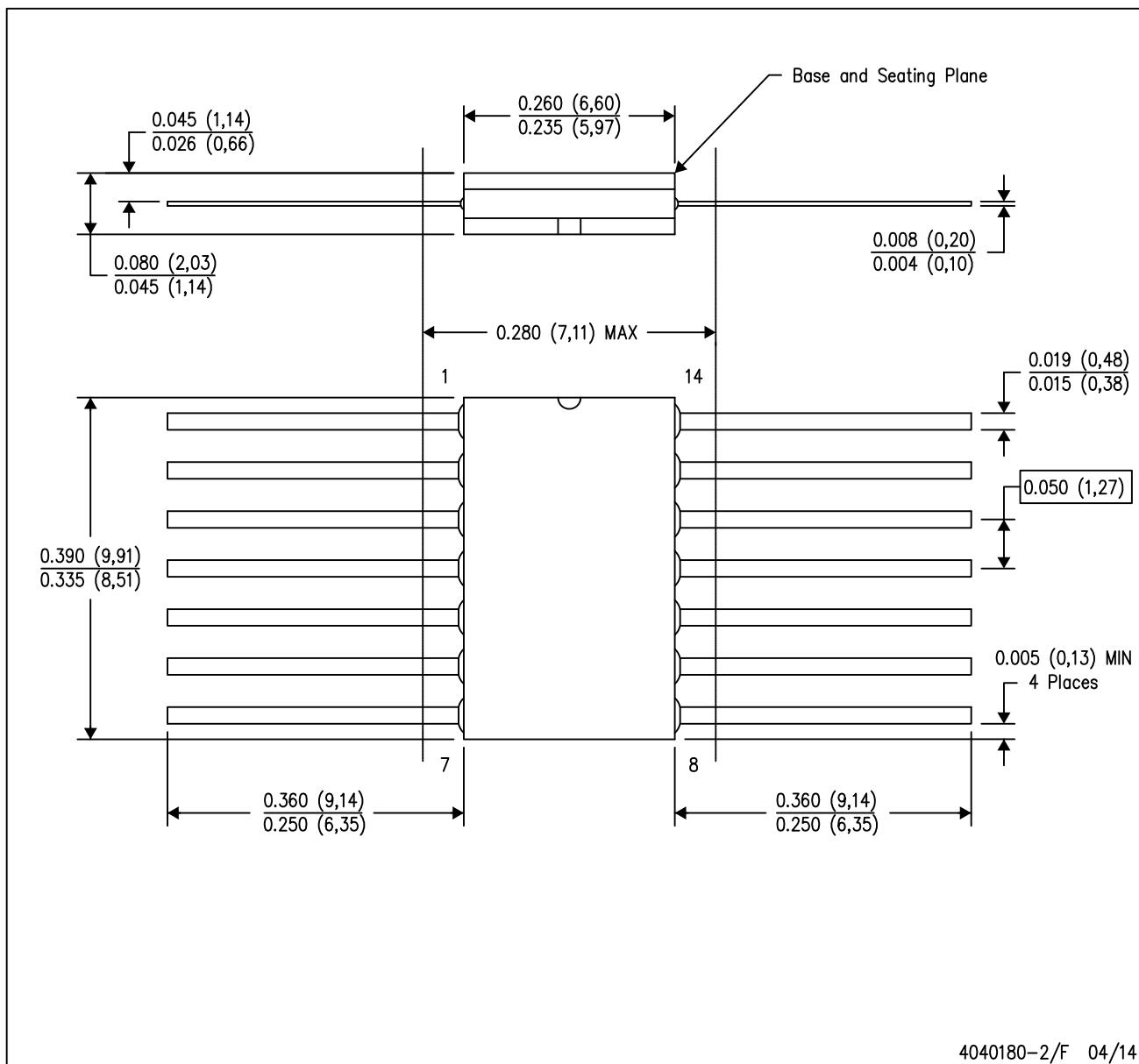


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



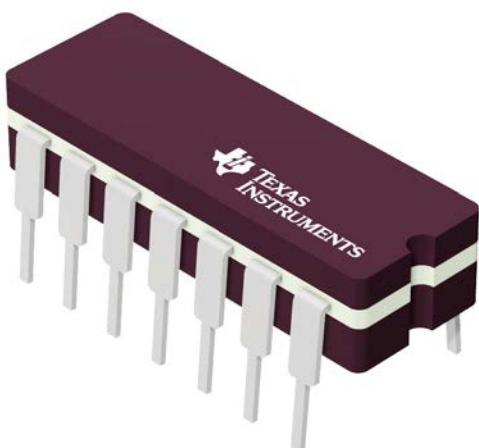
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

J 14

CDIP - 5.08 mm max height

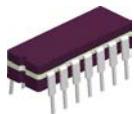
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

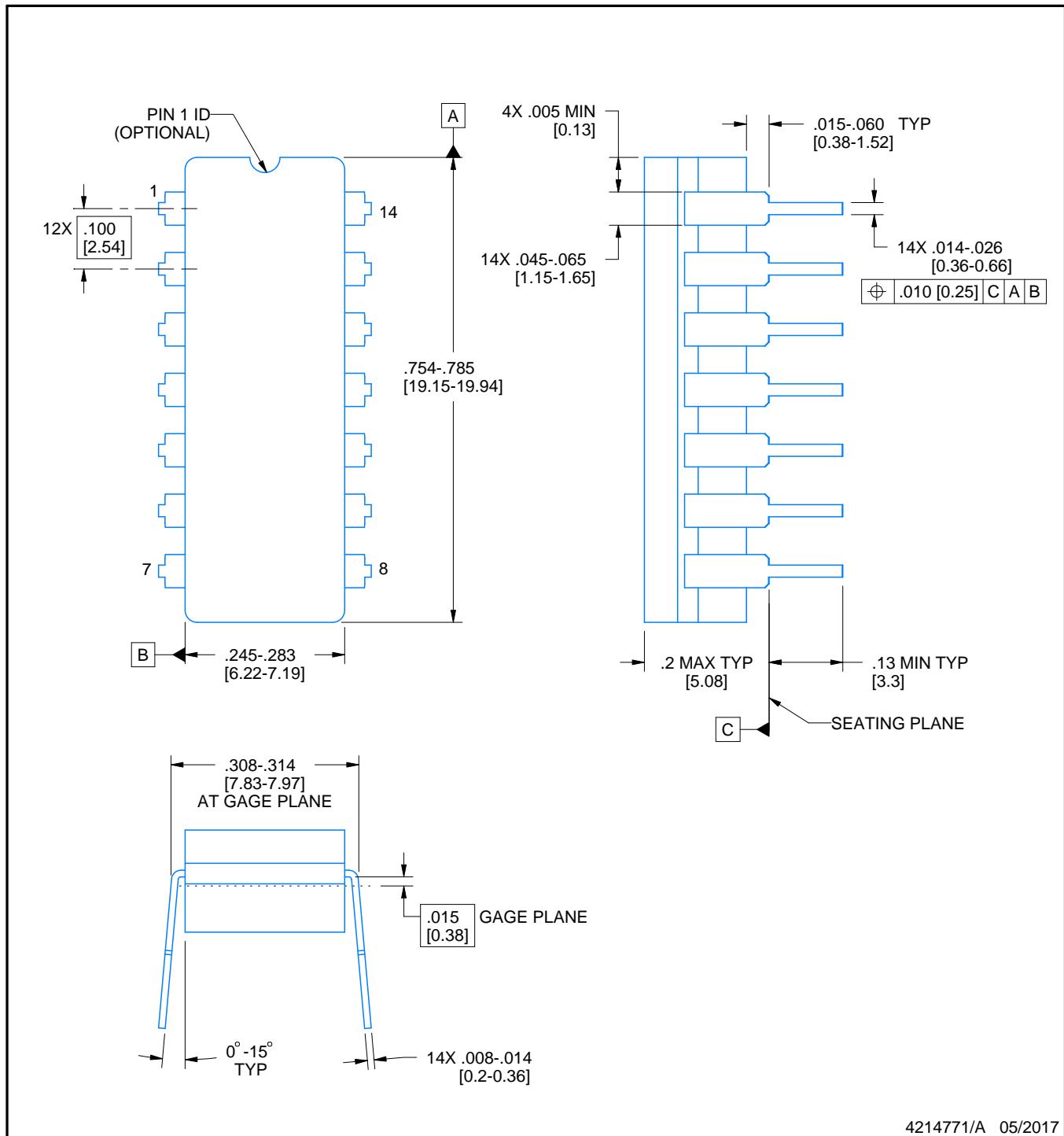
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

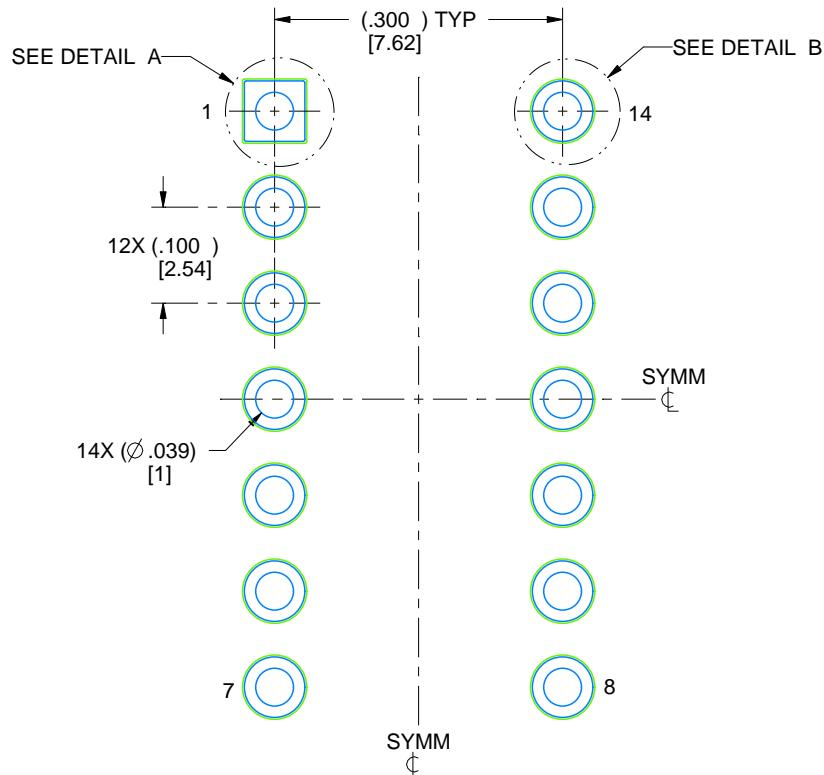
- All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This package is hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
- Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

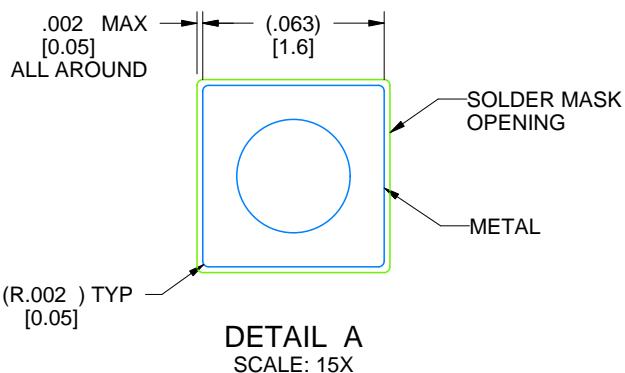
J0014A

CDIP - 5.08 mm max height

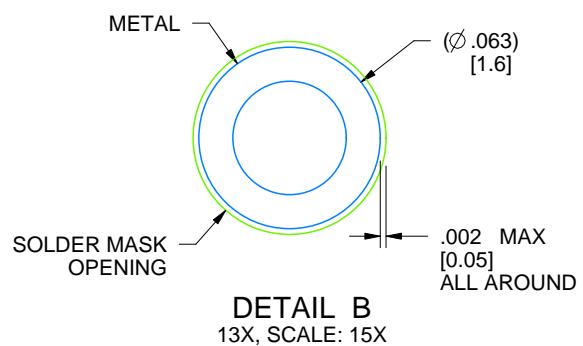
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



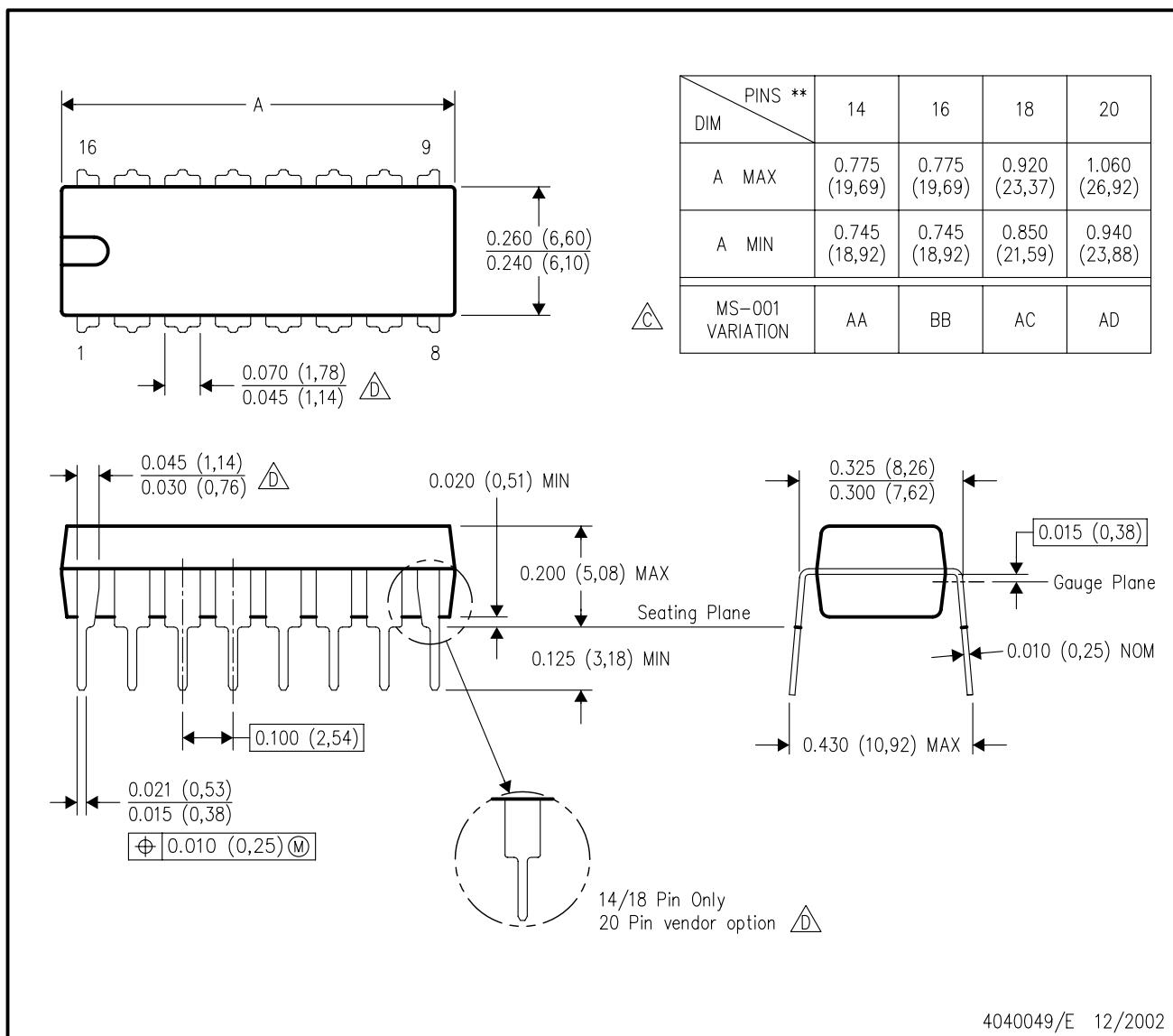
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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