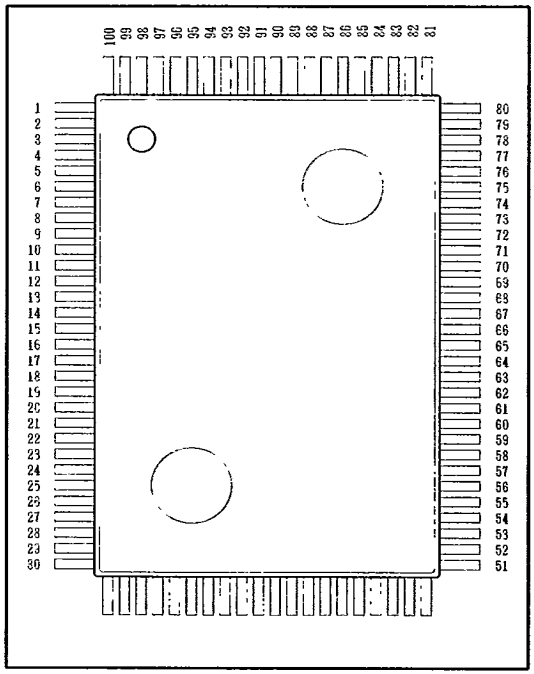
TC8566AF

Floppy Disk Controller

1. INTRODUCTION

TC8566AF is a single chip LSI for Floppy Disk controller which has VFO and other circuits with FDC chip for interfacing a processor to floppy disk drives.



2. FEATURES

- o Si-Gate CMOS technology
- o Single +5V power supply
- o 100 pin plastic flat package
- o Compatible FDC with TC8565AP
- o Built-in VCO and data separator circuit.
- o 16MHz oscillator inverter.
- o Standby function for battery operation
- o I/O address decoder include
- o Standard(500Kbps) and Mini(250Kbps) programable
- o FM,MFM recording formats (Specified by command)
- o Multi-sector data transfer
- o Up to four floppy disk drives
- o MOTOR ENABLE control for 4 drives
- o Direct interface to FDD with CMOS type interface system
- o Parallel seek operation up to four floppy disk drives
- o Programmable step rate time
- o Write pre-compensation circuit
- o Compatible with IBM track formats
- o Including CRC check function

$$(X^{16}+X^{12}+X^{5}+1)$$

- o DMA/Non DMA transfer

6

FLOPPY DISK CONTROLLER

The TC8566AF is an improvement on the TC8566F. The differences between them are as follows.

o VFO Part

66F : 2 filter switching type.
66AF : 2 filter switching type or 1 filter non-switching type, selectively.

o Address Decoder

66F : Address F0,F1 (Hex) is inhibit.
66AF : Address F0,F1 (Hex) is no selection.

o DMA Terminal Count

66F : DMATC signal is independent of ENID bit.
66AF : DMATC signal is enabled when ENID bit is "1".

o Step Rate Select

66F : Step Rate Time is selected by 2ms for mini-floppy mode (internal FDC Clock is 4MHz).
66AF : There is an option for mini-floppy mode that the FDC allows the internal Clock to be 8MHz at seek mode. Then step rate time is programable by 1ms like standard floppy mode.

o Reset State

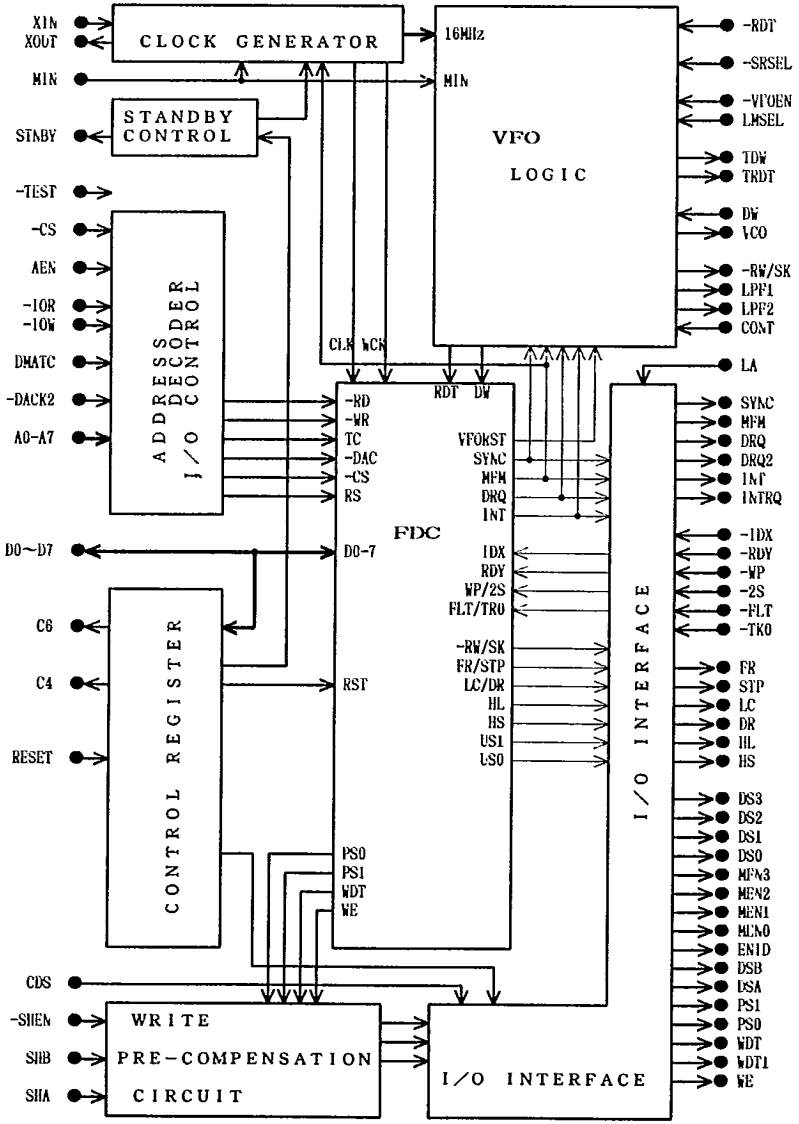
66AF : Drive Output Signals, WE, HL, HS, FR, STP, LC and DR become inactive when the external RESET signal is on a high level.

o Relation between Drive Select Signals and Motor Enable Signals

66F : Drive Select Signals are independent of Motor Enable Signals.
66AF : When drive select bits of the control register is used (CDS signal is on a high level), each Drive Select Signal is enabled by the corresponding Motor Enable Signal.

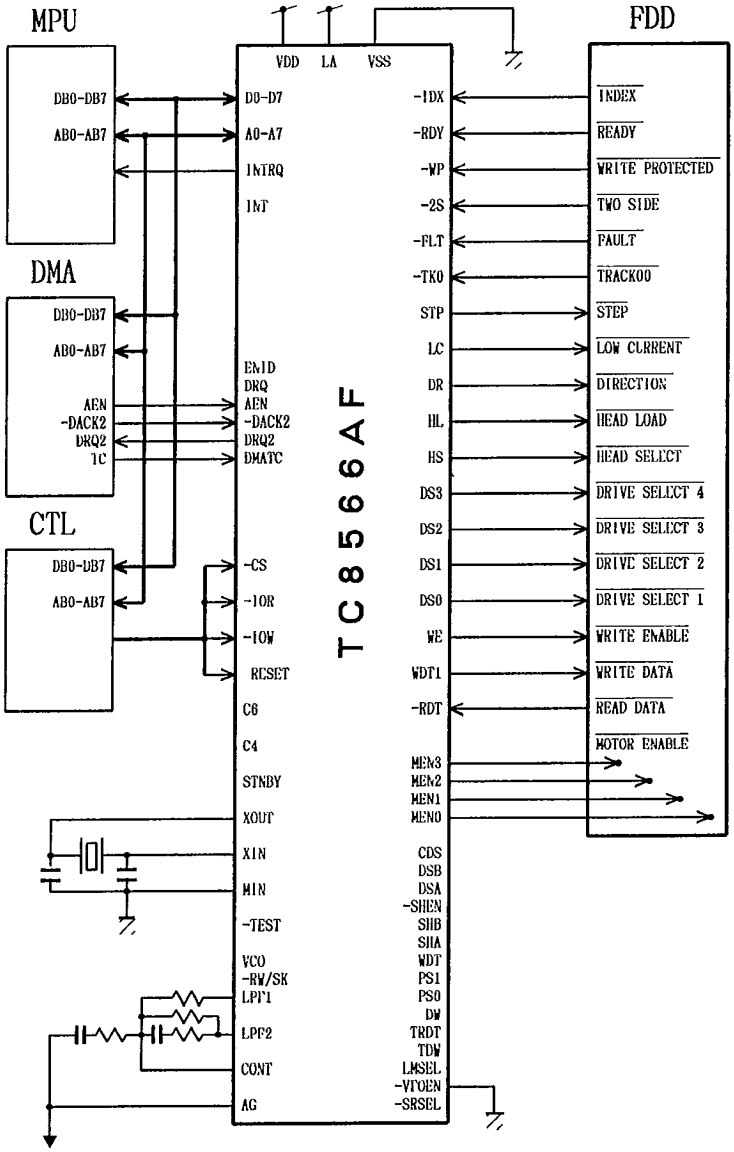
3. FLOPPY DISK SYSTEM

3.1. INTERNAL BLOCK DIAGRAM OF TC8566AF

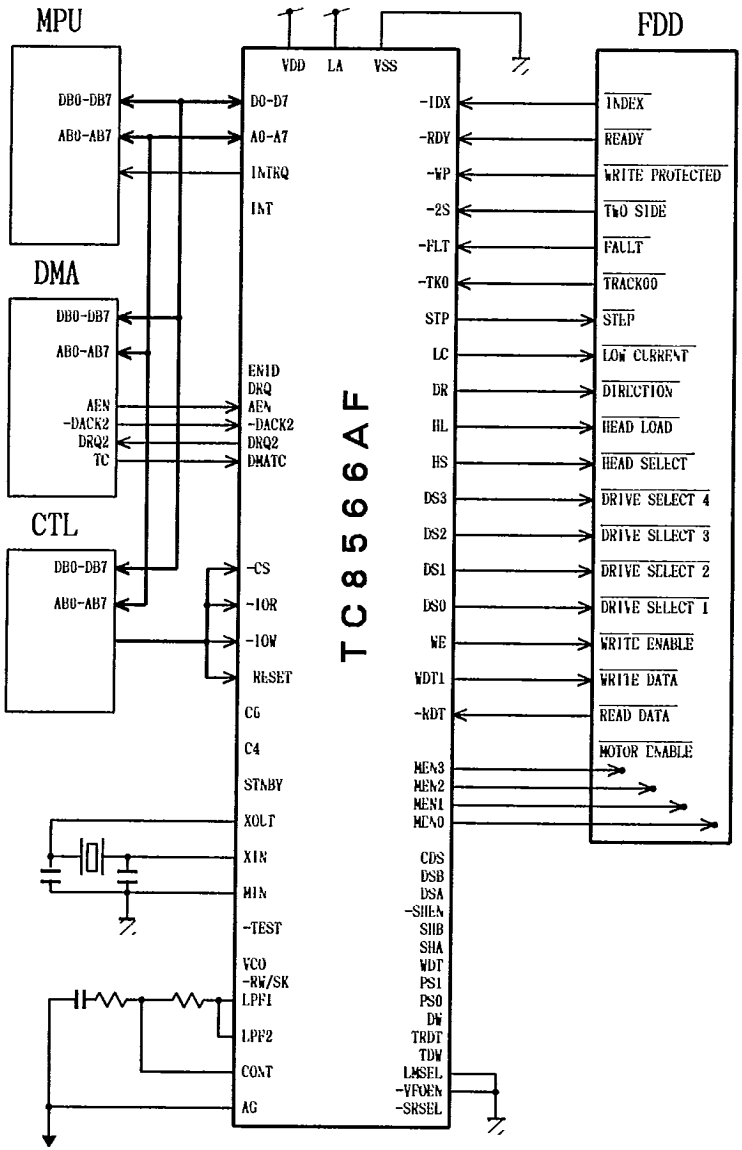


3.2. APPLICATION OF TC8566AF

3.2.1. 2 FILTER SWITCHING TYPE



3.2.2. 1 FILTER SWITCHING TYPE



4. PIN DESCRIPTION

4.1. PIN CONFIGURATION

NO.	I/O	NAME	NO.	I/O	NAME	NO.	I/O	NAME
1	O	C6	36	IO	VCO	71	O	FR
2	I	-IOR	37	O	LPF2	72	O	LC
3		NC	38	O	LPF1	73	O	DR
4	I	-IOW	39	O	CW	74	G	VSS
5	I	A0	40	I	DW	75	V	VDD
6	I	A1	41	O	FLT1	76	I	-IDX
7	I	A2	42	O	DOS	77	I	-RDY
8	I	A3	43	I	LOCK	78		NC
9	I	A4	44	I	-RDT	79		NC
10	I	A5	45	O	XOUT	80	I	-WP
11	I	A6	46	I	XIN	81	I	-2S
12	I	A7	47	I	-VFOEN	82	I	-FLT
13	I	-CS	48	I	MIN	83	I	-TKO
14	I	AEN	49	O	MFM	84	O	PS1
15	IO	D0	50		NC	85	O	PS0
16	IO	D1	51		NC	86	O	DSB
17	IO	D2	52		NC	87	O	DSA
18	IO	D3	53	I	-CL	88	I	LA
19	IO	D4	54	G	VSS	89		NC
20	IO	D5	55	O	SYNC	90	V	VDD
21	IO	D6	56	O	WDT1	91		NC
22	IO	D7	57	O	WE	92	I	CDS
23	O	DRQ2	58	O	HS	93	I	RESET
24	O	INTRQ	59	O	HL	94	I	SHB
25	O	INT	60	O	MEN3	95	I	SHA
26	O	DRQ	61	O	MEN2	96	I	-SHEN
27	G	VSS	62	O	MEN1	97	O	STNBY
28	G	AG	63	O	MEN0	98	O	WDT
29		NC	64	G	VSS	99	O	ENID
30		NC	65	V	VDD	100	O	C4
31		NC	66	O	DS3			
32	I	-DACK2	67	O	DS2			
33	I	DMATC	68	O	DS1			
34	I	CONT	69	O	DS0			
35	I	-TEST	70	O	STP			

4.2. DESCRIPTION OF PIN FUNCTION

[1] C6 (CONTROL OUT BIT 6) output
Output port of C6 bit in a control register.

[2] -IOR (IO READ) Input
Low active control signal to transfer data from the FDC to the Data-bus.

[3] NC (NON CONNECT)

[4] -IOW (IO WRITE) Input
Low active control signal to transfer data from the Data-bus to the FDC.

[5] A0 (ADDRESS 0) Input
[6] A1 (ADDRESS 1) Input
[7] A2 (ADDRESS 2) Input
[8] A3 (ADDRESS 3) Input
[9] A4 (ADDRESS 4) Input
[10] A5 (ADDRESS 5) Input
[11] A6 (ADDRESS 6) Input
[12] A7 (ADDRESS 7) Input
Address select input.

[13] -CS (Chip Select) Input
[14] AEN (Address enable) Input
"Low level" on [-CS] and [AEN] selects the FDC-II, and allows [-IOR] and [-IOW] to be effective.

[15] D0 (DATA 0) Input/Output
[16] D1 (DATA 1) Input/Output
[17] D2 (DATA 2) Input/Output
[18] D3 (DATA 3) Input/Output
[19] D4 (DATA 4) Input/Output
[20] D5 (DATA 5) Input/Output
[21] D6 (DATA 6) Input/Output
[22] D7 (DATA 7) Input/Output
Bidirectional 8-bit Data Bus.

[23] DRQ2 (DMA REQUEST 2) Output
Request signal for DMA transfer. This signal is the delayed [DRQ] from internal FDC chip. This signal is disabled to "Low level" with setting 0(zero) on the ENID bit in the CONTROL-REGISTER-0.

[24] INTRQ (INTERRUPT REQUEST) Output
Interrupt request signal for system from internal FDC chip. This signal is disabled to "LOW level" with setting 0(zero) on the ENID bit in the CONTROL-REGISTER-0.

[25] INT (INTERRUPT) Output
Interrupt request signal from internal FDC chip.

FLOPPY DISK CONTROLLER

[26] DRQ (DMA REQUEST) Output
DMA request signal from internal FDC chip.

[27] VSS (GROUND)
Chips ground for digital circuits.

[28] AG (ANALOGUE GROUND)
Analog ground for VCO and PLL circuits.

[29-31] NC (NON CONNECT)

[32] -DACK2 (DMA ACKNOWLEDGE) Input
Low active DMA cycle executing signal. When the FDC works DMA MODE, this signal controls DMA I/O.

[33] DMATC (DMA TERMINAL COUNT) Input
High active DMA transfer terminating signal. When the FDC works DMA MODE, this signal terminates the DMA transfer.

[34] CONT (VCO CONTROL INPUT) Input / Analog signal.
Analog voltage control input for VCO.

[35] -TEST (CHIP TEST) Input
The input terminal for LSI test. Internal PULL UP device allows to "High level" even if open circuits.

[36] VCO (VCO TEST) Input/Output
The input/output terminal for LSI test. To leave open for normal operation.

[37] LPF2 (LOW PASS FILTER 2) Output
The charge pump output for external Low Pass Filter. This output will select after PLL has pulled in the read signal and use low gain filter.

[38] LPF1 (LOW PASS FILTER 1) Output
The charge pump output for external Low Pass Filter. This output will activate when PLL circuit force to lock the read signal (Pull-in mode).

[39] TRDT (TEST READ DATA) Output
The terminal for test. Use in non-connect.

[40] DW (DATA WINDOW) Input
The window(for FDC) signal input when "External VCO mode" is selected. If internal VFO will be used, "HIGH or LOW level" should be applied for safe operation.

[41] -RW/SK (READ : WRITE/SEEK) Output
"Low" shows that read/write mode is selected, and "High" shows that seek mode is selected.

[42] TDW (TEST DATA WINDOW) Output
The terminal for test. Use in non-connect.

[43] LMSEL (LOCK MODE SELECT) Input
This signal decides the operation of the internal VFO circuit. Pull-up resistor is on-chip. The VFO operates in one filter non-switching mode when "Low", and operates in two filter (high gain and low gain filter) switching mode when "High" or open.

[44] -RDT (READ DATA) Input
The input for the READ DATA from the floppy disk drive. When internal VFO is operated, the negative MFM signal is applied. And when external VFO is used, then applied positive MFM signals.

[45] XOUT (XTAL OUT) Output
This output is inverted signal of [XIN], or connected the crystal oscillator.

[46] XIN (XTAL IN) Input
This input connects the crystal oscillator or external clock signal. In the standard usage, use 16MHz crystal oscillator.

[47] -VFOEN (VFO ENABLE) Input
"LOW level" on this terminal will select built-in VFO (internal). Otherwise use external VFO IC.

[48] MIN (MINI FLOPPY) Input
"HIGH level" on this terminal will select MINI-FLOPPY MODE and "LOW-level" will select STANDARD FLOPPY MODE.
In the MINI-FLOPPY mode, data transfer will perform at 250Kbps with 4MHz internal FDC clock which is selected by the clock control circuit in the LSI.

[49] MFM (MFM MODE) Output
This terminal output will show the mode of operation of FDC. "HIGH level" on this terminal shows that the FDC works at MFM mode and otherwise shows FM mode.

[50-52] NC

FLOPPY DISK CONTROLLER

[53] -SRSEL (STEP RATE SELECT) Input
When mini-floppy mode, this signal enables to change the internal FDC clock in accordance with the FDC operation mode. Pull-up resistor is on-chip.

MIN.	-SRSEL	-RW/SK	FDC OPERATION CLOCK
Low	X	X	Standard mode
High	High or non-connect	X	mini mode
High	Low	Low	mini mode
High	Low	High	Standard mode

"Low" enables to select 3ms step rate time for mini-floppy.

[54] VSS (GROUND)
Chips ground for digital circuits.

[55] SYNC (READ SYNC) Output
Indicate that FDC read out data from FDD. Signal for external VFO mode.

[56] WDT1 (WRITE DATA 1) Output
Pre-compensated write data.

[57] WE (WRITE ENABLE) Output
Write enable signal for FDD.

[58] HS (HEAD SELECT) Output

Head select signal	when LA=High	when LA=Low
High	Head 0	Head 1
Low	Head 1	Head 0

[59] HL (HEAD LOAD) Output
FDD head load signal. Low active when LA=Low.

[60] MEN3 (MOTOR ENABLE 3) Output
Motor enable for drive #3.

[61] MEN2 (MOTOR ENABLE 3) Output
Motor enable for drive #2.

[62] MEN1 (MOTOR ENABLE 3) Output
Motor enable for drive #1.

[63] MEN0 (MOTOR ENABLE 3) Output
Motor enable for drive #0.

[64] VSS (GROUND)
Chips ground for digital circuits.

[65] VDD (+5V POWER SUPPLY)

[66] DS3 (DRIVE SELECT 3) Output
Drive select for drive #3.

[67] DS2 (DRIVE SELECT 2) Output
Drive select for drive #2.

[68] DS1 (DRIVE SELECT 1) Output
Drive select for drive #1.

[69] DS0 (DRIVE SELECT 0) Output
Drive select for drive #0.

[70] STP (STEP PULSE) Output
Decoded step pulse signal, connected disk drives.

[71] FR (FAULT RESET) Output
Decoded fault reset signal, usually used in 8-inch STANDARD FDD.

[72] LC (LOW CURRNET) Output
Decoded Low current signal, indicates the Head position more inside than the 43rd track.

[73] DR (DIRECTION) Output
Decoded direction signal for head seek.

when	LA=high	LA=low
low	inner seek	outer seek
high	outer seek	inner seek

[74] VSS (GROUND)
Chips ground for digital circuits.

[75] VDD (+5V POWER SUPPLY)

[76] -IDX (INDEX) Input
Index pulse input from FDD system interface.

[77] -RDY (READY) Input
Drive ready signal from FDD system interface.

[78] NC
[79] NC

[80] -WP (WRITE PROTECT) Input
Write protected indicate signal from FDD system interface.

[81] -2S (2 SIDE) Input
Double sided indicate signal from FDD system interface. Usually use in the STANDARD 8-inch floppy disk.

FLOPPY DISK CONTROLLER

[82] -FLT (FAULT) Input
Fault states indicate signal from FDD system interface. Usually use in the STANDARD 8-inch floppy disk.

[83] -TK0 (TRACK ZERO) Input
Head position indicate signal from FDD system interface. Low level on this terminal means that the head of FDD is on the TRACK #0 position.

[84] PS1 (PRE- SHIFT 1) Output
[85] PS0 (PRE- SHIFT 0) Output
Raw signal from internal FDC chip. External pre-compensation circuit will use this signal as follows

PS0	PS1	PRE-SHIFT OPERATION
low	high	Late
low	low	Normal
high	low	Early

[86] DSB (DRIVE SELECT B) Output
[87] DSA (DRIVE SELECT A) Output
Undecoded drive select signal on the output of DS3-DS0.

DSB	DSA	selected drive
low	low	Drive #0
low	high	Drive #1
high	low	Drive #2
high	high	Drive #3

[88] LA (LOW ACTIVE) Input
Physical active level select on the output of FDD system interface signal, that is WDT1, WE, HS, HL, MEN0 - MEN3, DS0 - DS3, STP, FR, LC, and DR. High level on this terminal means that these signal will low active and can connect to directly FDD which has CMOS type of interface specification.

[89] NC
[90] VDD (+5V POWER SUPPLY)
[91]

[92] CDS (CONTROL DRIVE SELECT) Input
When this terminal is high level, DSB and DSA bits in a control register are used as a drive select code. And when CDS is low level, US1 and US0 outputs from internal FDC are used as a drive select code.

[93] RESET (RESET) Input
Reset control registers. The [-FRST] bit on the control register #0 is also reset, and consequently the internal FDC block is reset.

[94] SHB (SHIFT SELECT B) Input
[95] SHA (SHIFT SELECT A) Input
Select input for phase shift range of the write pre-compensation.

		Shift range	
SHB	SHA	MIN mode (5.25inch)	STD mode (8inch)
low	low	125ns	62.5ns
low	high	250ns	125.0ns
high	low	375ns	187.5ns
high	high	500ns	250.0ns

[96] -SHEN (SHIFT ENABLE) Input
If high level on this terminal, no pre-compensation shifting will be done.

[97] STNBY (STANDBY STATE) Output
This signal shows that FDC-II is in a standby mode. In a standby mode, all internal clock is stopped for save power dissipation and following signals are inactive states,
WDT1, WE, HS, HL, MEN0 -MEN3, DS0 - DS3, STP, FR, LC and DR.

[98] WDT (WRITE DATA) Output
Raw signal from internal FDC block. This signal made up of clock bits and data bits.

[99] ENID (ENABLE INT and DREQ) Output
Side output of ENID bit in a control register.

[100] C4 (CONTROL BIT 4) Output
Output of C4 bit in a control register.

5. DESCRIPTION

5.1. CONTROL REGISTER AND PERIPHERAL CIRCUITS

5.1.1. REGISTER AND ADDRESS

-AEN	-CS	A7	A6	A5	A4	A3	A2	A1	A0	Selection
High	X	X	X	X	X	X	X	X	X	NO SELECTION
X	High	X	X	X	X	X	X	X	X	
X	X	Low	X	X	X	X	X	X	X	
X	X	X	Low	X	X	X	X	X	X	
X	X	X	X	Low	X	X	X	X	X	
X	X	X	X	X	Low	X	X	X	X	
X	X	X	X	X	X	High	X	X	X	
Low	Low	High	High	High	High	Low	Low	Low	Low	
Low	Low	High	High	High	High	Low	Low	Low	High	
Low	Low	High	High	High	High	Low	Low	High	Low	CTL REG. 0
Low	Low	High	High	High	High	Low	Low	High	High	CTL REG. 1
Low	Low	High	High	High	High	Low	High	Low	Low	FDC STATUS REG.
Low	Low	High	High	High	High	Low	High	Low	High	FDC DATA REG.
Low	Low	High	High	High	High	Low	High	High	Low	NO SELECTION
Low	Low	High	High	High	High	Low	High	High	High	

High:High Level, Low:Low level, X:Don't care.
CTL REG. 0 : Control register 0
CTL REG. 1 : Control register 1

5.1.2. CONDITION OF STANDBY STATE

LSI will enter into standby mode after several times elapsed, when the SBM bit in the control register 0 is set to '1' and following conditions are filled. The waiting time is decided by the state of internal FDC mode. Usually, 6ms to 8ms in MINI floppy mode and 3ms to 4ms in STANDARD floppy mode. Additional condition is as follows.

- o -FRST bit of control register = 1.
- o Head is unloaded.
- o FDC is in the state that waiting command from the host.

The standby state will show with the output terminal [STNBY], and X'tal oscillation stops. Standby state allows the drive output signals, WE, HS, FR,STP, LC and DR to be inact-ive.

LSI will take off from the standby state when one of following condition is detected.

- o SBM bit is set to 0.
- o -FRST bit is set to 0.
- o FDC receives a command.

5.1.3. CONTROL REGISTER 0

This register is 8 bits write only register. High level on the [RESET] terminal will course all bits to 0.

BITS	SYMBOL	NAME	MEANINGS
D7	MEN3	Motor enable #3	Radial motor on signal for #3 Drive
D6	MEN2	Motor enable #2	Radial motor on signal for #2 Drive
D5	MEN1	Motor enable #1	Radial motor on signal for #1 Drive
D4	MEN0	Motor enable #0	Radial motor on signal for #0 Drive
D3	ENID	Enable INT & DMA Request	INTRQ and DRQ2 are enabled when this bit is High level.
D2	-FRST	Not FDC RST	0 on this bit will reset the internal FDC block. For normal operation, this bit should be set to 1.
D1	DSB	Drive select B	2 bit binary coded Drive select. This code is effective when the [CDS] input is high level.
D0	DSA	Drive select A	

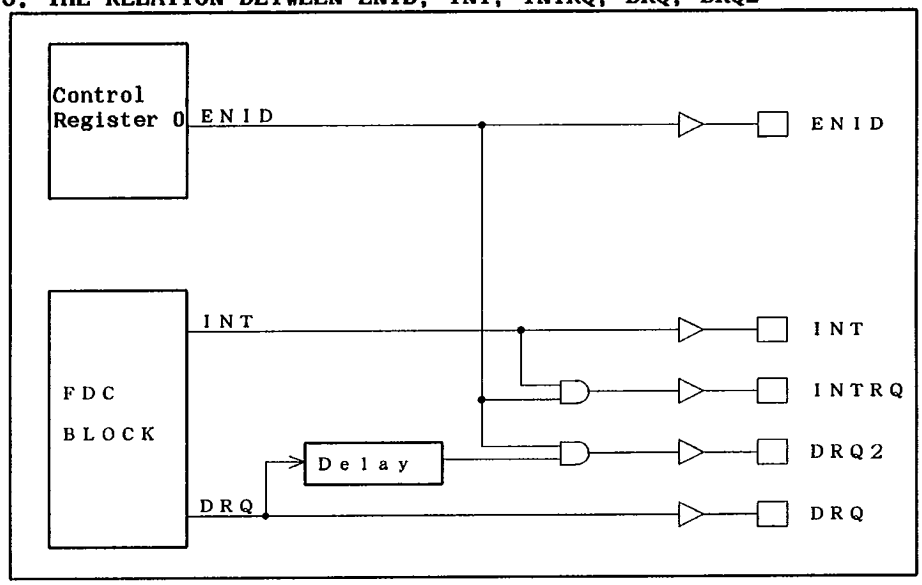
5.1.4 CONTROL REGISTER 1

This register is 4 bits write only register. High level on the [RESET] terminal will course all bits to 0.

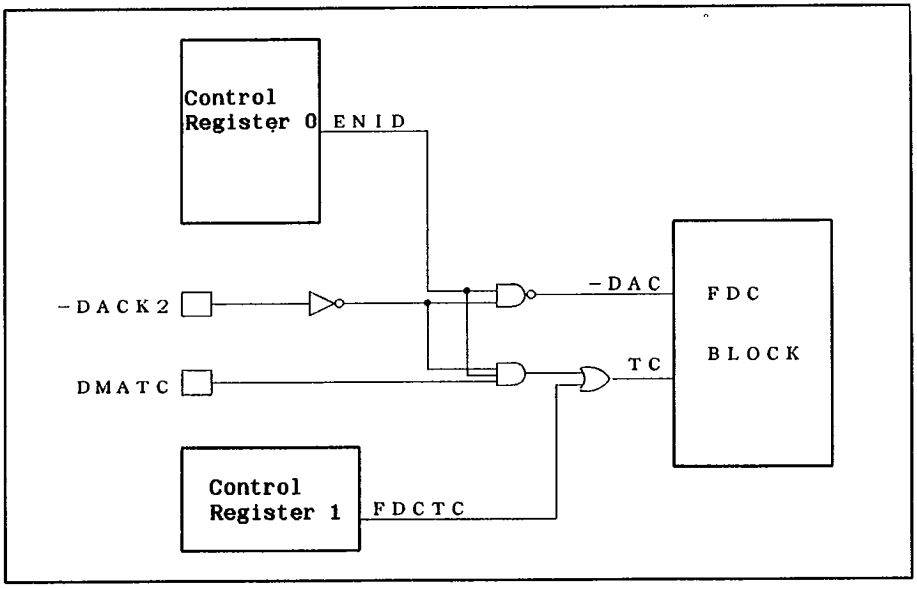
BITS	SYMBOL	NAME	MEANINGS
D7	NB6	ENABLE C6	When 1 is applied to this bit during byte write operation of this register, the value of C6 becomes to D6. When 0 is applied to this bit during byte write operation of this register, the value of C6 is to be copy of C6.
D6	C6	CONTROL 6	General purpose output port [C6].
D5	ENB4	ENABLE C4	Write enable of C4 i.e. C6
D4	C4	CONTROL 4	General purpose output port [C4]
D3	ENB2	ENABLE C2	Write enable of C2 i.e. C6
D2	SBM	STANDBY MODE	when 1 is applied to this bit, FDC enabled to transfer into stand by mode.
D1	ENB0	ENABLE C0	Write enable of C0 i.e. C6
D0	FDCTC	FDC Terminal Count	FDC terminal count control bit. This bit will be used to terminate data transfer with Non-DMA mode.

FLOPPY DISK CONTROLLER

5.1.5. THE RELATION BETWEEN ENID, INT, INTRQ, DRQ, DRQ2

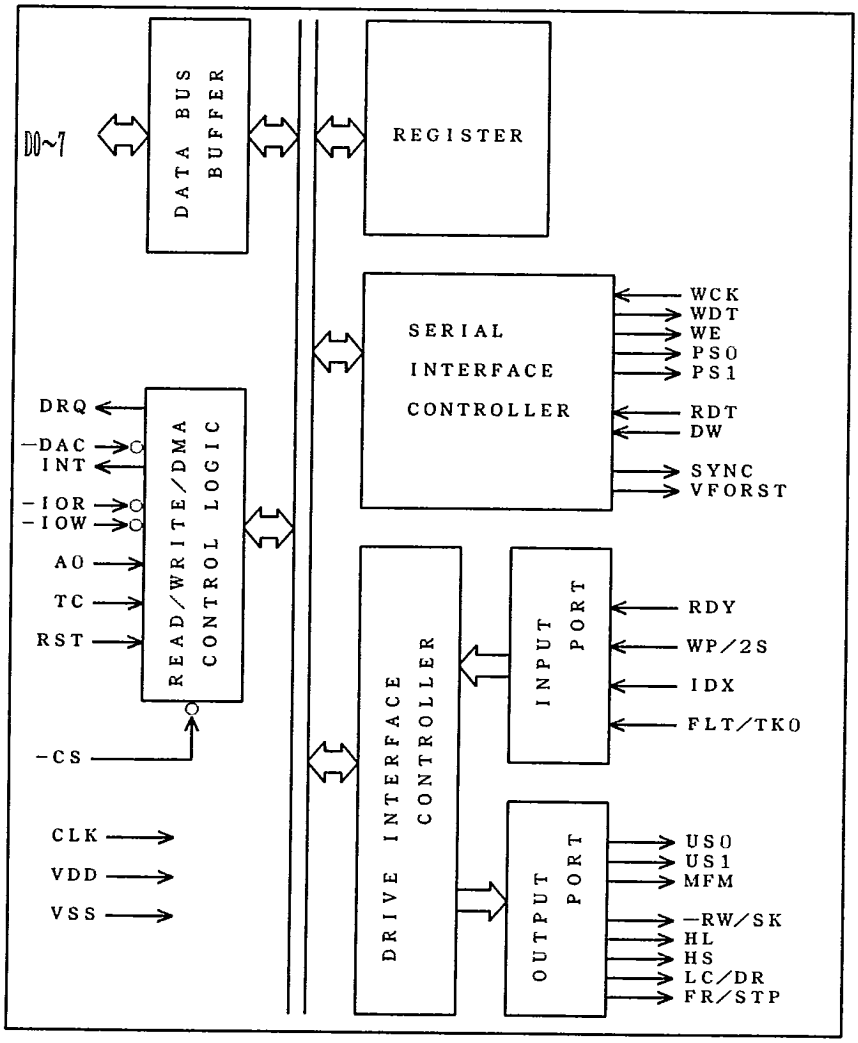


5.1.6. THE RELATION BETWEEN ENID, -DACK2, DMATC, FDCTC



5.2. FDC BLOCK

5.2.1. FDC BLOCK DIAGRAM



6

5.2.2. FDC'S REGISTER AND CPU INTERFACE

FDC has two 8-bit registers accessible by the main system processor. One is a Main Status Register, and the other is a Data Register. The Main Status Register indicates the status information of the FDC and is always accessible.

The Data Register is used for data transfer between the FDC and the main processor. Command bytes are written into the Data Register in order to program the FDC, and also Status bytes are read out of the Data Register in order to obtain the result after execution of the commands.

Main Status Register may be read and is used to facilitate the data transfer between the processor and the FDC. The relationship between Main Status Register and [-IOR],[-IOW] and [A0] signals is shown below.

[-CS]	[A0]	[-IOR]	[-IOW]	FUNCTION
H	X	X	X	Non Select
L	L	L	L	Illegal
L	L	L	H	Read Main Status Register
L	L	H	L	Illegal
L	H	L	L	Illegal
L	H	L	H	Read from Data Register
L	H	H	L	Write into Data Register

Each bit in the Main Status Register are defined as Table 5.2.2. The RQM and DIO bits in the Main Status Register indicate whether Data Register is ready or not and in which direction data will be transferred on Data Bus.

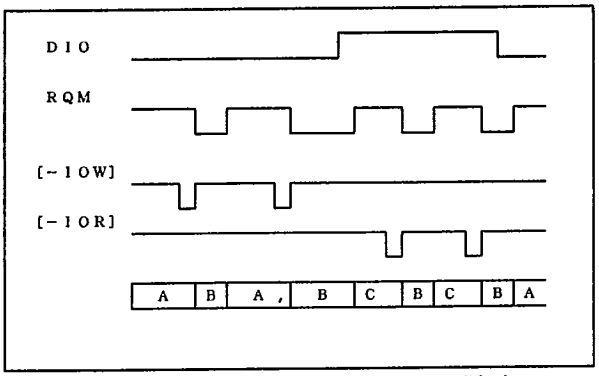


Fig.5.2.2. Main Status Register Timing

A: (DIO="Low" and RQM="High") The processor may write the data in Data Register.
B: (RQM="Low") Data Register is not ready.
C: (DIO="High" and RQM="High") In data register, data byte which will be read out by processor is already prepared.

Table 5.2.2. Main Status Register

BIT	SYMBOL	NAME	MEANING
D7	RQM	REQUEST for MASTER	Indicates that Data Register is ready to send the data to or to receive the data from the processor.
D6	DIO	DATA INPUT/ OUTPUT	Indicates the direction of data transfer between Data Register and the processor. When DIO is a "High", transfer is from Data Register to the processor. When DIO is a "Low", transfer from the processor to Data Register.
D5	NDM	Non-DMA mode	Indicates that the FDC is Non-DMA mode. It is set only during Execution-Phase in Non-DMA mode.
D4	CB	FDC BUSY	Indicates that FDC is in Execution-Phase of a read/write command , in Command-Phase, or in Result-Phase .
D3	D3B	FDD 3 BUSY	FDD number 3 is in the Seek mode.
D2	D2B	FDD 2 BUSY	FDD number 2 is in the Seek mode.
D1	D1B	FDD 1 BUsy	FDD number 1 is in the Seek mode.
D0	D0B	FDD 0 BUSY	FDD number 0 is in the Seek mode.

FDC supports fifteen different commands. Each of commands is initiated by a multi-byte transfer from the processor, and the result after executing of the command is a multi-byte transfer to the processor. Because the multi-byte information is interchanged between the FDC and the Processor, it is regarded that each command consists of following three phases.

Commands-Phase : The FDC receives the necessary information to perform a particular operation from the processor.
Execution-Phase : The FDC performs the specified operation .
Result-Phase : After the operation Result Status information or other information is sent to the processor.

In the Command-Phase or the Result-Phase, the processor must read out the Main Status Register before each byte of information is written into or read out from the Data Register.

When each byte of the command and the parameter is written into the FDC, bit D7 and D6 in the Main Status Register must be in high level and low level, respectively.

Because most of the Commands need multiple bytes, the Main Status Register must be read out before each byte is transferred to the FDC. In the Result-phase, the bit D7 and D6 in Main Status Register must be both in high levels before each byte is read out from the Data Register. The reading out of the Main Status Register before each byte transfer to the FDC is necessary only in the Command-Phase and the Result-Phase, but it is not always necessary in the Execution-Phase.

When the FDC is in Non-DMA mode, the receipt of each data byte (if the FDD is now reading out data from the FDD) is indicated by the Interrupt signal.

The generation of the Read signal ([-IOR]=0) will not only output the data on the data bus but also reset the INT signal. If the processor can not deal with interrupts fast enough (within 13us for MFM mode.), then it examines the Main Status Register, and then bit 7 (RQM) functions just like the Interrupt signal. Similarly in the Write command, Write signal resets the Interrupt signal.

If the FDC is in the DMA mode, then the Interrupt signal is not generated during the Execution-Phase. When the each data byte is available, the FDC generates DRQ(DMA request) signal. Then the DMA controller generates both DMA Acknowledge signal and Read signal ([-DAC]=0 and [-IOR]=0).

In a Read command, when the DMA acknowledge signal becomes low level, the FDC automatically resets the DRQ. In a Write command, [-IOW] is substituted for [-IOR]. If the Execution-Phase is terminated (Terminal Count has been inputted), the Interrupt request is generated. This means the beginning of the Result-Phase. When the first data byte is read during the Result-Phase, Interrupt signal is automatically reset. During the Result-Phase, all data bytes shown in the COMMAND TABLE must be read.

For example, the READ DATA COMMAND has seven data bytes in the Result-Phase. All seven data bytes must be read out in order to complete the READ DATA COMMAND. This FDC will not accept the next command until all these seven data bytes are read out. In the same way, all the data bytes of the other commands must be read out during the Result-Phase. The FDC has five Status Registers. The Main Status Register mentioned above can always be read out by the processor. The Other four Result Status Register (ST0,ST1,ST2,ST3) is available only in the Result-Phase, and read out only after the termination of the command .

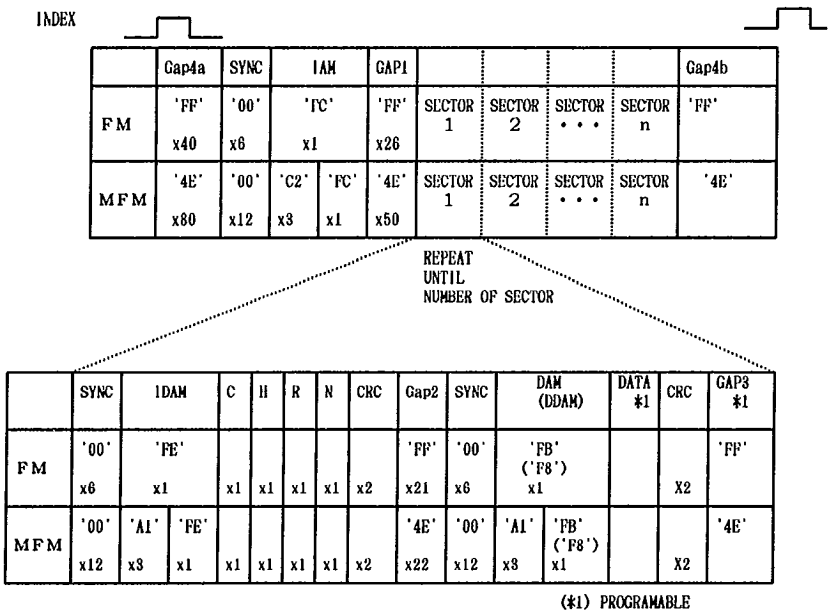
The specified command determines how many the Result Status Registers will be read. The COMMAND TABLE shows the data bytes that are sent to the FDC in the Command-Phase and read out from the FDC in the Result-Phase. That is, the command code must be sent first, and the other bytes must be sent in order. So the Command-Phase and the Result-Phase can not be shorten. When the last data byte in the Command-Phase is sent to the FDC, the Execution-Phase automatically starts. Similarly, when the last byte in the Result-Phase is read out, the command is automatically terminated, and then the FDC is ready for a new command.

5.2.3. POLLING FEATURE OF THE FDC

After the SPECIFY COMMAND has been sent to the FDC, the drive select signals , the US1 and US0, are automatically in the polling mode. Between the commands (and between the step pulses in the Seek mode), the FDC checks the four FDDs looking for a change of the ready signals from drive units.

If the Ready signal is changed, then the FDC generates the Interrupt signal. After the processor has issued the SENSE INTERRUPT STATUS COMMAND, the Result Status Register 0 (ST0) is read out, and the Not Ready bit (NR) in ST0 shows the present status. Because of the polling of Ready signal between the Commands, the processor can notice which drives are on line or which drives are off line.

5.2.4. TRACK FORMAT (IBM FORMAT)



MISSING CLOCK PART OF ADDRESS MARK

AM	FM		MFM	
	Data	Clock	Data	Clock
IAM	FC	D7	C2	14
IDAM	FE	C7	A1	0A
DAM	FB	C7	A1	0A
DDAM	F8	C7	A1	0A

5.2.5. MFM RULES

The data bit is written where the each bit will correspond to the center of the bit sell with "1". The clock bit is written at the head of the bit cell with "0" whose previous bit cell has "0".

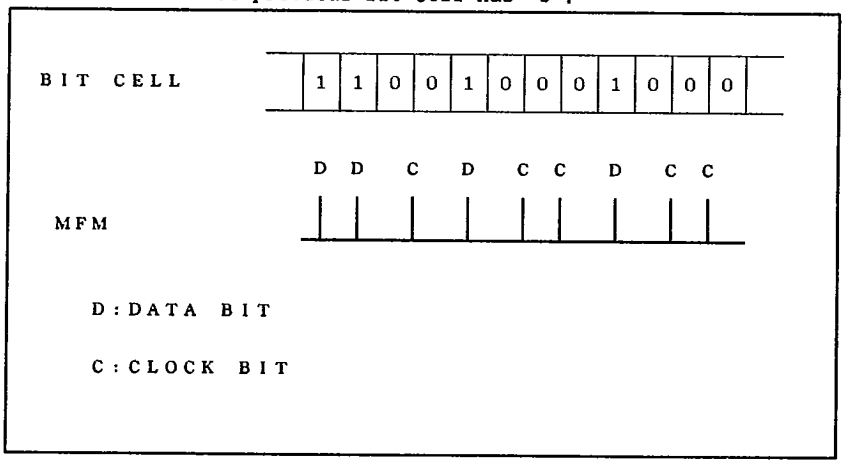


Fig.5.2.5. MFM Rules

5.2.6. COMMAND

(x:Don't care)

READ DATA COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	SK	0	0	1	1	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

WRITE DATA COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	0	0	0	1	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

WRITE DELETED DATA COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	0	0	1	0	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

READ DELETED DATA COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	SK	0	1	1	0	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

READ DIAGNOSTIC COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	MFM	0	0	0	0	1	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

READ ID COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	MFM	0	0	1	0	1	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* The first correct
		H								* ID information
		R								* read out during
		N								* Execution-Phase

FORMAT COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	MFM	0	0	1	1	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		N								
		SC								
		GPL								
		D								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* No meaning in
		H								* this case
		R								*
		N								*

SCAN EQUAL COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	SK	1	0	0	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		STP								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of last compared
		R								* sector
		N								*

SCAN LOW or EQUAL COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	SK	1	1	0	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		STP								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of last
		R								* compared sector
		N								*

SCAN HIGH or EQUAL COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	SK	1	1	1	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		STP								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of last
		R								* compared sector
		N								*

SEEK COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	0	0	0	1	1	1	1	Command code
		x	x	x	x	x	x	DS1	DS0	
		NCN								
E										Seek

RECALIBRATE COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	0	0	0	0	1	1	1	Command code
		x	x	x	x	x	x	DS1	DS0	
E										Recalibrate

SENSE INTERRUPT STATUS COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	0	0	0	1	0	0	0	Command code
R	R	STO								
		PCN								

SPECIFY COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	0	0	0	0	0	1	1	Command code
		SRT				HUT				
		HLT							ND	

6

FLOPPY DISK CONTROLLER

SENSE DEVICE STATUS COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	0	0	0	0	1	0	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
R	R	ST3								

INVALID COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	Invalid codes								
R	R	ST0								ST0=80H

Table 5.2.6. Symbols in the COMMAND TABLE

SYMBOL	NAME	DESCRIPTION
C	Cylinder Number	Indicates the cylinder number.
D	Data	Indicates the data pattern which is going to be written into data field.
D7-D0	Data Bus	8 bit data bus , D7 is MSB and D0 is LSB.
DS1,0	Drive Select	Indicates the drive number(0,1,2,3).
DTL	DATA Length	IF N=00, indicates the data length per sector which is going to be processed.
EOT	End of Track	Indicates the last Sector of a cylinder.
GPL	Gap Length	Indicates the length of Gap 3 (see 5.2.4. Track Format).
H	Head Address	Indicates the logical head address.
HS	Head Select	Indicates the physical head address.
HLT	Head Load Time	Indicates the head load time of FDD defined by Specify Command.
HUT	Head Unload Time	Indicates the head unload time after a read or write operation has completed which is defined by Specify Command .
MFM	MFM mode	If "Low" , FM mode is selected. If "High", MFM mode is selected.
MT	Multi Track	If "High" , multi track operation is to be performed.
N	Number	N is the code which indicates the number of data bytes written in a sector.
NCN	New Cylinder Number	Indicates the new cylinder number to be reached as a result of the seek operation.
ND	Non-DMA	Indicates the Non-DMA mode. Defined by the Specify Command.
PCN	Present Cylinder Number	Indicates the cylinder number when the Sense Interrupt Status Command has completed.
R	Record	Indicates the sector number.
R/W	Read/ Write	Indicates whether Read or Write.
SC	Sector	Indicates the number of sector per cylinder.
SK	Skip	Indicates the skip of the sector which has DDAM or DAM.
SRT	Step Rate Time	Indicates the step rate of FDD which is defined by Specify Command.

SYMBOL	NAME	DESCRIPTION
STP	Step	During the Scan operation , if STP is "1", then data in contiguous sector is compared byte by byte with data sent from the processor ,and if STP is "2" ,then alternate sectors are read and compared.

5.2.7. COMMAND DESCRIPTION

During the Command-Phase, the CPU must examine the Main Status Register before the writing of the each data byte into the Data Register. The DIO and RQM in the Main Status Register must be in a low level and a high level , respectively , before each byte is written into the FDC.

READ DATA COMMAND

The FDC needs nine data bytes in order to execute the READ DATA COMMAND. After the READ DATA COMMAND has been issued, the FDC loads the head (if it is in unload state), and waits the specified head load time . After the head load time has passed, the FDC begins to search ID Address Marks and read ID fields. If ID information stored in the ID Register agrees with ID information in ID field read from the diskette, then the FDC outputs data from the data field byte-by-byte to the main system via the data bus.

After the read operation of the current sector has been completed, the Sector Number (R) is incremented by one , the FDC reads the data from the next sector , and outputs the data on the data bus.

This continuous read function is called a "Multi-Sector Read Operation". The READ DATA COMMAND may be terminated by receiving a Terminal Count (TC) signal. If the FDC receives a TC signal, the FDC stops outputting data to processor, but continues to read data from the current sector, and checks the CRC(Cyclic Redundancy Code) bytes, and then terminates the READ DATA COMMAND at the end of the sector.

The amount of data which can be handled with a single command to the FDC depends on MT(Multi-Track), MFM(MFM/FM), and N(Number of bytes/sector). The Transfer Capacity is shown in Table 5.2.7A. below.

Table 5.2.7A. Transfer Capacity

MT	MFM	N	Maximum Transfer Capacity		Final Sector
			Bytes/Sector	Number of Sector	
0	0	00	128	26	SIDE 0 SECTOR 26 or
	1	01	256		SIDE 1 SECTOR 26
1	0	00	128	52	SIDE 1 SECTOR 26
	1	01	256		
0	0	01	256	16	SIDE 0 SECTOR 15 or
	1	02	512		SIDE 1 SECTOR 15
1	0	01	256	30	SIDE 0 SECTOR 15
	1	02	512		
0	0	02	512	8	SIDE 0 SECTOR 8 or
	1	03	1024		SIDE 1 SECTOR 8
1	0	02	512	16	SIDE 1 SECTOR 8
	1	03	1024		

FLOPPY DISK CONTROLLER

This FDC can read out the data from both sides of the diskette by the Multi-Track function. Data transfer will be performed from the Sector 1 of Side 0 to the last Sector of Side 1 for a particular cylinder at a time. But this function is effective to only one cylinder of the diskette.

After the reading out of the last sector, the FDC must receive the Terminal Count. If the FDC does not receive the Terminal Count signal, then the FDC sets the EN(end of cylinder) flag of ST1 to a high level and terminates the READ DATA COMMAND (bits 7 and 6 of ST0 is also set to a low level and a high level respectively : abnormal termination).

When N=0, DTL defines the data length which the FDC must treat as a sector. IF DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the data bus, but the FDC reads the whole sector internally, and then checks CRC bytes. When N≠0 DTL has no meaning.

When the READ DATA COMMAND has been completed , the head is not unloaded until the Head Unload Time(specified in the Specify Command) has passed. When the processor issues the next command (a read/write command) before head is unloaded, the head load time of the command is saved.

If the FDC can not find out the right sector until the FDC detects the Index Hole twice, the FDC sets the ND(No Data) flag in ST1 to a high level, and the READ DATA COMMAND will be abnormal terminated (bit 7 and bit 6 in ST0 set to a low level and a high level respectively).

After the reading of the ID field and the data field of the each sector, the FDC checks the CRC bytes. If a read error (incorrect CRC bytes in the ID field) is detected, the FDC sets the DE(Data Error) flag of ST1 to a high level, and if data error in the data field is detected , the DD(Data Error in Data Field) flag in ST2 is set to a high level, and then the READ DATA COMMAND is abnormal terminated.

IF the FDC read a Deleted Data Address Mark in the diskette, and SK bit (D5 bit in the Command code)is not set, then the FDC sets CM (Control Mark) flag to a high level after reading out all the data in the sector, and terminates the READ DATA COMMAND. When SK=1, the FDC skips the Sector that has DDAM, and reads out the next sector.

During the data transfer between the FDC and the processor, the FDC must receive the service from the processor within 27us in FM mode, and 13 us in MFM mode. If the FDC does not receive this service, the FDC sets OR (Over Run) flag to a high level, and terminates the READ DATA COMMAND (abnormal termination).

If a read (or write) operation is terminated by inputting the Terminal Count signal, the information of Result-Phase is defined by MT bit and EOT byte. Table 5.2.7B. shows the value for C,H,R and N when the command is normally terminated.

Table 5.2.7B ID Information at Normal Termination

MT	EOT	Final Transferred Sector	ID Information in Result-Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R+1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C+1	NC	R=01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R+1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C+1	NC	R=01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R+1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R=01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R+1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C+1	LSB	R=01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes) NC(No Change): The same value as the one at the beginning of command execution.
LSB(Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA COMMAND

The FDC needs nine data bytes in order to execute the WRITE DATA COMMAND. If the WRITE DATA COMMAND has been issued, the FDC loads the head (if the head is in the unload state). After the specified head load waiting time(defined in the SPECIFY COMMAND) has passed, the FDC begins to read the ID field. If the sector number stored in ID Register (IDR) matched with the sector number read from the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs to the FDD.

After the writing the data into the current sector, the FDC increments the sector number stored in R by one, and then the FDC writes the next data field. The FDC continues this Multi-Sector write operation until the Terminal Count signal is issued. Even if the FDC has received the Terminal Count signal, the FDC continues writing for the sector, and the data field will be completed. If the FDC receives the Terminal Count signal while the FDC is writing data in data field, then the remained data field will be filled with 00.

The FDC reads out the each sector of ID field, and checks the CRC bytes. If the FDC finds out the Read Error in ID field (incorrect CRC bytes), the FDC sets DE (Data Error) of ST1 to a high level, and terminates the WRITE DATA COMMAND(Abnormal termination).

The rules of the WRITE COMMANDs are much similar to the rules of the READ DATA COMMAND. The following items are same ; see the previous section (5.2.1).

- Transfer Capacity
- EN flag
- Head unload time
- ID information at the normal termination
- Meaning of DTL when N=0 and when N≠ 0

During the execution of the WRITE DATA COMMAND, the data transfer between the processor and the FDC must be performed within 31us in FM mode, and 15us in MFM mode. If it is not performed, the FDC sets OR flag of ST1 to a high level, and terminates the command (Abnormal Termination).

WRITE DELETED DATA COMMAND

This command is the same command as the WRITE DATA COMMAND except that the FDC writes the DDAM (Deleted Data Address Mark) at the beginning of the Data Field instead of the normal DAM (Data Address Mark).

READ DELETED DATA COMMAND

This command is the same as the READ DATA COMMAND except that the FDC reads the sectors with DDAM instead of those with DAM at the beginning of a Data Field. If the FDC detects DAM and SK=0 ,then the FDC will read the whole sector and set CM flag in ST2 to a high level and terminate the command (Normal Termination). If the FDC finds out DAM and SK=1 then the FDC will skip the sector with DAM and read the next sector.

READ DIAGNOSTIC COMMAND

This command is the same as the READ DATA COMMAND except that the FDC reads all the data continuously from each sector of a track. Just after the FDC receives the Index signal, the FDC begins to read out all the data field on the track as a continuous block. Even if the FDC finds out the CRC error in ID or data field, the FDC continues to read data from the track. The FDC compares the ID information read out from each sector with the value stored in IDR, and if there is no comparison, the FDC sets ND flag to a high level. This command has neither the Multi-Track function nor the skip function.

This command will be terminated when EOT number of sectors have been read out. When ID Address Mark on the diskette is not found out until the FDC finds out the Index Hall twice, MA (Missing Address Mark) in ST1 is set to a high level, and the command is terminated(Abnormal Termination).

READ ID COMMAND

This command is used to inform the processor of the current head point. The FDC stores the first ID information to be read out. If the right ID Address Mark is not found on the diskette until the FDC finds out the Index Hall twice, the FDC sets MA flag in ST1 to a high level, and if there is no ID field without CRC error, ND flag in ST1 is set to a high level, and the command is terminated(Abnormal Termination).

FORMAT COMMAND

The Format Command allows an entire track to be formatted. After the Index Hall is detected, the FDC writes data on the Diskette. Gaps, Address Marks, ID fields and Data fields in IBM System34 (double density) or IBM System3740 (single density) Format are recorded. The particular format is controlled by the values programmed in N,SC,GPL and D during the Command-Phase. The data byte stored in D is written into the data field. The data bytes of ID field in each sector is provided by the processor. That is, the FDC requests four data bytes per sector for C, H, R and N. This function allows the diskette to be formatted with non-sequential sector numbers.

After the each sector is formatted, the processor must send the new values of C,H,R and N to the FDC for the next sector on the track. After a sector is formatted, the contents of the R-register is incremented by one. Thus, when the R register is read out during the Result-Phase, it contains a value of R+1. This incrementing and formatting continues for the track until the FDC detects the Index Hall for the second time. When the FDC finds the Index Hall twice, the command is terminated.

When the FDC received the Fault signal from the FDD at the end of the write operation, the FDC sets the EC flag in ST0 to a high level, and sets bit 7 and bit 6 in ST0 to a low level and a high level respectively, and terminates the command. If the Ready signal changes to a low level at the beginning of the command execution, then the command is terminated.

Table 5.2.7C. shows the relationship of N, SC and GPL for various Sector sizes.

Table 5.2.7C. Relationship of Sector Sizes

FORMAT	SECTOR SIZE byte/sector	N (16)	SC (16)	GPL (16)	REMARKS
FM mode	128	00	1A	1B	IBM Diskette 1
	256	01	0F	2A	IBM Diskette 2
	512	02	08	3A	
	1024	03	04	-	
	2048	04	02	-	
	4096	05	01	-	
MFM mode	256	01	1A	36	IBM Diskette 2D
	512	02	0F	54	
	1024	03	08	74	IBM Diskette 2D
	2048	04	04	-	
	4096	05	02	-	
	8192	06	01	-	

SCAN COMMAND

The SCAN COMMANDs allow the data read from the diskette to be compared with the data sent from the Main System (the processor in Non-DMA mode, and the DMA controller in DAM mode). The FDC compares the data byte-by-byte, and searches the sector which meets the condition(equal, low or equal, high or equal).

After a entire sector is compared ,if the condition is not met, the sector number is incremented (R+STP→R), and the scan operation is continued. The scan operation is continued until the following conditions occur ;

- o The conditions for scan are met (equal,high or equal,low or equal).
- o The last sector on the track (EOT) is reached.
- o The Terminal Count signal is received.

If the scan equal condition are met, the FDC sets SH(Scan Hit) flag in ST2 to a high level, and then the SCAN COMMAND is terminated(Normal termination).

If the condition for scan is not met between the starting sector (specified by R) and the last sector (EOT) on the same cylinder, the FDC sets the SN (Scan Not Satisfied) flag in ST2 to a high level, and then terminates the command. If the FDC receives the Terminal Count from the processor or the DMA controller during the scan operation, the FDC completes the comparison of the data byte in process, and then terminates the command. TABLE 6 shows the status of bit SN and SH under the scan conditions.

Table 5.2.7D. Scan Status Codes

COMMAND	ST2		COMMENTS
	SN	SH	
SCAN	0	1	DISK = MAIN
EQUAL	1	0	DISK ≠ MAIN
SCAN	0	1	DISK = MAIN
LOW or	0	0	DISK < MAIN
EQUAL	1	0	DISK > MAIN
SCAN	0	1	DISK = MAIN
HIGH or	0	0	DISK > MAIN
EQUAL	1	0	DISK < MAIN

If the FDC finds out the DDAM on the sector and SK=0, then the FDC regards the sector as the last sector on the cylinder, and sets the CM flag in ST2 to a high level, and terminates the command (Normal Termination). If SK=1, the FDC skips the sector with DDAM, and reads out the next sector. Then the FDC sets CM flag in ST2 to a high level in order to show that the DDAM is found out. When either STP or MT is programmed, the FDC must read out the last sector on the track.

For example, if STP=02, MT=0 and the sectors are numbered in sequence 1 to 26, and SCAN COMMAND is started from the 21 Sector, then the FDC reads out the sector 21,23,25 and skips the next sector 26 , and finds out the Index Hall before reading the EOT value of 26. This result causes the abnormal termination of the command. If EOT is set at 25 or the scanning is started at the sector 20, then the command will be normal termination.

During the SCAN COMMAND, it is necessary to transfer the data which will be compared with the data read out from the diskette to the FDC by whether the processor or the DMA controller. If the data are not transferred within 27us in FM mode and 13us in MFM mode, the FDC sets the OR (Over Run) flag in ST1, and terminates the command (Abnormal Termination).

SEEK COMMAND

This command is used to move the Read/Write Head from cylinder to cylinder. The FDC compares the PCN which is current head position with the NCN. If there is a difference, the FDC performs the following operation.

PCN < NCN : Direction signal to the FDD is set to a high level, and the Step Pulses are issued (Step In).
PCN > NCN : Direction signal to the FDD is set to a low level, and the Step Pulses are issued (Step Out).

The rate of outputting the step pulses is controlled by the SRT (Step Rate Time) in the SPECIFY COMMAND. The FDC compares NCN with PCN at outputting the step pulses, and if NCN=PCN, then SE (Seek End) flag in ST0 is set to a low level, and the command is terminated. The FDC is in FDC Busy state during the Command-Phase of this command, but the FDC is in Non-Busy state during the Execution-Phase of this command. If the FDC is in Non-Busy state, the FDC accepts another SEEK COMMAND. This function allows the FDC to do the parallel seek operation for up to 4 FDDs at a time.

If the FDD is in the Not Ready state at the beginning of the Execution-Phase of this command or during the seek operation, the NR (Not Ready) flag in ST0 is set to a high level and the command is terminated.

RECALIBRATE COMMAND

The Read/Write Head within the FDD is moved to the Track 0 position under control of the RECALIBRATE COMMAND. The FDC clears the contents of PCN register, and checks the Track 0 signal. If the Track 0 signal is in a low level, the FDC sets the Direction signal to a low level, and issues the Step Pulses.

When the Track 0 signal changes to a high level, the FDC sets SE (Seek End) flag to a high level, and terminates the command. If the Track 0 signal is still low after the FDC has issued the 255 Step Pulses, SE flag and EC flag in ST0 are set to both high levels, and the command is terminated. The RECALIBRATE COMMAND is the same as the SEEK COMMAND about the function to overlap the operation to multiple FDDs and about the loss of the Ready signal.

SENSE INTERRUPT STATUS COMMAND

The FDC generates the Interrupt signal by the following reasons.

1 The beginning of Result-Phase in the Following commands:
   a READ DATA COMMAND
   b READ DIAGNOSTIC COMMAND
   c READ ID COMMAND
   d READ DELETED DATA COMMAND
   e WRITE DATA COMMAND
   f FORMAT COMMAND
   g WRITE DELETED DATA COMMAND
   h SCAN COMMANDS
2 The change of Ready line of FDD.
3 At the end of the SEEK or RECALIBRATE COMMAND.
4 During the Execution-Phase in the Non-DMA mode.

Interrupts caused by reason 1 and 4 occur during the normal command operation, and the processor can notice the interrupts easily. But the interrupts caused by the reason 2 and 3 may be identified with the request of issuing the SENSE INTERRUPT STATUS COMMAND. When this command is issued, Interrupt signal is reset, and bit 5, bit 6 and bit 7 in ST0 indicate the reason of the interrupt.

Neither the SEEK nor the RECALIBRATE COMMAND has a Result-Phase. Therefore, it is necessary to use the SENSE INTERRUPT COMMAND after these commands in order to terminate them effectively and confirm the head position (PCN).

Table 5.2.7E. SEEK , INTERRUPT CODES

INTERRUPT CODE		SEEK END	MEANING
BIT 7	BIT 6	BIT 5	
1	1	0	Changing of the state of the READY LINE
0	0	1	Normal Termination of the SEEK and RECALIBRATE COMMAND
0	1	1	Abnormal Termination of the SEEK and RECALIBRATE COMMAND

SPECIFY COMMAND

This SPECIFY COMMAND initiates the values of three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution-Phase of the read/write commands to the unloading of the head. This timer is programmable from 16 to 240 ms at intervals of 16 ms (01=16ms, 02=32ms, ... ,0F=240ms).

The SRT defines the time interval between step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F=1ms,E=2ms ,... ,0=16ms). The HLT defines the time from the rising of the Head Load signal to the starting of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2ms (01=2ms, 02=4ms, 03=6ms, ... ,7F=254ms).

The interval times mentioned above are a direct function of the clock. The times indicated above are for a 8MHz clock. If the clock frequency is 4MHz (mini floppy), all the times are twice as long as the times indicated above.

The ND bit is a flag to select the DMA operation or Non-DMA operation. If ND is in a high level then Non-DMA mode is selected, and if ND is in a low level then DMA mode is selected.

SENSE DEVICE STATUS COMMAND

The processor may use this command whenever it wishes to know the status of the FDDs. The drive status information is contained in ST3.

INVALID COMMAND

If an invalid command (a command not defined above) is send to the FDC, the FDC terminates the command. The FDC does not generate the Interrupt signal during the Result-Phase. Bit 6 and bit 7 in the Main Status Register set to both high levels indicates to the processor that the FDC is in the Result-Phase and that the contents of ST0 must be read out. ST0 is set to a 80H showing that an invalid command was received.

The SENSE INTERRUPT STATUS COMMAND must be sent after an interrupt of the SEEK COMMAND or RECALIBRATE COMMAND has occurred, otherwise the FDC regards this command as invalid. The users may use this command as a Non-Op command to place the FDC in a stand-by or non-operation state.

5.2.8. RESULT STATUS REGISTER

RESULT STATUS REGISTER 0 (ST0)

BIT	SYMBOL	NAME	DESCRIPTION
D7 D6	IC	Interrupt Code	D7=0 and D6=0 Normal Termination of Command (NT), Command was completed and properly executed.
			D7=0 and D6=1 Abnormal Termination of Command(AT). Command execution was started, but was not successfully completed.
			D7=1 and D6=0 Command was Invalid Command(IC). The command which has been issued was not started.
			D7=1 and D6=1 This indicates that the Ready Line from the FDD was changed.
D5	SE	Seek End	This flag is set to a "1",when the SEEK COMMAND was completed.
D4	EC	Equipment Check	When the FDC received the Fault signal from the FDD, or when the Track 0 signal was not set to a "1" after 255 step pulses during the RECALIBRATE COMMAND, this flag is set to a "1".
D3	NR	Not Ready	When the FDD is in the Not-Ready state and a read/write command is issued, this flag is set. For example, when a read/write command is issued for Side 1 of a single sided drive, this flag is set.
D2	HD	Head Address	This flag indicates the state of the head at interrupt.
D1 D0	DS1 DS0	Drive Select 0,1	These flags indicate the drive number at interrupt.

FLOPPY DISK CONTROLLER

RESULT STATUS REGISTER 1 (ST1)

BIT	SYMBOL	NAME	DESCRIPTION
D7	EN	End of Cylinder	This flag is set when the FDC tries to access a sector beyond the last sector of a cylinder.
D6	-		
D5	DE	Data Error	This flag is set when the FDC finds the CRC Error either in the ID field or the data field.
D4	OR	Over Run	This flag is set when the FDC does not receive the service from the main system during data transfers within a certain time interval.
D3	-		
D2	ND	No Data	o This flag is set when the FDC can not find out the sector specified in the IDR during the execution of following commands: READ DATA READ DELETED DATA WRITE DATA WRITE DELETED DATA SCAN o This flag is set when the FDC can not find the ID field without the CRC error during the execution of the READ ID COMMAND. o This flag is set when the starting sector cannot be found during the executing the READ DIAGNOSTIC COMMAND.
D1	NW	Not Writable	This flag is set if the FDC detects the write protect signal from the FDD during the executing following commands: WRITE DATA WRITE DELETED DATA FORMAT
D0	MA	Missing Address Mark	o This flag is set if IDAM cannot be found out until the FDC finds the Index Hall twice. o This flag is set if the FDC can not find the DAM or DDAM. The MD flag of ST2 is also set in this case.

RESULT STATUS REGISTER 2 (ST2)

BIT	SYMBOL	NAME	DESCRIPTION
D7	-		
D6	CM	Control Mark	While executing the READ DATA or the SCAN COMMAND, this flag is set when the FDC finds out the sector with the DDAM. During executing the READ DELETED DATA COMMAND, this flag is set when the FDC finds out the Sector with the DAM.
D5	DD	Data Error in Data Field	This flag is set when the FDC detects a CRC Error in data field.
D4	NC	No Cylinder	This flag is set when the contents of C on the medium is different from that stored in the IDR. This flag is related with the ND flag.
D3	SH	Scan Equal Satisfied	This flag is set if the condition of "equal" is satisfied during the execution of the SCAN COMMAND.
D2	SN	Scan Not Satisfied	This flag is set if the FDC cannot find out the sector which satisfies the condition during the execution of the SCAN COMMAND.
D1	BC	Bad Cylinder	This flag is set if the content of C on the medium is FF and differs from that stored in IDR. This bit is related with the ND bit.
D0	MD	Missing Address Mark in Data Field	This flag is set if the FDC cannot find out the DAM or DDAM while the data are read from the medium.

FLOPPY DISK CONTROLLER

RESULT STATUS REGISTER 3 (ST3)

BIT	SYMBOL	NAME	DESCRIPTION
D7	FLT	Fault	This bit indicates the state of the Fault signal from the FDD.
D6	WP	Write Protect	This bit indicates the state of the the Write Protect signal from the FDD.
D5	RDY	Ready	This bit indicates the state of the Ready signal from the FDD.
D4	TK0	Track 0	This bit indicates the state of the Track 0 signal from the FDD.
D3	2S	Two Side	This bit indicates the state of the Two Side signal from the FDD.
D2	HD	Head Address	This bit indicates the state of the Head Select signal to the FDD.
D1	DS1	Drive Select 1	This bit indicates the state of the Drive Select 1 signal to the FDD.
D0	DS0	Drive Select 0	This bit indicates the state of the Drive Select 0 signal to the FDD.

5.3. VFO UNIT

5.3.1. VFO UNIT BLOCK DIAGRAM

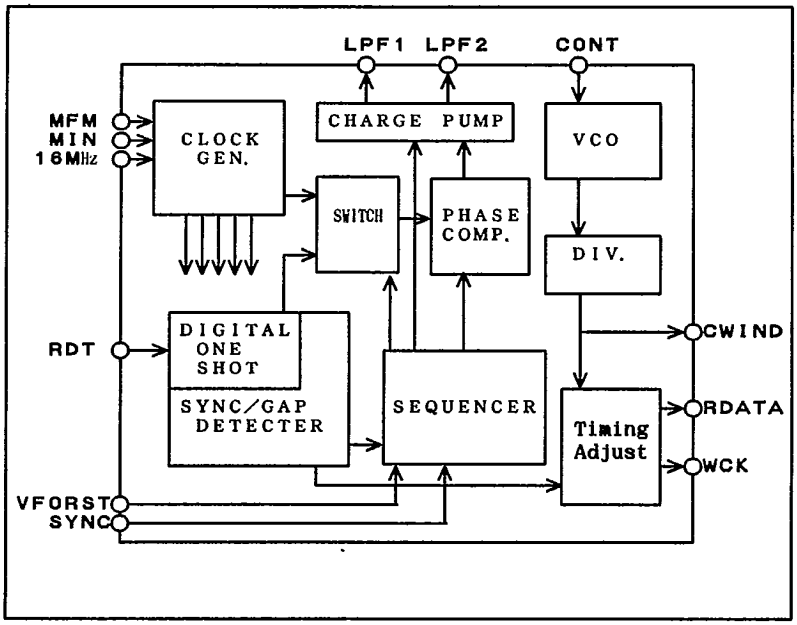


Fig.5.3.1. VFO Block Diagram

5.3.2. DESCRIPTION OF EACH BLOCKS.

(1) Time base generator/Divider circuit

This block consists of 16MHz crystal oscillator and divider. It generates all timing signals for VFO operation. The operation mode MFM and MIN signals change the divisor of these timings.

	STD mode (500kbps)	MINI mode (250kbps)
mode MFM	500 KHz	250 KHz
mode FM	250 KHz	125 KHz

(2) SYNC GAP DETECTOR/DIGITAL ONE-SHOT

SYNC pattern detect circuit when the FDC begins the read operation. SYNC pattern '00' is continuance pulse series whose interval is TSYNC. This circuit judges to be SYNC the pulse series whose interval is between TSYNC -25% and TSYNC +25%, and the other pulse series to be GAP. When 16MHz clock is applied in [XIN] terminal, the value of TSYNC, TSYNC +25% and TSYNC -25% are as follows.

	STD mode (500kbps)	MINI mode (250kbps)
TSYNC	2.0 us	4.0 us
TSYNC +25%	2.5 us	5.0 us
TSYNC -25%	1.5 us	3.0 us

Lower limit for MFM mode and upper limit for FM mode are non-sense for read/write operation but allow to distinguish 500Kbps from 300Kbps.

Digital one shot circuit works so as to centering the data pulse with window clock signal. This circuit use doubled [XIN] clock (16MHz), so it has 31.25 ns quantitized error.

	STD mode (500kbps)	MINI mode (250kbps)
mode MFM	500 ns	1000 ns
mode FM	1000 ns	2000 ns

(3) VOLTAGE CONTROLLED oscillator (VCO)

This VCO is automatically adjust its center frequency using PLL circuit. When 16MHz is used for [XIN] clock, 2MHz is the frequency at VCONT voltage is 2.5V. The conversion gain via voltage on VCONT terminal is as follows.

$Kv = 2.5 \times 10^{6}$ [rad/sec V]

(4) TIMING ADJUSTING CIRCUIT

This circuit regenerates data and clock bit in MFM signal so as to get best read margin against the peak shift phenomenon in the data from the FDD.

(5) SEQUENCER

VFO start its operation with the starting of read request from the FDC. The sequencer controls all operation that is, hunting SYNC pattern, detecting address mark, changing PLL filter constant etc..

5.3.3. OPERATION FLOW OF VFO

The operation of the VFO part is explained as the combination of the control mode of each circuit. The mode of each part which concerns the VFO operation is as follows.

[Phase Comparator]

One input of the phase comparator is the window signal which is the divided signal of the VCO output. The other input is either the read data or standardized clock from [XIN] whose frequency is the same as window signal.
There are things to switch the charge pump outputs and to change the gain of phase comparator in order to distinguish lock state from unlock state of the VCO.

[External Input]

SYNC	:	Input to indicate that the FDC is in read data.
VFORST	:	Pulse generated by internal FDC when the FDC becomes SYNC state, and when the first data byte after sync detection is not address mark and the FDC begins to search next sync pattern.

VFO has three transition states as follows.

QF : VCO is tracing for basic clock from [XIN] 16MHz with high gain.
QH : VCO is tracing for read data with high gain.
QL : VCO is tracing for read data with low gain.

There is SYNC/GAP detector to control state transition except mentioned above. This circuit always checks read data pulses. If there is a pulse without regular interval time, GAP is outputted. This output is held for 8 bit time, SYNCD is outputted when there is no GAP output during 2 byte time for FM mode or during 4 byte time for MFM mode. Fig. 5.3.3A. shows VFO states transition flow. Fig.5.3.3B. shows the timing of VFORST which the FDC outputs.

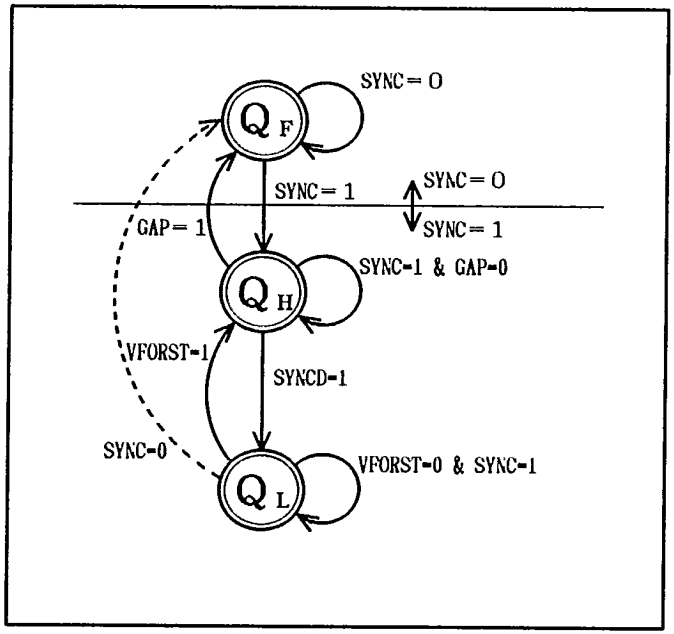


Fig.5.3.3A. VFO States Transition

6

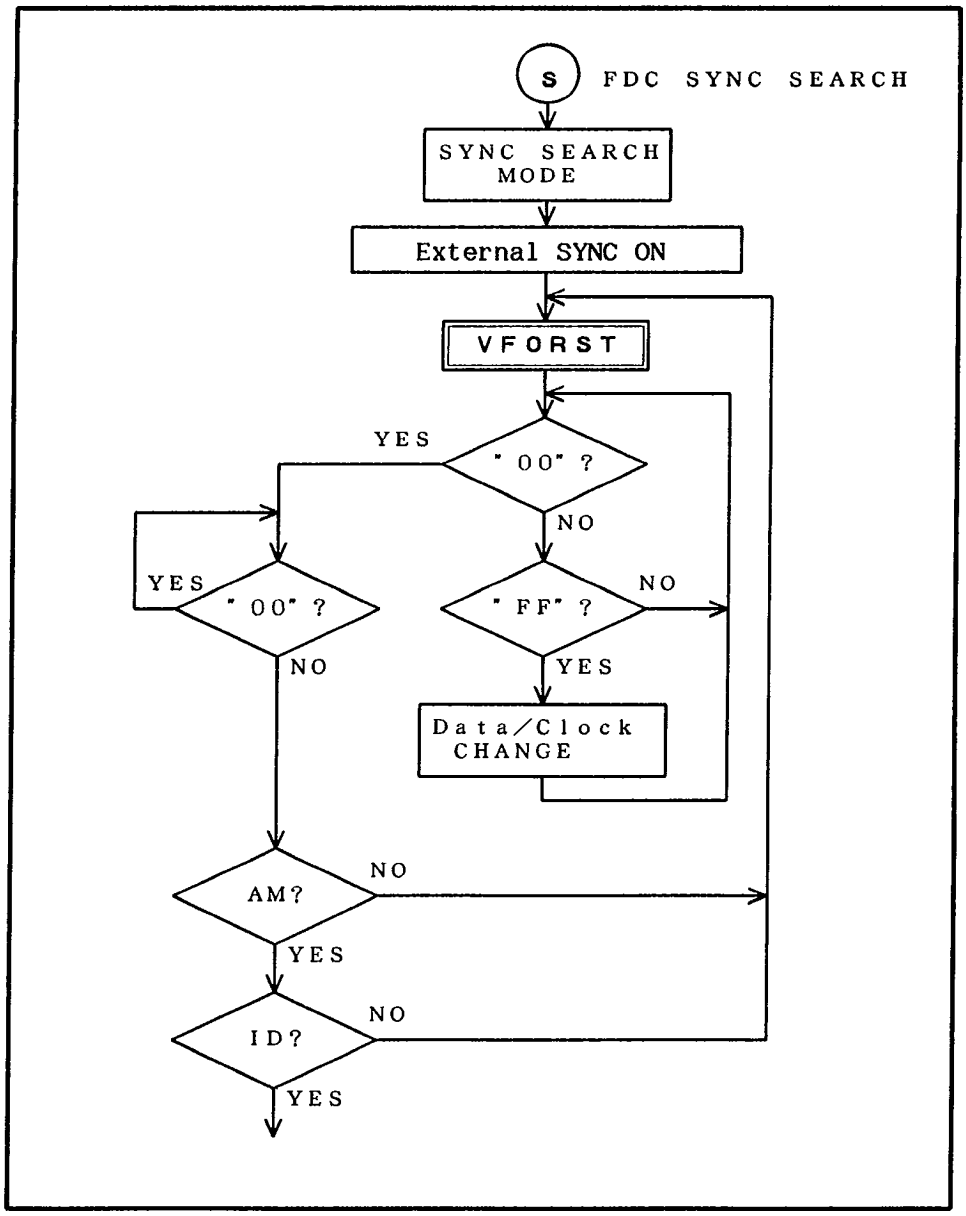


Fig.5.3.3B. VFORST Timing

5.3.4. FILTER CR CONSTANT OF VFO

When the VFO is used in 2 filter switching mode, the external components for the low pass filter are needed as follows.

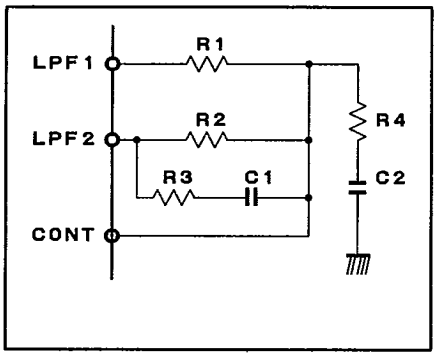


Fig.5.3.4. Filter Circuit

Recommended CR constant for MIN and STD mode is as follows. The accuracy of component is less than 5 % each.

R1	1 K OHM
R2	68 K OHM
R3	15 K OHM
R4	1 k OHM
C1	1000 pF
C2	0.01 uF

Also, when the VFO is used in 1 filter non-switching mode, the external components for the low pass filter are needed as follows.

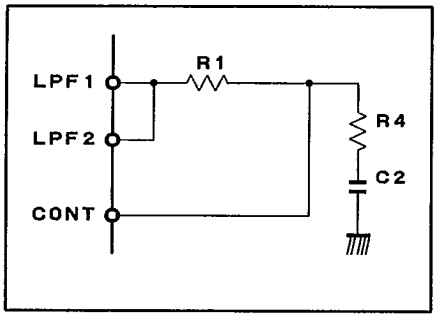


Fig.5.3.4B. Filter Circuit

FLOPPY DISK CONTROLLER

Recommended CR constant for MIN and STD mode is as follows.

R1	7.5 K OHM
R4	2.7 K OHM
C2	0.01 uF

5.3.5. VFO TIME MARGIN

(1) OUTLINE OF TIME MARGIN

Raw data being read from floppy disk drive have dynamic/static data rate variations on account of the variation in the rotational speed of disk (for example, wow flatter). On high density recording, magnetic effects cause read data to move to early or late position, which is called peak shift. Raw read data are influenced by the variation in disk speed on both writing and reading, which is regarded as low speed variation. The VFO is designed to track this variation. On the other hand, it is necessary to reduce the variation by peak shift, because its frequency is near the data transfer frequency.

Example: Waveform in case of data 6DB in MFM mode for mini-floppy

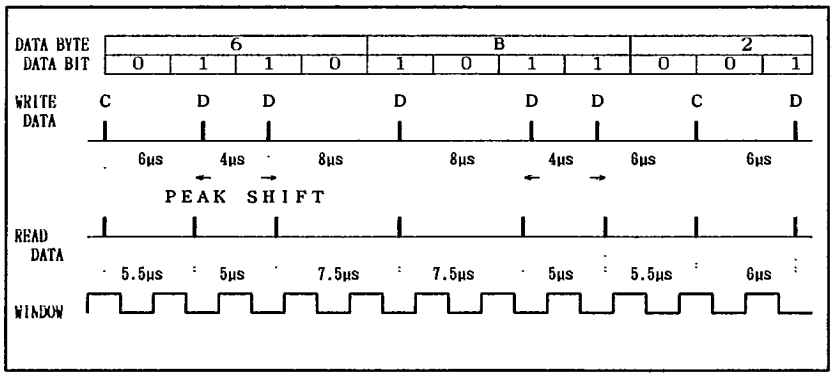
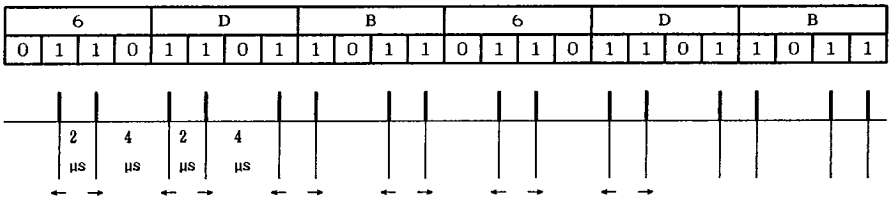


Fig.5.3.5A. Example of Peak Shift

In the example above, there are +0.5us pulse jitters by peak shift. The VFO operates to track the variation in disk rotation but to ignore the variation of this peak shift, and then generates the WINDOW signal to sample data accurately. The time margin is the tolerance for the peak shift. This value in the case of an ideal VFO is a half of the cycle of the bit transfer rate. It is 2us in MFM mode for mini-floppy (250Kbps).

(2) MEASUREMENT OF TIME MARGIN

There are many measurement methods of the time margin. We select the MFM data pattern of the repetition of 6DB (hex). Because it contains many worst-case peak shifted data in MFM mode. The MFM data pattern of the repetition of 6DB is shown below.



The measurement of the time margin is performed as follows. The FDC reads the sector data generated by the pattern generator whose data field is the repetition of 6DB above. At this time the data is shifted like peak shifted data with the bit-shift circuit of MFM data used in pre-compensation. The time margin of the VFO will be measured by researching the relation between the amount of peak shift and the read error rate of the FDC.

[RESULTS]

STD/MIN.	MFM/FM	TIME MARGIN
STD	MFM	0.76 us
	FM	1.60 us
MIN.	MFM	1.68 us
	FM	3.40 us

6. ELECTRICAL CHARACTERISTICS

6.1. ABSOLUTE MAXIMUM RATING

Vss = 0V

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	VDD	-0.5 to +7.0	V
Input Voltage	VIN	Vss-0.5 to VDD+0.5	V
Operation Temperature	topr	-40 to +85	℃
Storage Temperature	tstg	-65 to 125	℃
Output Current	IOUT1	+2.0 (*1)	mA
Output Current	IOUT2	+8.0 (*2)	mA
Output Current	IOUT3	+3.0 (*3)	mA
Power Dissipation	pd	300	mW

Comment : *1 XOUT
*2 WDT1, WE, HS, HL, MEN3 - MEN0, DS3 - DS0, STP, LC and DR.
*3 Others.

6.2. RECOMMENDED OPERATION CONDITION

Vss = 0V

ITEM	SYMBOL	MIN.	MAX.	UNIT
Operation Temperature	topr	-40	+85	℃
Power Supply Voltage	VDD	4.5	5.5	V
Clock Frequency	fo	15.5	16.5	MHz

6.3. DC CHARACTERISTICS

VDD=5.0±10% , VSS=0V , Ta=-40 ℃ to +85 ℃

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT
Hysterisis	(*3)	VHS3	0.2			V
	(*4)	VHS4	0.2			V
Input Leakage Current	(*1)	IIH1	3		10	uA
at VIH=VDD	(*3,*4,*5)	IIH345	-10		10	uA
Input Leakage Current	(*1)	IIL1	-10		-3	uA
at VIL=VSS	(*2,**)	IIL2	-70		-15	uA
	(*3,*4,*5)	IIL345	-10		10	uA
High Level Input Voltage	(*1)	VIH1	3.5		VDD	V
	(*2)	VIH2	2.2		VDD	V
	(*3,*4)	VIH34	2.4		VDD	V
	(*5)	VIH5	2.2		VDD	V
Low Level Input Voltage	(*1)	VIL1	0		1.5	V
	(*2)	VIL2	0		0.8	V
	(*3,*4)	VIL34	0		0.58	V
	(*5)	VIL5	0		0.8	V
High Level Input Current	(*6)	IOH1			-0.5	mA
at VOH=VDD-0.4V	(*7)	IOH2			-4.0	mA
	(*8)	IOH3			-2.0	mA
Low Level Input Current	(*6)	IOL1	0.5			mA
at VOL=0.4V	(*7)	IOL2	6.0			mA
	(*8)	IOL3	2.0			mA
Power Supply Current		IDD1		20	30	mA
Stand-by Current		IDD2			50	uA

Comment : *1 XIN
*2 -TEST,LOCK,-CL (Input with Pull-up)
*3 -RDT (Schimitt Trigger Input)
*4 -IDX,-RDY,-WP,-2S,-FLT,-TK0 (Schimitt Trigger Input)
*5 Other Inputs and Data Bus
*6 XOUT
*7 WDT1,WE,HS,HL,MEN3-0,DS3-0,STP,FR,LC,DR
*8 Other Outputs and Data Bus
** At VDD = 5.0V

6.4. AC CHARACTERISTICS

VDD=5.0±10% , VSS=0V , Ta=-40 ℃ to +85 ℃

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
AEN Setup time before -IOR	tAENR	0			ns
AEN Hold time after -IOR	tRAEN	0			ns
-CS Setup time before -IOR	tSR	0			ns
-CS Hold time after -IOR	tRS	0			ns
Address Setup time before -IOR	tAR	10			ns
Address Hold time after -IOR	tRA	0			ns
Data Delay time from -IOR	tRD			100	ns
Data Hold time after -IOR	tDR	20		100	ns
Pulse Width of -IOR	tRR	200			ns
AEN Hold time before -IOW	tAENW	0			ns
AEN Hold time after -IOW	tWAEN	0			ns
-CS Setup time before -IOW	tSW	0			ns
-CS Hold time after -IOW	tWS	0			ns
Address Setup time before -IOW	tAW	10			ns
Address Hold time after -IOW	tWA	10			ns
Data Setup time before -IOW	tDW	100			ns
Data Hold time after -IOW	tWD	10			ns
Pulse Width of -IOW	tWW	200			ns
INT Delay time from -IOR (*1)	tRI			500	ns
INT Delay time from -IOW (*1)	tWI			500	ns
INTRQ Delay time from -IOR (*1)	tRIR			500	ns
INTRQ Delay time from -IOW (*1)	tWIR			500	ns
DMA Cycle time (*1)	tDRQCY	13			us
DRQ Delay time from -DACK	tACDRQ			200	ns
-IOR Delay time from DRQ (*1)	tDRQR	800			ns
-IOW Delay time from DRQ (*1)	tDRQW	250			ns
-IOR/-IOW Delay time from DRQ (*1)	tDRQRW			12	us
DMA Cycle time (*1)	tDRQ2CY	13			us
DRQ2 Delay time from -DACK2	tACDRQ2			200	ns
-IOR Delay time from DRQ2	tDRQ2R	0			ns
-IOW Delay time from DRQ2	tDRQ2W	0			ns
-IOR/-IOW Delay time from DRQ2 (*1)	tDRQ2RW			11	us
Pulse Width of -DACK2 (*1)	tAA	250			ns
-DACK2 Setup time before -IOR	tACR	0			ns
-DACK2 Hold time after -IOR	tRAC	0			ns
-DACK2 Setup time before -IOW	tACW	0			ns
-DACK2 Hold time after -IOW	tWAC	0			ns
Pulse Width of DMATC (*1)	tTC	125			ns
DS Setup time before STP (*1)	tDSST	21			us
DS Hold time after STP (*1)	tSTDS	5			us
DR Setup time before STP (*1)	tDST	1			us
DR Hold time after STP (*1)	tSTD	24			us
Pulse Width of STP (*1)	tSTP		7		us

continue

FLOPPY DISK CONTROLLER

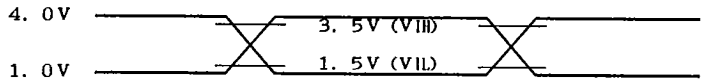
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Pulse Width of WDT	tWDD		250		ns
Pulse Width of WDT1 (*1)	tWDD1		250		ns
Low Level Pulse Width of -RDT	tRDD1	130			ns
High Level Pulse Width of RDT	tRDD2	130			ns
Pulse Width of FR (*1)	tFR	8		10	us
Pulse Width of -IDX (*1)	tIDX	250			ns

Comment

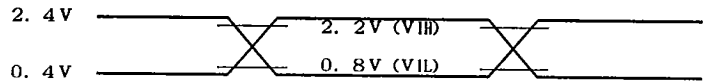
The values for 8" mode are in the above list.
The values which are marked (*1) should be doubled for mini-floppy mode.

6.4.1. AC TEST INPUT WAVE FORM

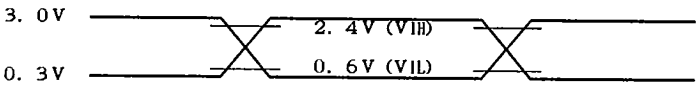
Input Terminal Group 1 : XIN Input



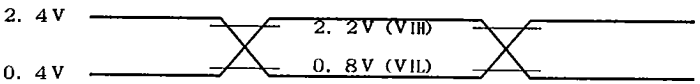
Input Terminal Group 2 : Input with Pull-up Device



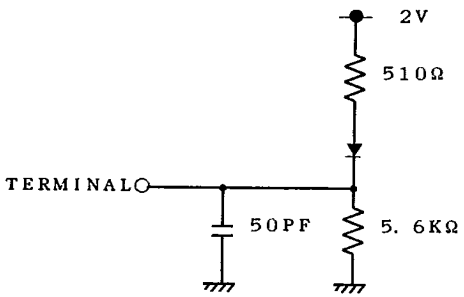
Input Terminal Group 3, 4 : Schmitt trigger



Input Terminal Group 5 : The other Input and Data Bus



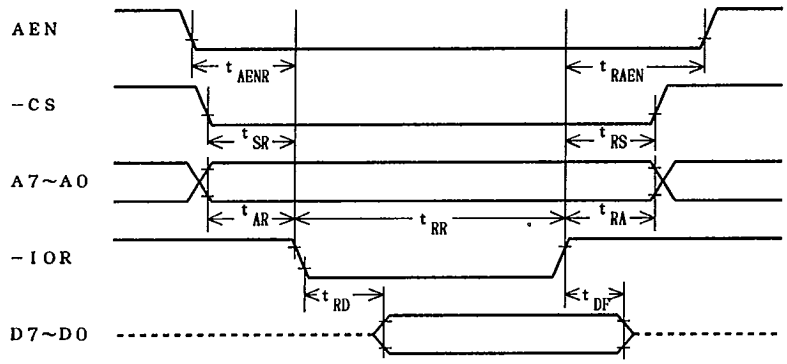
6.4.2. OUTPUT LOAD CIRCUIT



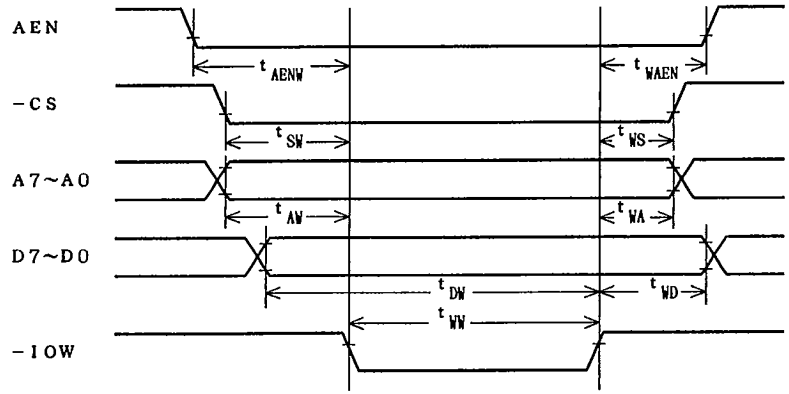
6

6.4.3. TIMING CHART

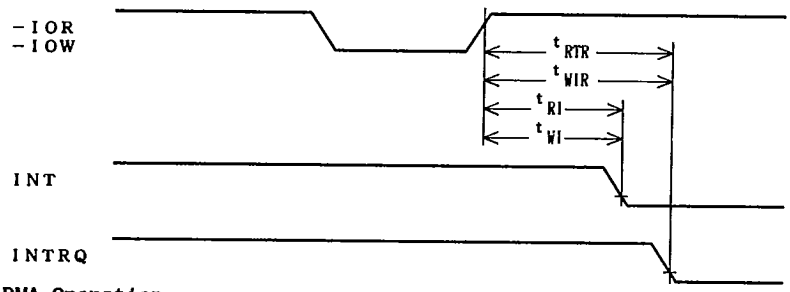
(1) Read Operation



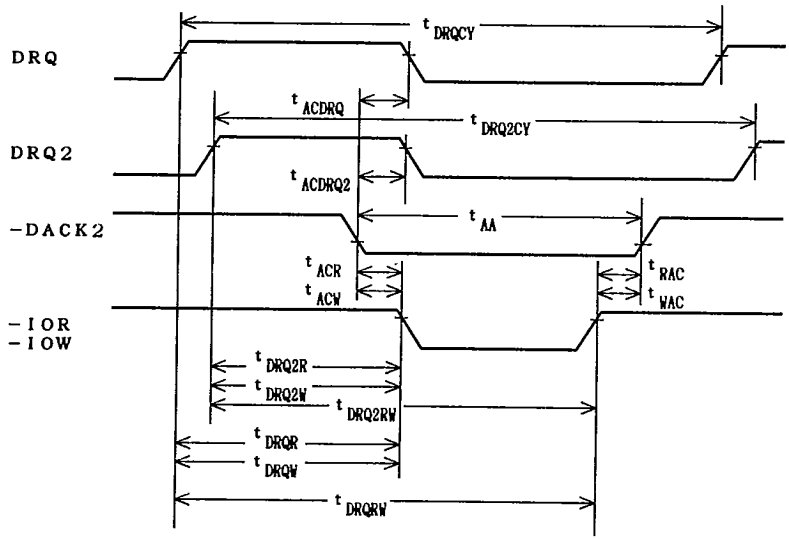
(2) Write Operation



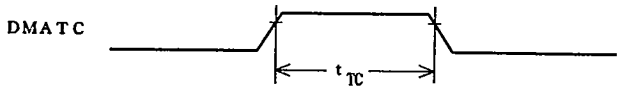
(3) Non - DMA Operation



(4) DMA Operation

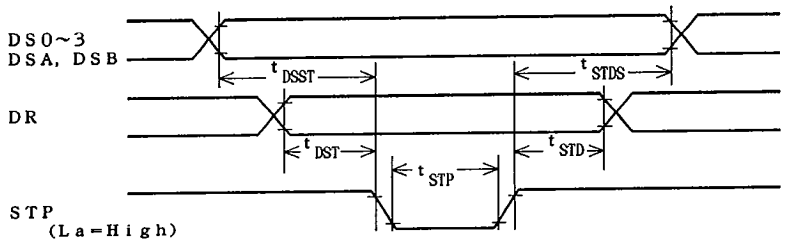


(5) Terminal Count Wave Form

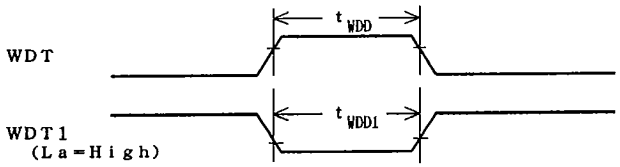


6

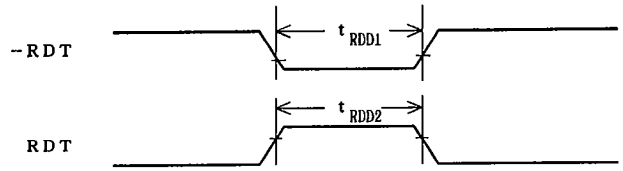
(6) Seek Operation (CDS = Low)



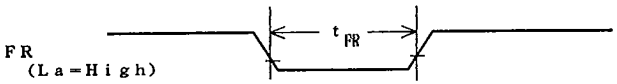
(7) Write Data Wave Form



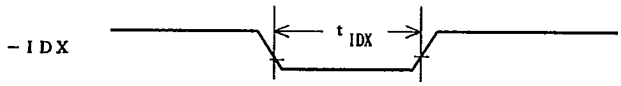
(8) Read Data Wave Form



(9) Fault Reset Wave Form



(10) Index Wave Form



FLOPPY DISK CONTROLLER

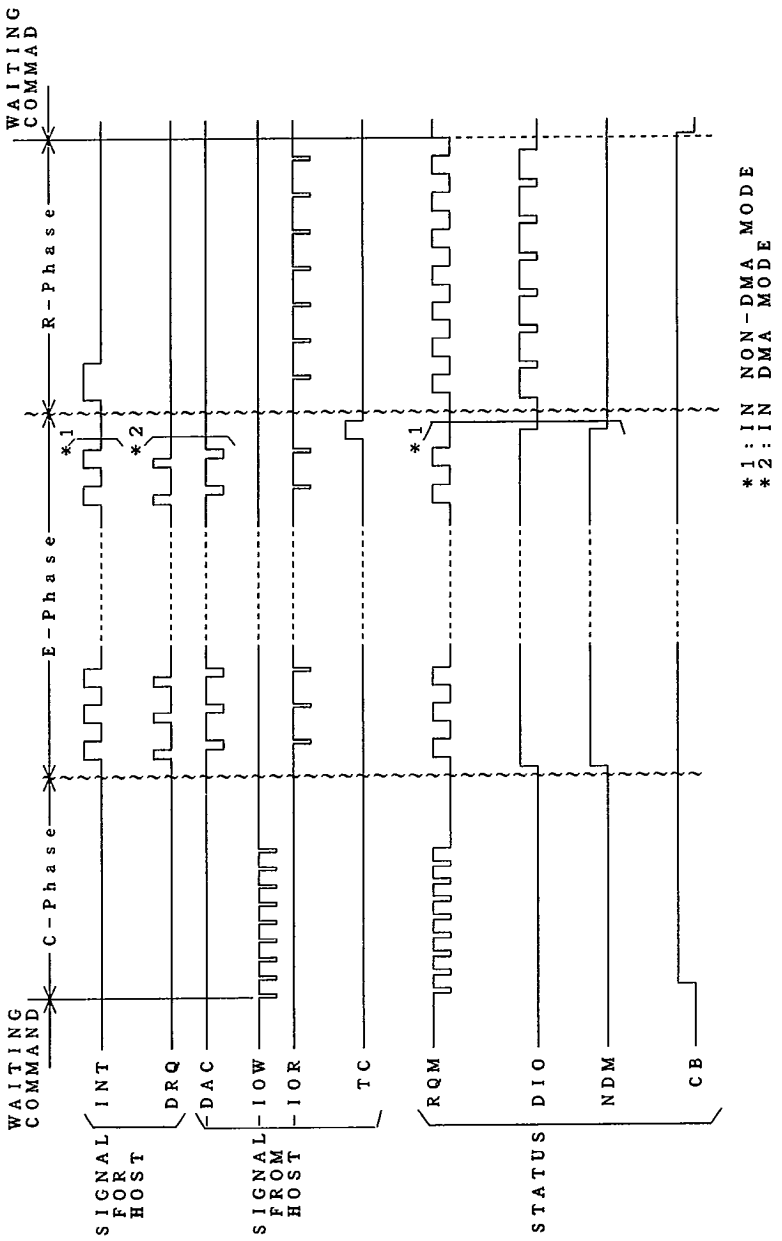
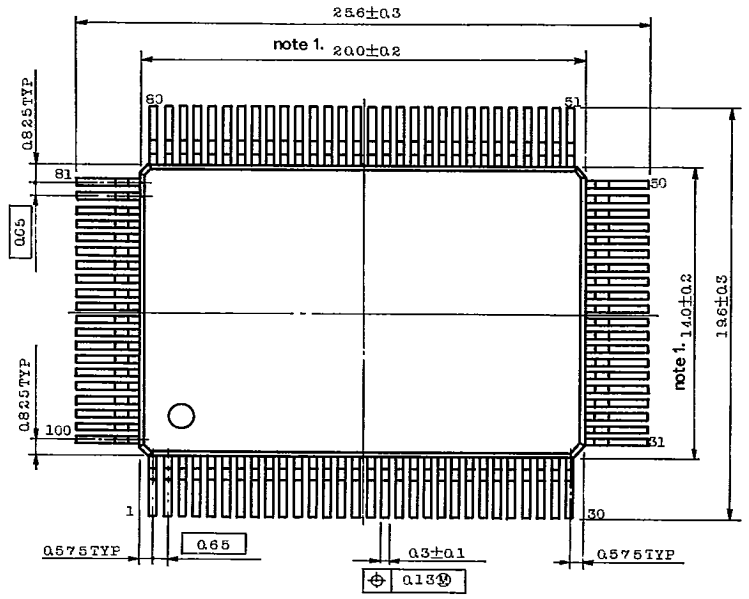
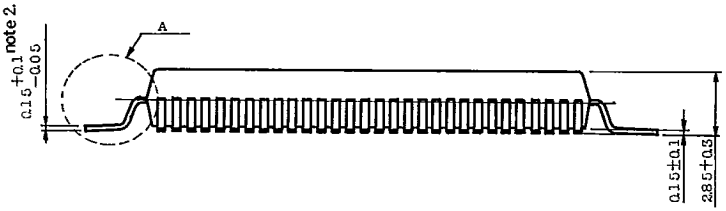


Fig.5.2.7. Operation Timings of The READ DATA COMMAND

7. PACKAGE DIMENSION

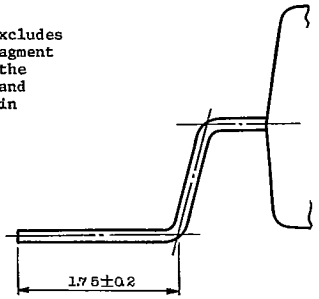
100PIN FLAT PLASTIC PACKAGE unit: mm





note 1: Outline dimension of the mold excludes of the remainder of the mold fragment and the tie-bar-cut. However, the remainder of the mold fragment and the tie-bar-cut are 0.15mm Max in each side.

note 2: Aplly to the flat part of the lead.



Detail figure of A