Bangladesh University of Engineering and Technology

BUET

Department of Computer Science and Engineering

Course No: CSE -306
Course Name: Computer Architecture Sessional

Experiment: Arithmetic Logic Unit(ALU) Design and Implementation.

Date of Submission: 20-12-2022

Group: 2
Subsection: B2
Student ID: 1905092,1905114,1905116,1905117,1905120

1. Introduction:

As part of the assignment, we first designed the algorithmic logic unit for group specified 3 selector bits. We designed and simulated the ALU in logisim software. The ALU has 3 selection bits and 2 sets of 4-bit inputs with 4 output bits and 4 flags to determine the state of the output.

2. Problem Specifications with Assigned instructions:

Group 2(B2) was assigned 6 operations for 3 selector bits which are the following:

cs2	**cs1**	**cs0**	**Functions:**	**Operations:**
X	0	0	AND	A and B
0	0	1	Sub	A-B (A+B'+1)
X	1	0	Decrement A	A-1 (A+1'+1)
0	1	1	Add with carry	A+B+1
1	0	1	NEGA	-A (A'+1)
1	1	1	Complement of A	A'

There are 2 pairs of 4-bit input and 4-bit output with 4 flags: Sign, Carry, Zero, Overflow

2. Detailed Design Steps with K-maps:

The original arithmetic logic unit has 3 selection bits and a carry input but here we have only 3 selection bits. Here we have an extra operation A'+1, so we have to do a logical + arithmetic operation on the first set of input bits for which we use an extra selector bit called A'. We will have 2 selector bits for arithmetic operations s0 and s1 and 1 selector bit called MUX for the 2*1 mux which selects between logical and arithmetic operations. We also used an extra input bit C in.

Truth Table for 3 selectors to 5 selector conversion adapter:

	A	**B**	**C**						
Operation	**cs2**	**cs1**	**cs0**	**MUX**	**s1**	**s0**	**A'**	**Cin**	**B**
AND	0	0	0	0	0	1	0	X	B
Sub	0	0	1	1	1	0	0	1	B'
Dec A	0	1	0	1	1	1	0	0	All 1
Add with Carry	0	1	1	1	0	1	0	1	B
AND	1	0	0	0	0	1	0	X	B
NEGA	1	0	1	1	0	0	1	1	All 0
Dec A	1	1	0	1	1	1	0	0	All 1
Comp A	1	1	1`	1	0	0	1	X	All 0

K map for MUX:

A	BC	00	01	11	10
0		0	1	1	1
1		0	1	1	1

K map for s1:

A	BC	00	01	11	10
0		0	1	0	1
1			0	0	1

K map for s0:

A	BC	00	01	11	10
0		1	0	1	1
1		1	0	0	1

K map for A':

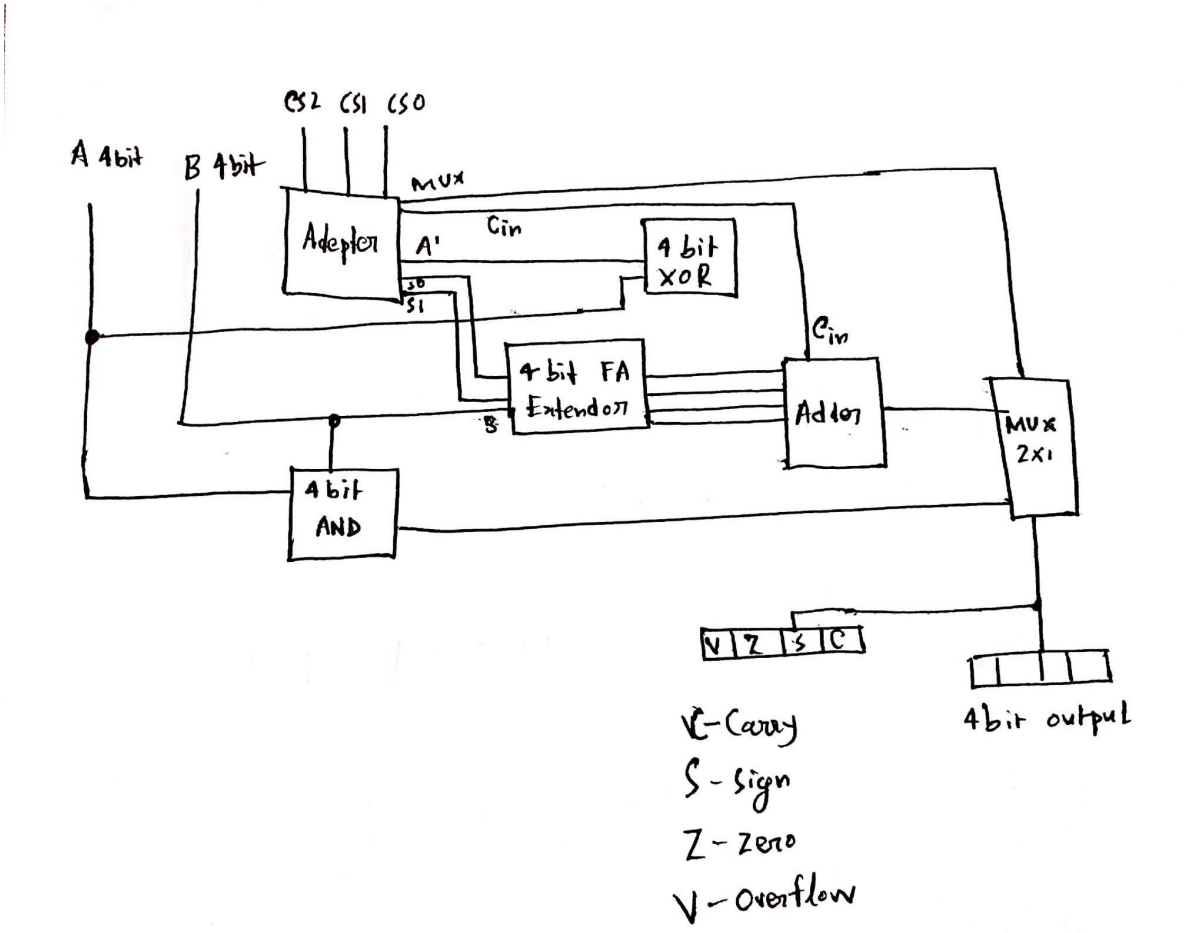
A	BC	00	01	11	10
0		0	0	0	0
1		0	1	1	0

K map for Cin:

A	BC	00	01	11	10
0		X	1	1	0
1		X	1	0	0

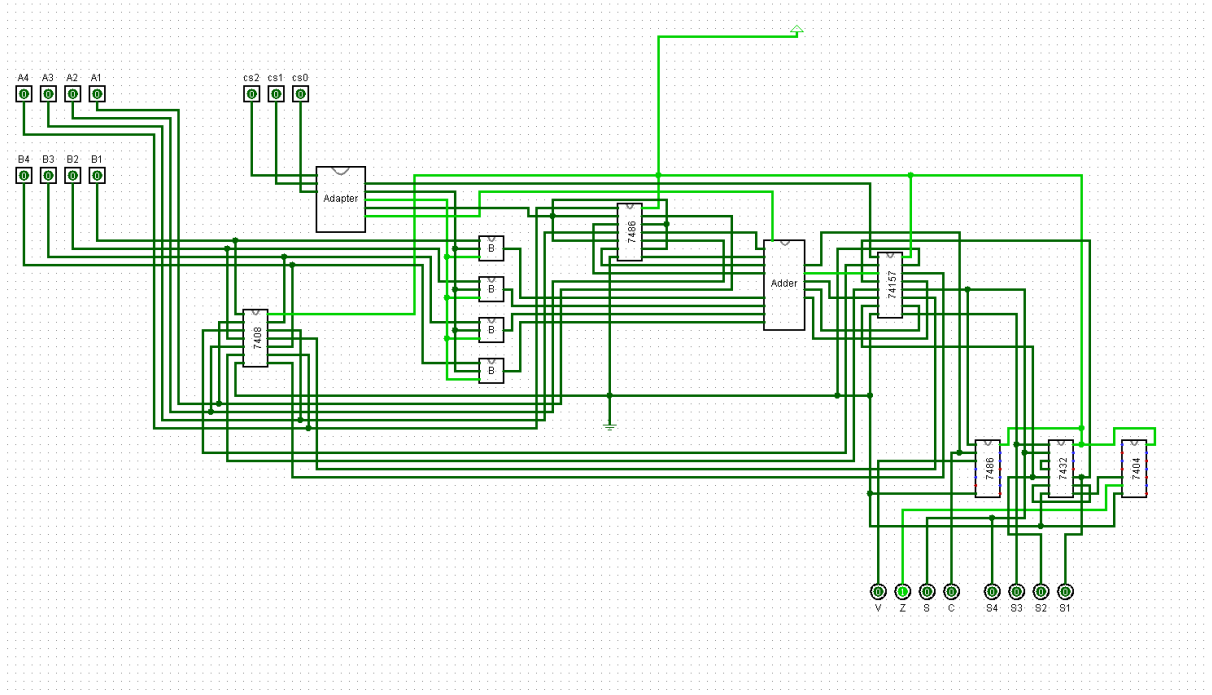
Equations:
MUX = B + C
s1 = (A+B)'C+BC'
s0 = A'B+C'
A' = AC
C in= B'+A'C

Block Diagram:

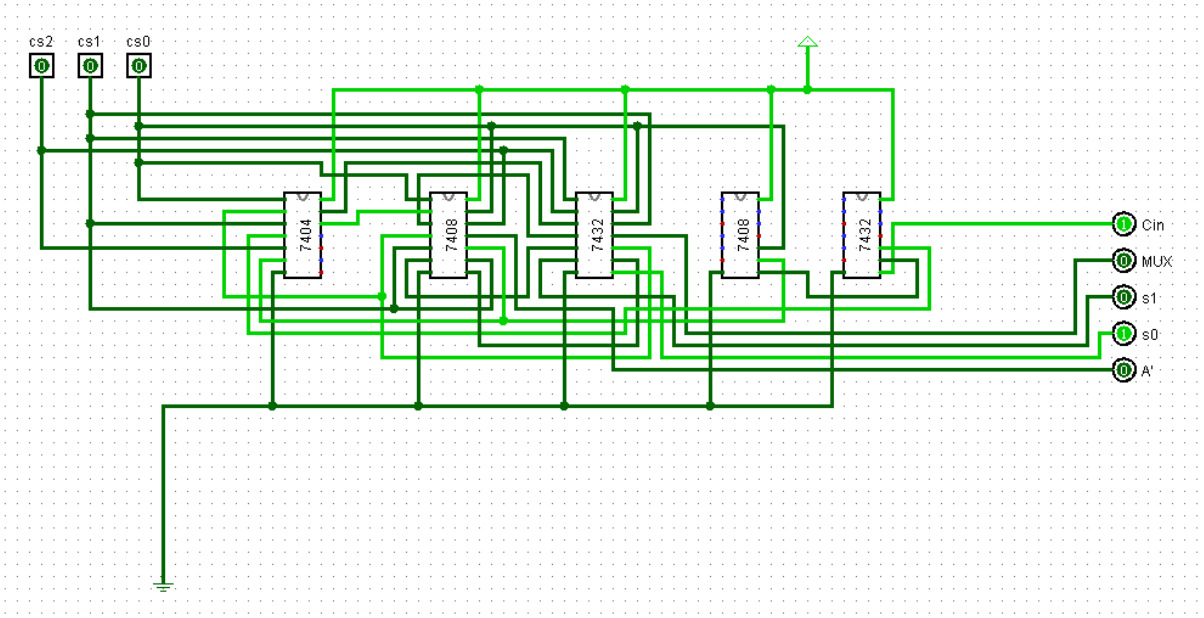


Complete Circuit Diagram:

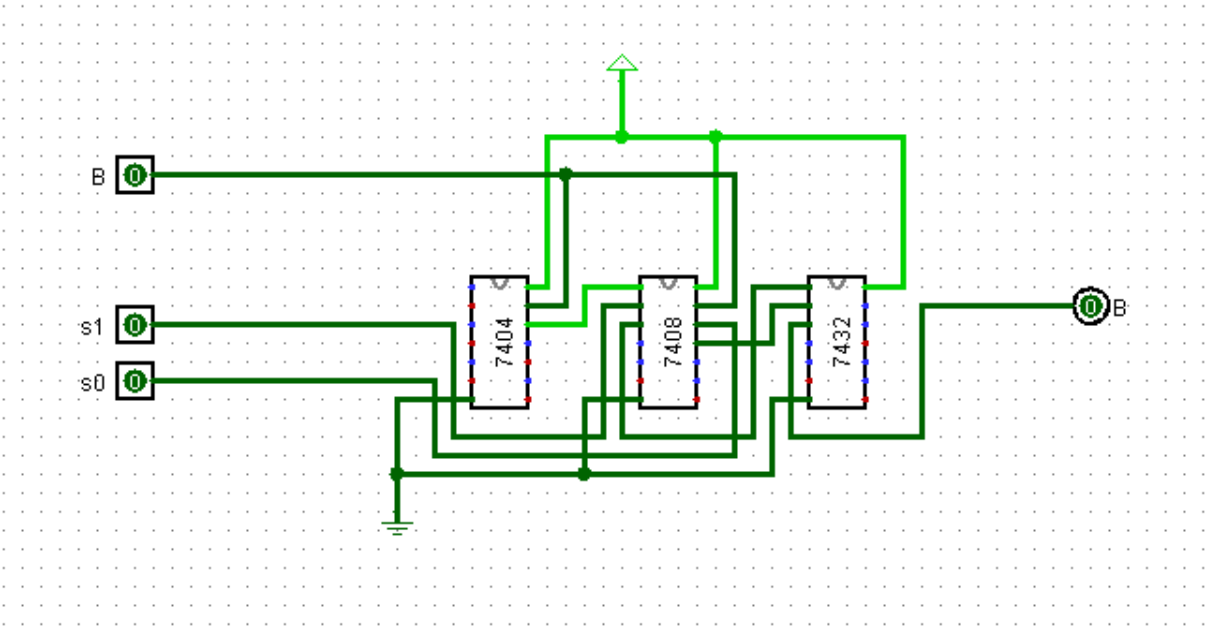
Main:



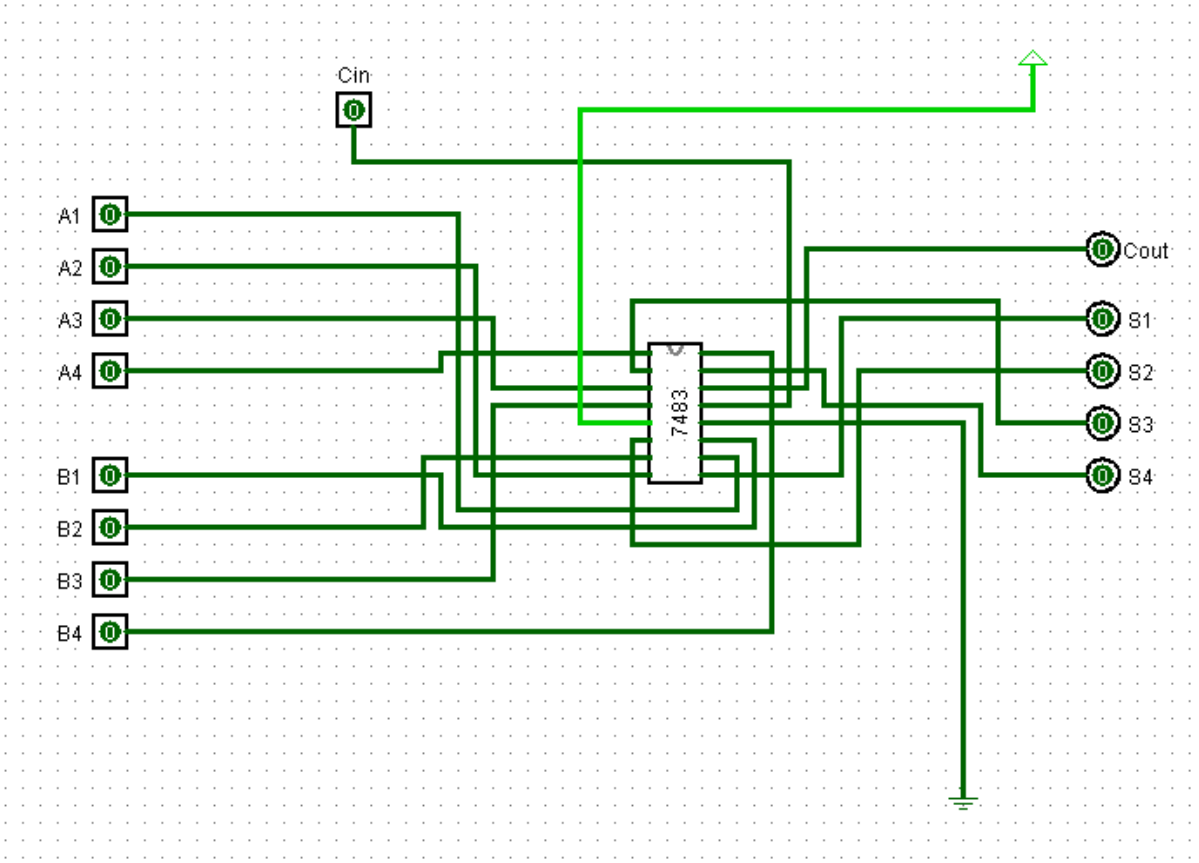
Adapter:



Full Adder Extender(B):



Adder(IC 7483):



IC used:

Name	**Number**
7404	2
7408	6
7432	3
7483	1
7486	1
74157	1
Total	**14**

Simulator Used:
Logisim-win-2.7.1 with Lib 7400

Discussion:

We used 5 V power supply as input which is distributed in the whole board. As a result voltage dropped to 2.5 V in the ICs' situated in the lower portion of the board. IC 7483 or adder requires more than 4 volt in every input to get value 1 so it shows some anomaly while running as it only gets roughly 2.5-3 V in the inputs. Every other place of the circuit works flawlessly.