
STM32
CubeMX

1. Description

1.1. Project

Project Name	WIPNAENAE
Board Name	custom
Generated with:	STM32CubeMX 6.4.0
Date	02/22/2022

1.2. MCU

MCU Series	STM32G0
MCU Line	STM32G0x1
MCU name	STM32G071RBIx
MCU Package	UFBGA64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M0+

2. Pinout Configuration

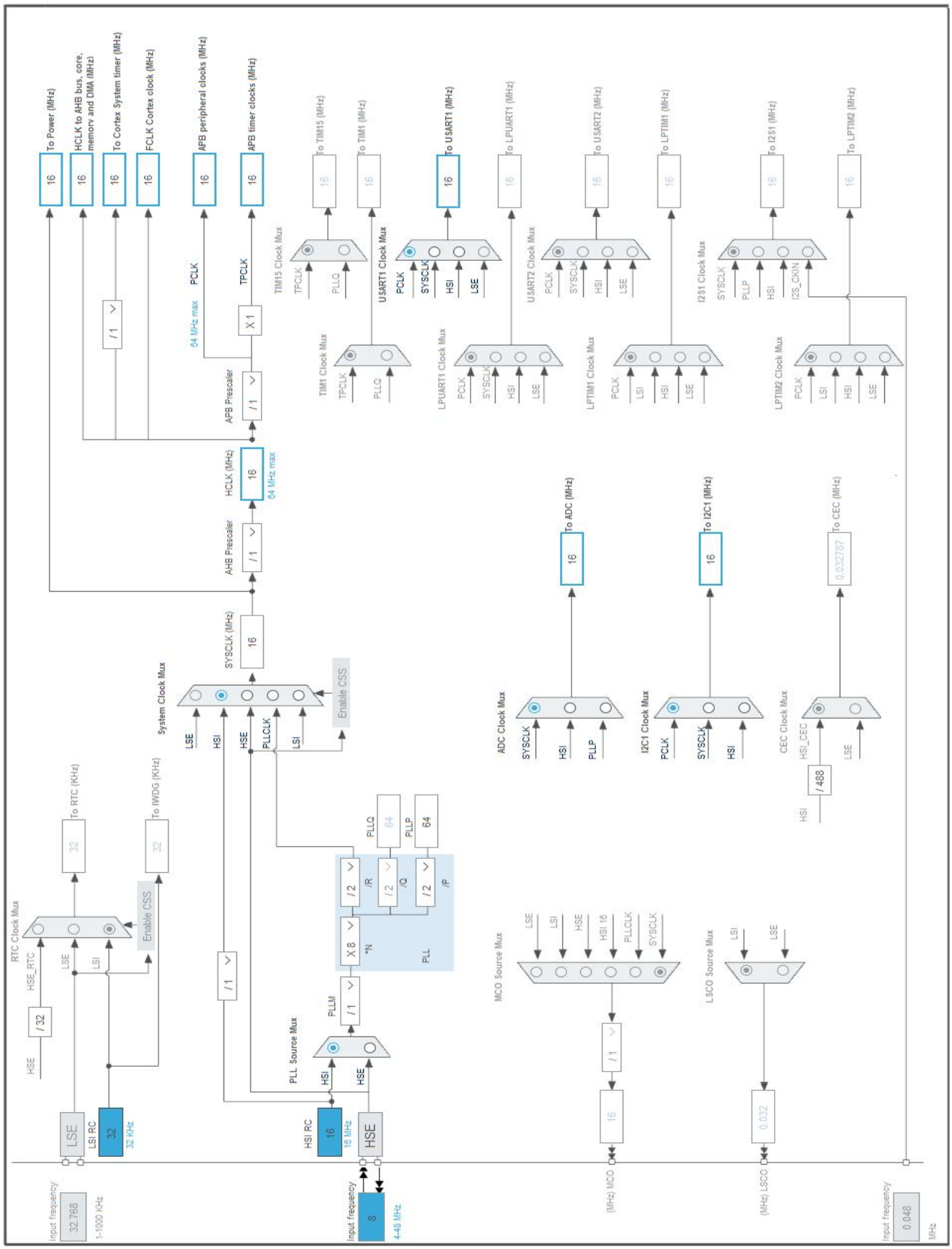
UFBGA64 (Bottom view - Rotated +90°)

3. Pins Configuration

Pin Number UFBGA64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A3	PB7	I/O	I2C1_SDA	
A4	PB6	I/O	I2C1_SCL	
B8	PA12 [PA10]	I/O	I2C2_SDA	
C6	PA15	I/O	TIM2_CH1	
C8	PA11 [PA9]	I/O	I2C2_SCL	
D1	VDD	Power		
D3	VBAT	Power		
D6	PA10	I/O	USART1_RX	
E1	VSS	Power		
E6	PA9	I/O	USART1_TX	
F1	PF0-OSC_IN (PF0)	I/O	RCC_OSC_IN	
G1	PF1-OSC_OUT (PF1)	I/O	RCC_OSC_OUT	
H2	PA0	I/O	ADC1_IN0	
H3	PA1 *	I/O	GPIO_Output	
H5	PC4 *	I/O	GPIO_Output	
H6	PC5 *	I/O	GPIO_Output	
H7	PB2 *	I/O	GPIO_Output	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	WIPNAENAE
Project Folder	C:\Users\Jonathan Martini\Desktop\stm32src
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G0 V1.5.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_I2C1_Init	I2C1
5	MX_I2C2_Init	I2C2
6	MX_USART1_UART_Init	USART1
7	MX_TIM2_Init	TIM2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G0
Line	STM32G0x1
MCU	STM32G071RBIx
Datasheet	DS12232_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(AAA700)
Capacity	700.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	10.0 mA
Max Pulse Current	30.0 mA
Cells in series	1
Cells in parallel	1

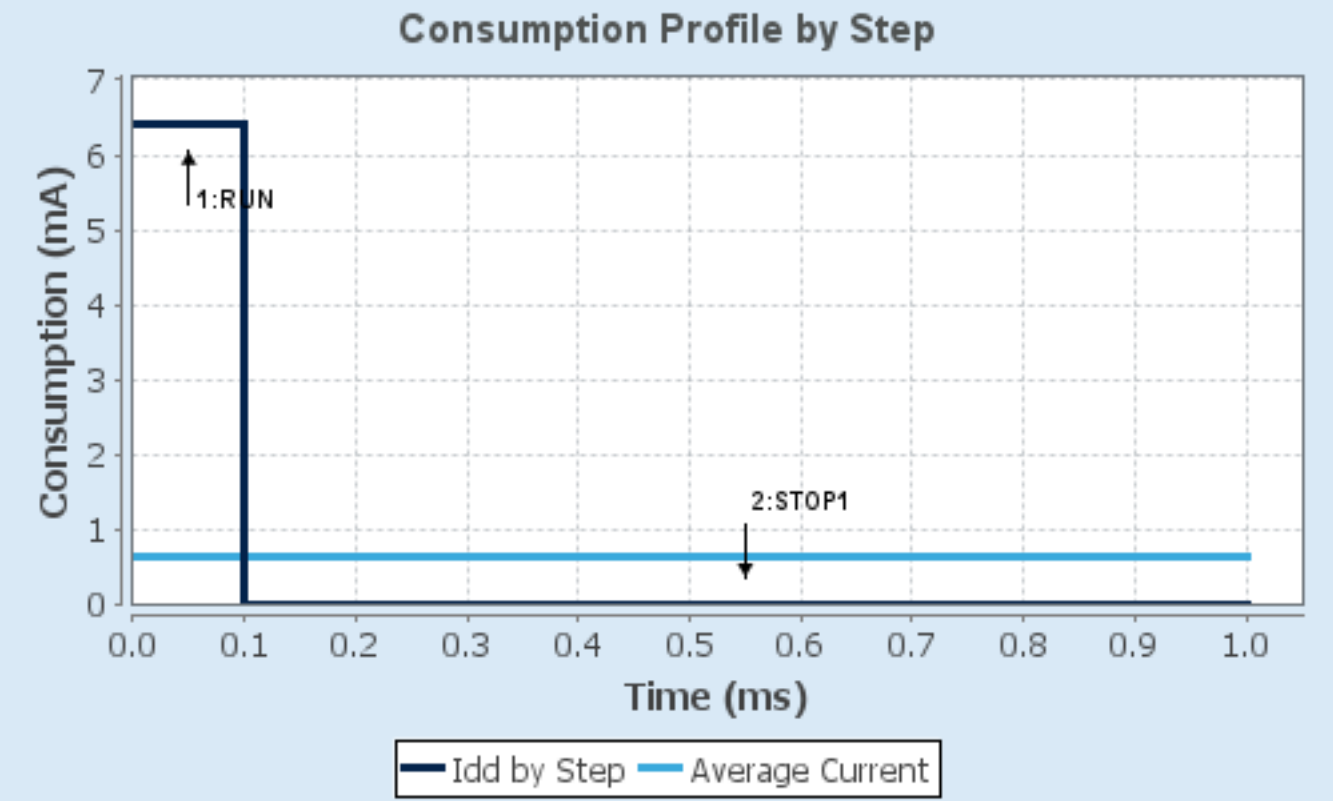
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	Flash-PowerDown
CPU Frequency	64 MHz	16 MHz
Clock Configuration	HSI PLL	HSI
Clock Source Frequency	16 MHz	16 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	6.4 mA	3.4 µA
Duration	0.1 ms	0.9 ms
DMIPS	80.0	0.0
Ta Max	128.54	130
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	643.06 µA
Battery Life	1 month, 14 days, 21 hours	Average DMIPS	80.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
7
6
5
4
3
2
1
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN0

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 2
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Sequencer	Sequencer set to fully configurable
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled
Auto Off	Disabled
Oversampling Mode	Disabled

ADC_Regular_ConversionMode:

SamplingTime Common 1	1.5 Cycles
SamplingTime Common 2	1.5 Cycles
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Trigger Frequency	High frequency
Rank	1
Channel	Channel 0
Sampling Time	Sampling time common 1

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00303D5B

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.3. I2C2

mode: I2C

7.3.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00303D5B

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.5. SYS

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.6. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.7. USART1

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PA12 [PA10]	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PA11 [PA9]	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PF0-OSC_IN (PF0)	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT (PF1)	RCC_OSC_OUT	n/a	n/a	n/a	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	3	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, COMP1 and COMP2 interrupts (COMP interrupts through EXTI lines 17 and 18)	unused		
TIM2 global interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C2 global interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		

8.3.2. NVIC Code generation

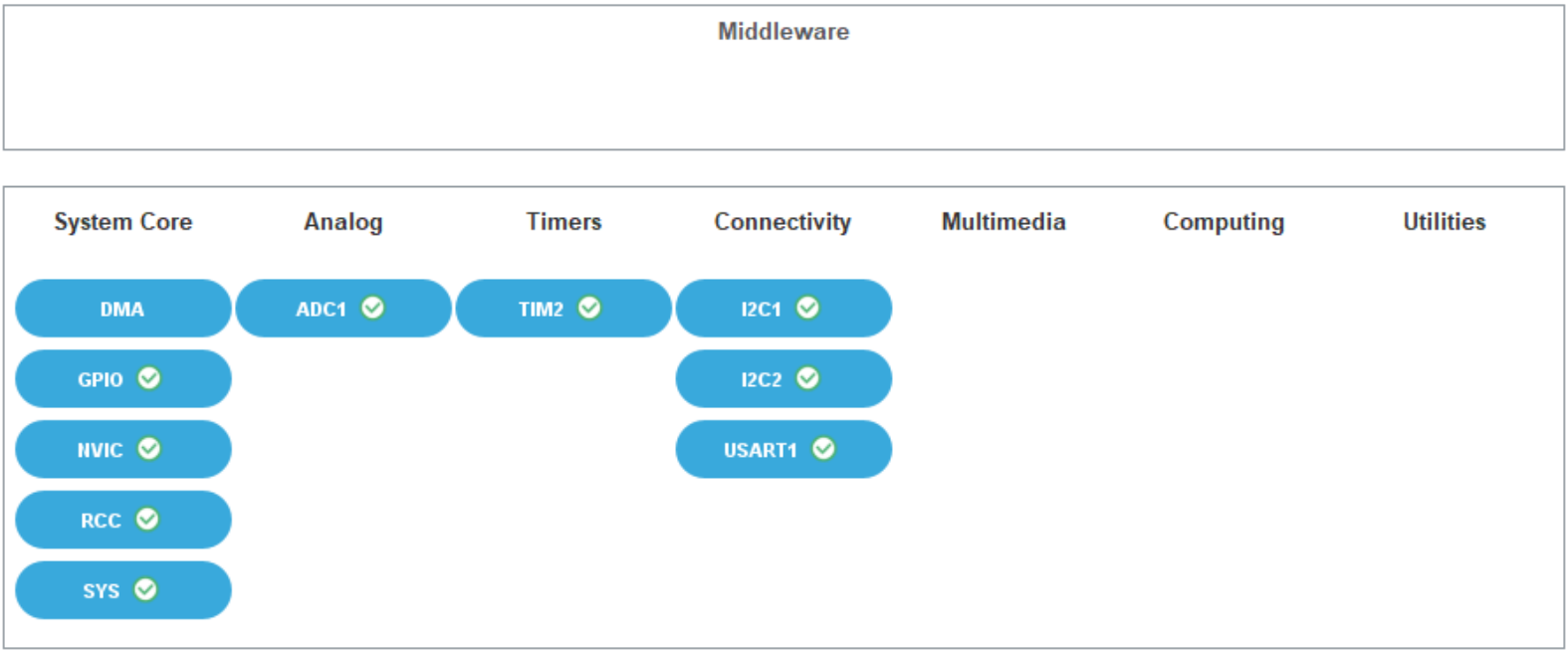
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00412180.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00371828.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00104451.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00463881.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00311483.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
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