# CadPack

## Import from Veribest-Expedition PCB

Software tool for import part/net list from Veribest-Expedition PCB

### Technical Info

**Version : 2**
**Code : 81190419.152**


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# Contents

# Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The Import from Veribest CAD import driver enables to import the data present in the Veribest CAD file and convert them in the SPEA Board data format.

***Conventions, symbols and abbreviations***

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.



This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

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# 1. Veribest file data

With the “Veribest CAD files” words we refer to the output information generated by the Veribest CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Veribest CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movements for Flying Probes).

Information can be grouped in 4 different categories and typically concern the printed circuit:

| **Part List** |
| --- |
| It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc. |
| **Net List** |
| It is also called wiring list, containing device interconnection data; basically it is presentation of the electrical diagram. |
| **Coordinate and access list** |
| It is the list containing the devices coordinates, concerning their barycentre and pins. |
| **Wiring and Routing list** |
| It is the list containing the path of the Net tracks in the PCB. |

For the import of the information above mentioned SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

## 1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

| Information | Description |
|---|---|
| **Drawing Reference** | Reference designator (e.g. U10, R105, D23, etc.). |
| **Part Number** | Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.). |
| **Value** | Device value (e.g. 10KΩ, 10µF, 1mH, etc.). |
| **Tolerance** | Positive and negative device tolerances (e.g. 1%, 5%, etc.). |
| **Mounting side** | The legal values for this item can be:<br>- **Top** (Component side)<br>- **Bottom** (Soldering side)<br>- **Not mounted Top**<br>- **Not mounted Bottom** |
| **Rotation** | Device mounting rotation angle (e.g. 0°, 180°, etc.). |
| **Dimensions** [1] | Device dimensions. |
| **Case code** | Device package (case) code. |

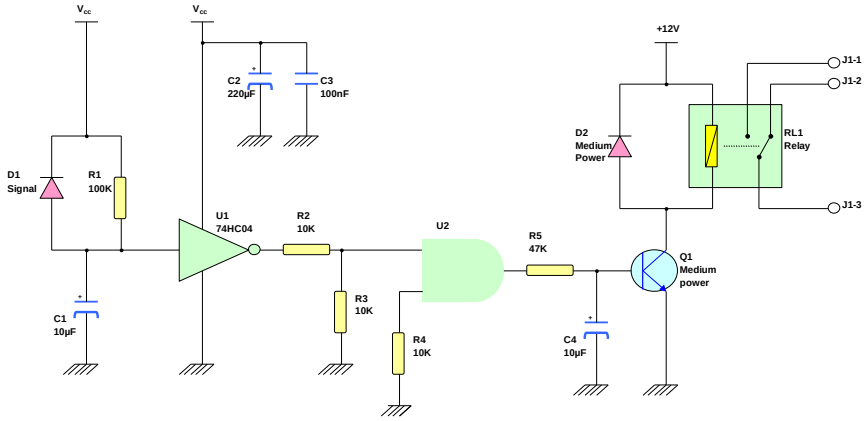
[1] **Optional data (not yet managed)**

## 1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

| Information | Description |
|---|---|
| **Net name** | Net identifier (e.g. +5V, RESET, A01, etc.). |
| **Drawing reference** | Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.). |
| **Pin name** | Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.). |
| **Pin access side** | Access side for the device pin, legal values are:<br>- **Top** (Device side access).<br>- **Bottom** (Soldering side access).<br>- **Not accessible**<br>- **All** (both top and bottom side access) |



## 1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

| Information | Description |
|---|---|
| **Drawing Reference** | Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.). |
| **Pin name** | Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.). |
| **Pin X position** | Pin X-coordinate. |
| **Pin Y position** | Pin Y-coordinate. |
| **X barycentre** [1] | Device X barycentre. |
| **Y barycentre** [1] | Device Y barycentre. |

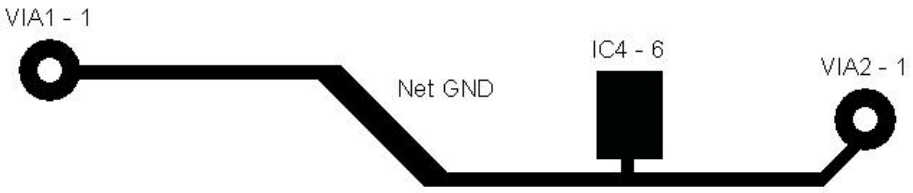
## 1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

| Information | Description |
|---|---|
| **Net name** | Net identifier (e.g. +5V, RESET, A01, etc.). |
| **X Start** | Track segment start X-coordinate. |
| **Y Start** | Track segment start Y-coordinate. |
| **X End** | Track segment end X-coordinate. |
| **Y End** | Track segment end Y-coordinate. |
| **Width** | Net segment thickness. |
| **Layer** | Layer the segment belongs to. |

Example:




[1] **Optional data**

# 2. Veribest file generalities

## 2.1 Veribest Layout file name

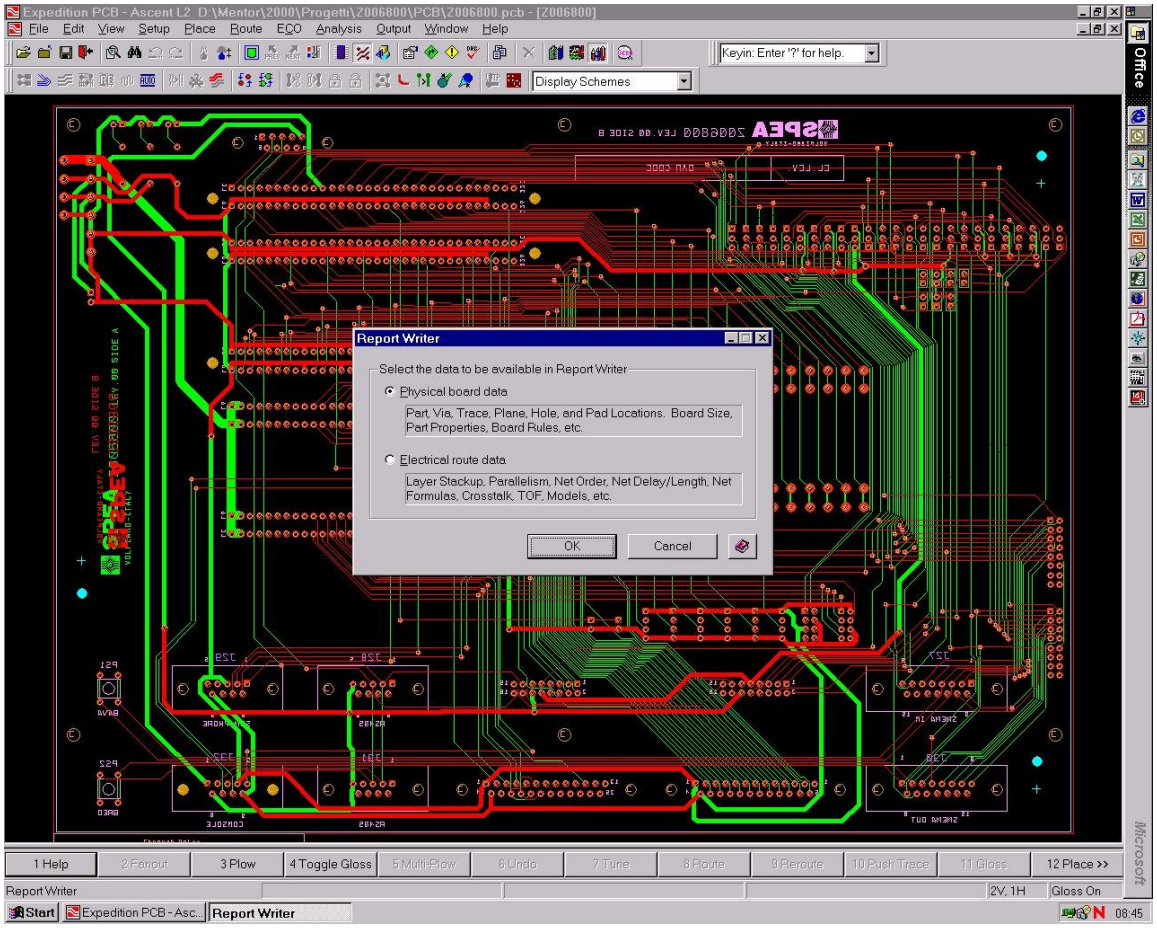
The Veribest file name has to have the ***.MDB** or ***.MDC** extensions.

It is a Microsoft® Access data base and it contains the information concerning the board, component and their connections.

## 2.2 Extracting Veribest file

The ***.MDB** or ***.MDC** files can be generated by executing the following operations:

1. Select **Output > Report Writer** to display the **Report Writer** window.
2. Select the **Physical board data** option and click **Ok** button.



# 3. Import setting

The options to be checked and/or modified are listed below.

| Cad Type | Category | | Description |
|---|---|---|---|
| **VERIBEST** | Options | Cad file version | Selects the Cad file version. |
| | | Net Name for NOT Connected Pins | Indicates how to name the nets connected to non-connected pins. |

## 3.1 Pin function assignment

This assignment table must be filled, in order to correctly execute the CAD file import.

In order to correctly test some polarized devices such as diodes, bipolar transistors, etc., it is basic to correctly identify the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table, are described below:

| Field | Description |
|---|---|
| **Device Type** | Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.). |
| **Pin Function** | Function concerning the Pin. |
| **Pin Name** | Pin reference. |
| **Cad Pin** | Pin reference in Cad file. |

## 3.2 Drawing ref. initials/device type assignment

The Veribest file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the point of view of the test program generation.

The fields contained in the table are described below:

| Field | Description |
|---|---|
| **Drawing Reference** | Initial letter identifying the **Device Type**. |
| **Device Type** | Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.). |
| **Default Tol+, Tol-** | Value and tolerance of the device only if required (as for resistors). |

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.