CadPack

Import from Pads

Software tool for import part/net list from Pads

Technical Info

Version : 2
Code : 81190412.096

SPEA SpA
16, Via Torino
10088 Volpiano - Italy
Tel.: + 39 011 9825 400
Fax: + 39 011 9825 405
E-mail: info@spea.com
Web: www.spea.com

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Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The Import from Pads software tool converts the CAD files of the board from the Pads format to the SPEA board data format.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

SPEA SpA
Ufficio Documentazione
16, Via Torino
10088 Volpiano – Italy
Tel.: +39 011 9825400
Fax: +39 011 9825405
Email: info@spea.com
Web: www.spea.com

1. Pads file data

With the “Pads CAD files” words we refer to the output information generated by the Pads CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Pads CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movement for Flying Probes).

Information can be grouped in 4 different categories and typically concern the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is presentation of the electrical diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information above mentioned SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List, all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: - **Top** (Component side) - **Bottom** (Soldering side) - **Not mounted Top** - **Not mounted Bottom**
Rotation [1]	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code [1]	Device package (case) code.

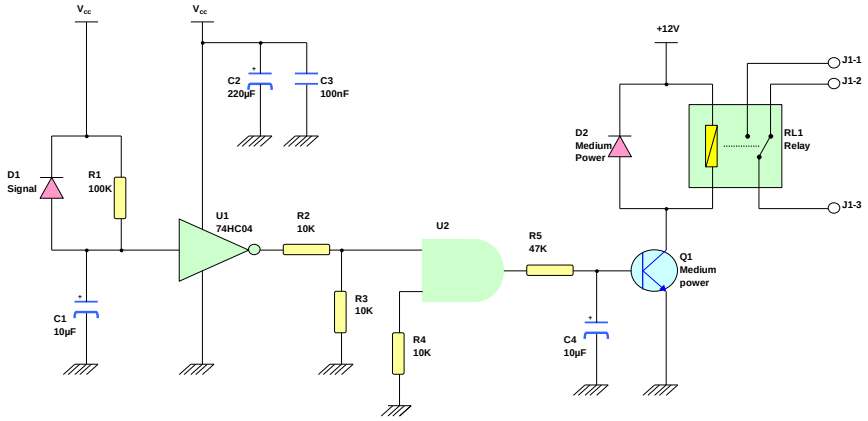
[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: - **Top** (Device side access). - **Bottom** (Soldering side access). - **Not accessible** - **All** (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

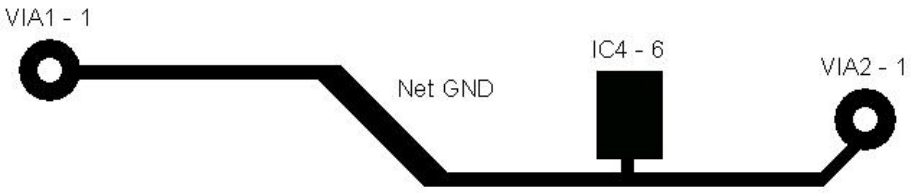
1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



[1] **Optional data**

2. Pads file generalities

The Pads required file is: **<FileName>.ASC**

Containing the Part list and the Net list.

The SPEA system is based on a PC platform operating in MS-Windows environment.

The files need to be stored into a directory defined by the user.

The SPEA Import from Pads software tool can retrieve the Pads file from each defined disk and directory.

3. Pads file format

The Pads files listed below are a significant example of the format that the file must have to be converted into SPEA format.

```
!PADS-POWERPCB-V3.0-MILS! DESIGN DATABASE ASCII FILE 2.0
*PCB*        GENERAL PARAMETERS OF THE PCB DESIGN"

.
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*PART*       ITEMS

*REMARK*  REFNM  PTYPENM  XLOC YLOC ORI GLUE MIRROR  NMXLOC NMYLOC NMORI =
ALT

SF1     FH320FC320R 1200  1300  180.0 U N 900  50   270.0 0 -1 0          Drawing reference
SF2     FH320FC320R 1200  850   180.0 U N 900  50   270.0 0 -1 0
D1      P6KE400C    1050  1950  180.0 U N 350  25   180.0 0 -1 0          Part number
D2      P6KE400C    1050  1700  180.0 U N 350  25   180.0 0 -1 0
D3      P6KE400C    1050  2200  180.0 U N 350  25   180.0 0 -1 0          Component barycenter
FR1     FN405       475   3425  180.0 U N -225 350  180.0 0 -1 0
FR2     BNX00201    5000  1900  180.0 U N -25  125  180.0 0 -1 0
PD1     W04G        4050  1900  180.0 U N 175  125  180.0 0 -1 0          Rotation
C1      037,2200UF/35V,+-20% 4550  1900  270.0 U N 175  -50   90.0 2 -1 0
T1      44272@MYRRAEI48A 5175  3475  180.0 U N 550  550  180.0 0 -1 0
SF3     FH320FC320R 5525  1400  270.0 U N 1100 -75   90.0 0 -1 0          Mounting side. N=Top, M=Bottom
F3      F1,1A       5525  1400  270.0 U N 800  -50   90.0 0 -1 0
C2      489D,1UF/35V,+/-20% 5175  1275   90.0 U N 75   50   270.0 0 -1 0
U21     7824        2665  652   270.0 U N 25   -375  90.0 0 -1 0
R1      MRS25,249,+-1%/50/100PPM 3700  1400    0.0 U N 150  -25    0.0 2 -=
C5      037,2200UF/35V,+-20% 2175  1700  270.0 U N 175  -50   90.0 2 -1 0
FR4     BNX00201    2625  1650  180.0 U N -25  125  180.0 0 -1 0
SF5     FH320FC320R 3450  1425  270.0 U N 1100 -75   90.0 0 -1 0

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*ROUTE*

*REMARK*  *SIGNAL*  SIGNAME WIDTH SIGFLAG RTRWDTH RTCLR LVL
*REMARK*  REFNM.PIN REFNM.PIN RFLAG FIXFLAG FLAG
*REMARK*  XLOC YLOC [VIATYPE]LAYER SEGMENTWIDTH

*SIGNAL* $$$7317 24 0 0 0 -2                                              Net name
U6.3      U6.8      R 0 20
17425  1850   2 24 0                                                      Coordinates of DrawingRef1-Pin1
17425  1775   2 24 0
17450  1750   2 24 0
17900  1750   2 24 0
17925  1775   2 24 0
17925  1850   31 24 0                                                     Coordinates of DrawingRef1-Pin1
U7.11     U6.8      R 0 20                                                DrawingRef1-Pin1 and DrawingRef2-Pin2
18425  2150   1 24 0
18425  2375   2 24 0 STANDARDVIA
18425  2450   2 24 0
18400  2475   2 24 0
18125  2475   2 24 0
18025  2375   2 24 0
17875  2375   1 18 0 STANDARDVIA                                          Via identifier
17875  2100   1 18 0
17925  2050   1 24 0
17925  1850   31 24 0
```

```
*SIGNAL* $$$5059 75 0 0 0 -2
T3.1      FR1.1     R 0 20
3125   3425   2 75 0
3125   3750   2 75 0
550    3750   2 75 16384
475    3675   2 75 16384
475    3425   31 75 0

*TESTPOINT*

*REMARK* PIN XLOC YLOC SIDE SIGNAME REFDES.PIN
PIN   6090    1050    0   WBDA       P1.1
PIN   5890    1950    0   WWAS       P1.2
PIN   6090    1950    0   GND1       P1.3
PIN   5890    3850    0   GND2       P1.6
PIN   6090    2850    0   ADD1       J1.8
PIN   5890    1750    0   ADD2       J1.9
PIN   6090    1750    0   ADD3       J1.7
PIN   6090    1550    0   GNDA       J1.3
PIN   6090    1550    0   N12        J1.1
PIN   4840    1010    0   VCC        IC3.1
*REMARK* TEST POINTS ON VIAS
*REMARK* VIA XLOC YLOC SIDE SIGNAME SYMBOLNAME
VIA   1070     300    0   INP        STANDARDVIA
VIA   1070     500    0   INP2       STANDARDVIA
```

PIN — Pin identifier

Coordinates

VIA — Via Test point identifier

Net name

```
ATTRIBUTE VALUES
{
PART C52
{
WERT 100N
EDV-NUMMER 000.710.064
BEZEICHNUNG SMD Chip-Kondensator
BAUFORM 1206/X7R
LIEFERANT#1 Rutronik
BEST-NR AN 1206 X7R 100N 63V
PREIS
}
PART C54
{
WERT 100N
EDV-NUMMER 000.710.064
BEZEICHNUNG SMD Chip-Kondensator
BAUFORM 1206/X7R
LIEFERANT#1 Rutronik
}
```

ATTRIBUTE VALUES — Begin of attribute value section

WERT 100N — WERT or VLAUE are the identifier used to extract the component value

4. Import setting

4.1 Pin function assignment

In order to correctly execute the CAD file import, this assignment table must be filled.

In order to test correctly some polarized devices such as diodes, bipolar transistors, etc., it is basic to correctly identify the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table, are described below:

Field	Description
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Pin Function	Function concerning the Pin.
Pin Name	Pin reference.
Cad Pin	Pin reference in Cad file.

4.2 Drawing ref. initials/device type assignment

The Pads file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the test program generation point of view.

The fields contained in the table are described below:

Field	Description
Drawing Reference	Initial letter identifying the **Device Type**.
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Default Tol+, Tol-	Value and tolerance of the device only if required (as for resistors).

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.

5. Component Properties Identification

The ATPG Software of the SPEA Systems requires to identify the following data for each component:

Passive Components:

- **Component Family**
- **Part Number**
- **Component Value**
- **Tolerance + and -**

Other Components:

- **Component Family**
- **Part Number**
- **Device Name** (commercial name)

The **Component Family** is not specified in the Part List file so it is necessary to fill a table containing the assignment between Drawing Reference initials and Component Family and the CAD Type before executing the import process.

The table contains also the default tolerance for the specified family of the components.

Example:

Device Type	Drawing. ref. initials	Default Tol+	Default Tol-
Capacitor	C	20	20
Resistor	R	10	10
Connector	J		
Digital IC	IC		

For polarized components such as diodes, it is important to identify the pin function (e.g. Anode) of each pin.
Before running the import it is required to edit the pin Id/pin function table.

Example:

Device Type	Pin Function	Pin Id
Diode	Anode	1
Diode	Cathode	2
Polarized Capacitor	Positive	1
Polarized Capacitor	Negative	2

6. Component properties default value

The SPEA Import software automatically assigns a default value if all or part of the component properties are not available in the CAD file.

In this case a further manual ending can be done to perform the necessary modifications by using the Board Data editor.

The default values are shown in the following table:

Property	Default Value
Component Family	Not identified
Value of component	0
Tolerance	0
Device Name	None