CadPack

Import from Cadif

Software tool for import part/net list from Cadstar, Visula, Zuken

Technical Info

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Introduction

CAD files are the base for the automatic generation of test programs for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The Import from Cadif software tool converts the CAD files of the board from Cadstar/Visula/Zuken format to SPEA board data format.

The Cadif format is the standard output for Cadstar, Visula and Zuken.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

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1. Cadif file data

With the “Cadif CAD files” words we refer to the output information generated by the Cadif CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Cadif CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movement for Flying Probes).

Information can be grouped in 4 different categories and typically concern the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is presentation of the electric diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information mentioned above, SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: - **Top** (Component side) - **Bottom** (Soldering side) - **Not mounted Top** - **Not mounted Bottom**
Rotation [1]	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code [1]	Device package (case) code.

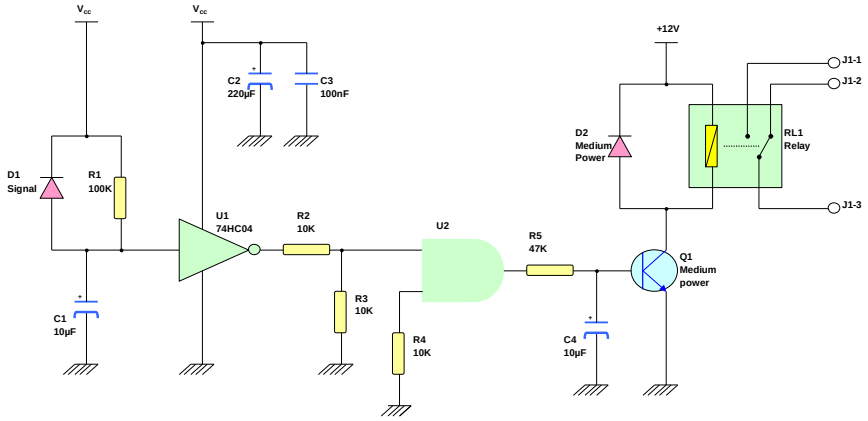
[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: - **Top** (Device side access). - **Bottom** (Soldering side access). - **Not accessible** - **All** (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

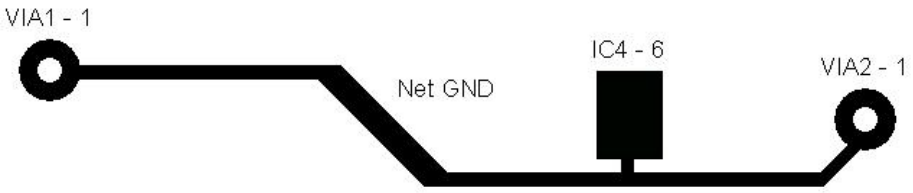
1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



[1] **Optional data**

2. Cadif file generalities

2.1 Cadif file name

The Cadif Neutral file name has to have the **.PAF** extension.
It is an ASCII text file and it contains the information related to the board, device and their connections.

2.2 Cadif file conversion from Unix to MS-DOS

When the diagram entry has been performed and checked on the Cadif CAD workstation, the Cadif file **.PAF** should be made available for the SPEA system.

The SPEA system is based on a PC platform operating in a Windows® environment, this means that the CAD import driver can manage ASCII Text file in MS-DOS format.

Due to the fact that the Cadif workstation typically uses the Unix operating system, the output ASCII text file has to be converted from Unix to MS-DOS format.

In order to perform the conversion, please refer to appendix A – **Note about the Cadif ASCII text file format**.

3. Cadif file format

The Cadif file listed below is a significant example of the format that the file must have to be converted into SPEA format.

```
(cadif
 (format CADIF 4 0)
 (design
  (dataSet ARCHIVE ROUTE_RULES PLACE_RULES)
  (dataSet ARCHIVE ROUTE_RULES PLACE_RULES)
  (paper (name "A2")
   (box (pt -29700000 -21000000) (pt 29700000 21000000))
   (designOrigin (pt -12046028 -11665028))
   (paperScale (e 1 0)))
  (signalList
   (signal S1 (name "50HZ_CLOCK"))                    Signal reference
   (signal S2 (name "A/B_IN"))
   (signal S3 (name "A/B_OUT"))
   (signal S4 (name "BCLOCK"))                        Signal name
   (signal S5 (name "DTMF_CLK"))
   (signal S6 (name "DTMF_CLOCK"))
   (signal S6 (name "DTMF_CLOCK"))
   (signal S7 (name "DTMF_DATA"))
   (signal S8 (name "FALE"))
   (signal S9 (name "FCLE"))


  (package PAC1 (name "0204dio")                      Package reference and Package name
   (packDesc
    (symName "0204dio")
    (leadForm SMD)                                    Package type
    (packTerm T1 (name "1") (id 1))
    (packTerm T2 (name "2") (id 2))
    (packTerm T3 (name "3") (id 3))))
  (package PAC2 (name "0204dioz")
   (packDesc
    (symName "0204dioz")
    (leadForm SMD)
    (packTerm T1 (name "1") (id 1))                   Pin identifier and pin name
    (packTerm T2 (name "2") (id 2))
    (packTerm T3 (name "3") (id 3))))
  (package PAC3 (name "0204wid")
   (packDesc
    (symName "0204wid")
    (leadForm SMD)
    (packTerm T1 (name "1") (id 1))
    (packTerm T2 (name "2") (id 2))
    (packTerm T3 (name "3") (id 3))))




  (packAlt ALT1 (name "reflow")                       Package alternative name
   (packRef PAC1)




    (packAltTerm T1 (id 1)                            Pin identifier
     (position (pt -158750 0))
     (labelPosn (pt -158750 0))
     (padCodeRef PC82)
     (exitDirn SOUTH NORTH WEST))
    (packAltTerm T2 (id 2)
     (position (pt 158750 0))                         Pin coordinates (offset from the barycenter)
```

```
      (labelPosn (pt 158750 0))
      (padCodeRef PC82)
      (exitDirn SOUTH NORTH EAST))
     (packAltTerm T3 (id 3)
      (padCodeRef PC43)                                  Pad reference
      (exitDirn))))


(padCodeLib
     (padShape PS26145                                   Pad shape
      (padRound 100000
       (filledFigure
        (circle 100000 (pt 0 0))                         Pad dimensions
        (fillType SOLID))))
     (padShape PS26146
      (padFinger 70000 30000 30000 0
       (filledFigure
        (rectangle (pt -65000 -35000) (pt 65000 35000))  Pad dimensions
        (fillType SOLID))))
     (padShape PS26147
      (padOblong 60000 80000 80000 0
       (filledFigure
        (rectangle (pt -80000 -30000) (pt 80000 30000))
        (fillType SOLID))))


     (padCode PC106 (name "Circle 1.0/0.6")              Pad reference
      (padCodeDesc
       (drill (name "60000mm")
        (drillSize 60000) (drillLetter "i")
        (drillSymbol (name "60000mm"))
        (plated))
       (padAssign PS26145 (elecLayers))                  Pad shape
     (padCode PC114 (name "Finger 1.3x0.7/0.6")
      (padCodeDesc
       (drill (name "60000mm")
        (drillSize 60000) (drillLetter "i")
        (drillSymbol (name "60000mm"))
        (plated))
       (padAssign PS26146 (elecLayers))


   (part PRT2 (name "B32529-B3333-J")                    Part identifier and Part number
    (partDesc
     (description "KON")
     (detailName "b32529-b3333-j")
     (prefix "C")                                        Part prefix used to identify the family of the
                                                         component (ex. C = Capacitor, R = Resitor)
     (packRef PAC13)
     (catRef CAT1)
     (subElem SE1 (elemRef EL2) (elemSuffix "P"))
     (viaRestrict RESTRICT_NONE)
     (trackRestrict RESTRICT_NONE)
     (partTerm T1 (id 1)
      (elemTermRef T1 (subElemRef SE1)))
     (partTerm T2 (id 2)
      (elemTermRef T2 (subElemRef SE1))))
    (attribute "EMC_part_type" "CAPACITOR" (visible))
    (attribute "Package" "2/7.5/4.5/8")
    (attribute "part_type" "Kondensator ungepolt"
(fixed))
    (attribute "thm_power_diss" "0" (visible))
    (attribute "tolerance" "5.0")
    (attribute "value" "33n" (fixed)))                   Value of the component




 (component C1 (name "C100")                             Component identifier and Drawing reference
```

```
   (compDefn (partRef PRT2) (packAltRef ALT37))
   (location
    (orientation 270)                                   Rotation
    (side BOTTOM)                                       Mounting side
    (position (pt 2768972 2439972))                     Barycenter coordinates


  (net N1 (signalRef S1)
   (netJoins
    (compPinRef T73 (compRef C147))
    (compPinRef T1 (compRef C193))
    (compPinRef T2 (compRef C140))
    (compPinRef T2 (compRef C559))
    (compPinRef T1 (compRef C560))
    (compPinRef T1 (compRef C657)))
   (via V1
    (position (pt -5486028 469972))
    (padCodeRef PC148)
    (layerRange L1 L50))
   (via V2
    (position (pt -2081028 4194972))
    (padCodeRef PC148)
    (layerRange L1 L50))




  (net N2 (signalRef S2)                                Signal reference
   (netJoins
    (compPinRef T19 (compRef C147))
    (compPinRef T1 (compRef C207))                      Component identifier and Pin identifier
    (compPinRef T13 (compRef C167)))
   (via V1
    (position (pt -2621028 -1235028))
    (padCodeRef PC148)
    (layerRange L1 L50))
   (via V2                                              Via identifier
    (position (pt -2146028 -4230028))                   Via coordinates
    (padCodeRef PC148)
    (layerRange L1 L50))
```

4. Import setting

The options to be checked and/or modified are listed below.

Cad Type	Category		Description
CADIF	Options	Add Not Connected Pin	Enables the non-connected pins addition.

4.1 Pin function assignment

This assignment table must be filled, in order to correctly execute the CAD file import.

In order to test correctly some polarized devices such as diodes, bipolar transistors, etc., it is basic to identify correctly the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table, are described below:

Field	Description
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Pin Function	Function concerning the Pin.
Pin Name	Pin reference.
Cad Pin	Pin reference in Cad file.

4.2 Drawing ref. initials/device type assignment

The Cadif file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the point of view of the test program generation.

The fields contained in the table are described below:

Field	Description
Drawing Reference	Initial letter identifying the **Device Type**.
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Default Tol+, Tol-	Value and tolerance of the device only if required (as for resistors).

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.

5. Component Properties Identification

The ATPG Software of the SPEA Systems requires to identify, for each component, the following data:

Passive Components:

- **Component Family**
- **Part Number**
- **Component Value**
- **Tolerance + and -**

Other Components:

- **Component Family**
- **Part Number**
- **Device Name** (commercial name)

The **Component Family** is not specified in the Part List file so it is necessary to fill a table containing the assignment between Drawing Reference initials and Component Family and the CAD Type before executing the import process.

The table contains also the default tolerance for the specified family of the components.

Example:

Device Type	Prefix	Default Tol+	Default Tol-
Capacitor	C	20	20
Resistor	R	10	10
Connector	J		
Digital IC	IC		

For polarized components such as diodes, it is important to identify the pin function (e.g. Anode) of each pin.
Before running the import it is required to edit the pin Id/pin function table.

Example:

Device Type	Pin Function	Pin Id
Diode	Anode	1
Diode	Cathode	2
Capacitor Polarized	Positive	1
Capacitor Polarized	Negative	2

6. Component properties default value

The SPEA Import software automatically assigns a default value if all component properties or part of them are not available in the CAD file.

In this case a further manual ending can be done to perform the necessary modifications by using the Board Data editor.

The default values are shown in the following table:

Property	Default Value
Component Family	Not identified
Value of component	0
Tolerance	0
Device Name	None

A. Note about the Cadif ASCII text file format

The Cadif CAD-CAE typically runs under Unix operating system and generates its neutral ASCII output file in Unix format.

The Unix ASCII text files use the ASCII character "$0a_{hex}$" as end of line identifier.
The Windows® (MS-DOS) operating system uses the ASCII characters "$0d_{hex}$" and "$0a_{hex}$" as end of line identifier for ASCII text files.
This means that output ASCII text files may require an ASCII format conversion (from Unix to Windows® format).

This operation can be performed using "WordPad", a standard text file editor.
Open the Cadif ASCII file with this editor and save it, this operation will automatically perform the conversion from ASCII Unix format to ASCII Windows® format.