CadPack

Import from Gencad

Software tool for import part/net list from Gencad

Technical Info

Version : 2
Code : 81190407.129

SPEA SpA
16, Via Torino
10088 Volpiano - Italy
Tel.: + 39 011 9825 400
Fax: + 39 011 9825 405
E-mail: info@spea.com
Web: www.spea.com

Contents

Introduction II

1. Gencad file data 1

1.1 Part List ... 2

1.2 Net List ... 3

1.3 Coordinates and access list ... 4

1.4 Wiring and Routing list ... 4

2. Gencad file generalities 5

3. Gencad file format 6

4. Import setting 9

4.1 Pin function assignment ... 9

4.2 Drawing ref. initials/device type assignment ... 10

5. Component Properties Identification 11

6. Component properties default value 12

Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

Both Bed of Nails and Flying Probe testers, require the circuit information available on CAD format, in order to generate the ICT test program in a short time and without errors.

The Import from Gencad software tool converts the CAD files of the board from the Gencad format to the SPEA board data format.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

SPEA SpA
Ufficio Documentazione
16, Via Torino
10088 Volpiano – Italy
Tel.: +39 011 9825400
Fax: +39 011 9825405
Email: info@spea.com
Web: www.spea.com

1. Gencad file data

With the “Gencad CAD files” words we refer to the output information generated by the Gencad CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Gencad CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movements for Flying Probes).

Information can be grouped in 4 different categories and typically concern the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is the presentation of the electrical diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information above mentioned SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: - **Top** (Component side) - **Bottom** (Soldering side) - **Not mounted Top** - **Not mounted Bottom**
Rotation [1]	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code [1]	Device package (case) code.

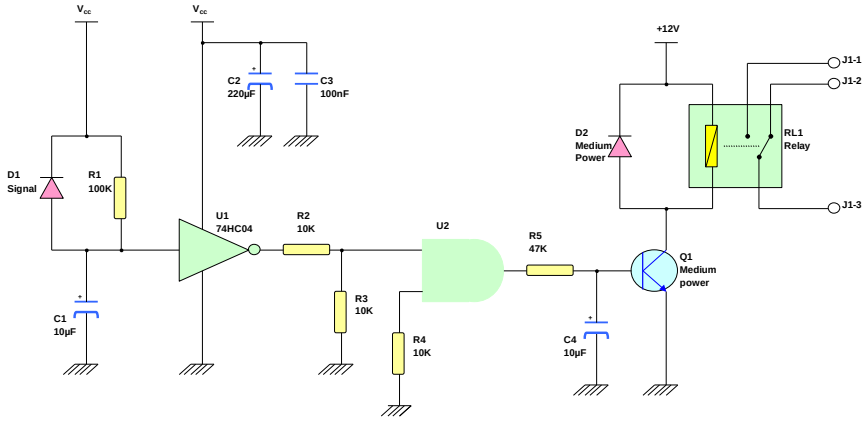
[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: - **Top** (Device side access). - **Bottom** (Soldering side access). - **Not accessible** - **All** (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

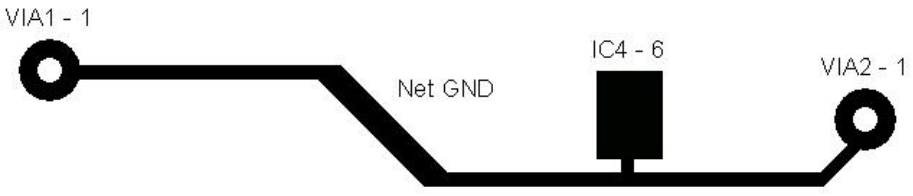
1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



[1] **Optional data**

2. Gencad file generalities

The Gencad required file is: **<FileName>.GCD**

It contains the Part list and the Net list.

The SPEA system is based on a PC platform operating in MS-Windows environment.

The files need to be stored into a directory defined by the user.

The SPEA Import from Gencad software tool can retrieve the Gencad file from each defined disk and directory.

3. Gencad file format

The Gencad file listed below is a significant example of the format that the file must have to be converted into SPEA format.

```
$HEADER
GENCAD 1.4
USER RSI-TRANSLATOR GENCAD OUTPUT V:14
DRAWING 011159_2
REVISION Tue MM DD hh:mm:ss yyyy
UNITS USER 1000
ORIGIN 0 0
INTERTRACK 0
$ENDHEADER


$COMPONENTS                                                    Component Drawing reference
COMPONENT C1
DEVICE "C1_301-009501"
PLACE 3450.000 5725.000                                        Component position on the board
LAYER TOP                                                      Mounting side
ROTATION 270                                                   Rotation
SHAPE TAJD_D_P 0 0
ATTRIBUTE COMPATTR_1 "EDWA" "1983"
ATTRIBUTE COMPATTR_2 "MODEL" "NULL"
ATTRIBUTE COMPATTR_3 "REFLOC" "IN,0.025,0.0,180,CC,0.05,0.05,0.01,std,0,DRAWING,0.0,-
0.125,180,CC,0.05,0.05,0"
COMPONENT C2
DEVICE "C2_301-009501"                                         Device attributes identifier
PLACE 5450.000 5275.000
LAYER TOP
ROTATION 90
SHAPE TAJD_D_P 0 0                                             Shape identifier
ATTRIBUTE COMPATTR_1 "EDWA" "1983"
ATTRIBUTE COMPATTR_2 "MODEL" "NULL"
ATTRIBUTE COMPATTR_3 "REFLOC" "IN,0.025,0.0,0,CC,0.05,0.05,0.01,std,0,DRAWING,-
0.475,0.1125,0,TL,0.06,0.06,0."


$SHAPES
SHAPE C0805_B                                                  Shape identifier
LINE 71.000 -46.000 -71.000 -46.000
LINE -71.000 -46.000 -71.000 46.000
LINE -71.000 46.000 71.000 46.000
LINE 71.000 46.000 71.000 -46.000
PIN 1 smd_o050x075 -38.000 0.000 TOP 0 0                       Pin offset from the barycenter
PIN 2 smd_o050x075 38.000 0.000 TOP 0 0
INSERT SMD
SHAPE R0805_A
LINE 66.000 -46.000 -66.000 -46.000
LINE -66.000 -46.000 -66.000 46.000
LINE -66.000 46.000 66.000 46.000
LINE 66.000 46.000 66.000 -46.000
PIN 1 smd_o050x075 -32.500 0.000 TOP 0 0
PIN 2 smd_o050x075 32.500 0.000 TOP 0 0
INSERT SMD


SHAPE R1206_A
LINE 92.000 -47.000 -92.000 -47.000
LINE -92.000 -47.000 -92.000 47.000
LINE -92.000 47.000 92.000 47.000
LINE 92.000 47.000 92.000 -47.000
PIN 1 smd_o040x075 -62.000 0.000 TOP 0 0
PIN 2 smd_o040x075 62.000 0.000 TOP 0 0
```

```
INSERT SMD
SHAPE SO16B_D
LINE -310.000 -230.000 310.000 -230.000
LINE 310.000 -230.000 310.000 230.000
LINE 310.000 230.000 -310.000 230.000
LINE -310.000 230.000 -310.000 -230.000
PIN 1 smd_o025x060 -275.000 -190.000 TOP 0 0
PIN 2 smd_o025x060 -225.000 -190.000 TOP 0 0
PIN 3 smd_o025x060 -175.000 -190.000 TOP 0 0
PIN 4 smd_o025x060 -125.000 -190.000 TOP 0 0
PIN 5 smd_o025x060 -75.000 -190.000 TOP 0 0
PIN 6 smd_o025x060 -25.000 -190.000 TOP 0 0
PIN 7 smd_o025x060 25.000 -190.000 TOP 0 0
PIN 8 smd_o025x060 75.000 -190.000 TOP 0 0
PIN 9 smd_o025x060 125.000 -190.000 TOP 0 0
PIN 10 smd_o025x060 175.000 -190.000 TOP 0 0
PIN 11 smd_o025x060 225.000 -190.000 TOP 0 0
PIN 12 smd_o025x060 275.000 -190.000 TOP 0 0
PIN 13 smd_o025x060 275.000 190.000 TOP 0 0
PIN 14 smd_o025x060 225.000 190.000 TOP 0 0
PIN 15 smd_o025x060 175.000 190.000 TOP 0 0
PIN 16 smd_o025x060 125.000 190.000 TOP 0 0
INSERT SMD


$DEVICES
DEVICE "C1_301-009501"                                  Device and Part number identifier
VALUE "100uf"
TYPE "CAP_POLAR"
DESC "TAJD_D_P"
PINDESC 1 1
PINDESC 2 2
DEVICE "C2_301-009501"
VALUE "100uf"                                           Value
TYPE "CAP_POLAR"
DESC "TAJD_D_P"
PINDESC 1 1
PINDESC 2 2
DEVICE "C3_TAJD336K016"
VALUE "33u"
TYPE "CAP_POLAR"
DESC "TAJD_D_P"
PINDESC 1 1
PINDESC 2 2


$SIGNALS
SIGNAL VCC                                              Net identifier
NODE P2 33
NODE IC18 90
NODE IC18 40
NODE IC18 28




NODE IC18 53
NODE R121 1
SIGNAL /A(1)
NODE IC6 4                                              Net list
NODE P1 30
SIGNAL /A(2)
NODE IC6 6
NODE P1 29
SIGNAL /A(3)
NODE IC6 8
NODE P1 28
SIGNAL /A(4)
NODE IC6 17
NODE P1 27
```

```
SIGNAL /A(5)
NODE IC6 15
NODE P1 26
SIGNAL /A(6)
NODE IC6 13
NODE P1 25


$ROUTES
ROUTE VCC                                                    Net identifier
VIA via_s030_040 4550.000 1625.000 ALL -1 via1
VIA via_s030_040 3500.000 2100.000 ALL -1 via2
VIA via_s030_040 2250.000 4300.000 ALL -1 via3
VIA via_s030_040 1800.000 4300.000 ALL -1 via4
VIA via_s030_040 2250.000 4850.000 ALL -1 via5
VIA via_s030_040 1800.000 4850.000 ALL -1 via6               Via identifier and properties


ROUTE DGND
VIA via_s030_040 525.000 5000.000 ALL -1 via57
VIA via_s030_040 950.000 5000.000 ALL -1 via58
VIA via_s030_040 1375.000 5000.000 ALL -1 via59
VIA via_s030_040 2250.000 2750.000 ALL -1 via60
VIA via_s030_040 1100.000 2750.000 ALL -1 via61


ROUTE /A(1)
ROUTE /A(2)
ROUTE /A(3)
ROUTE /A(4)


ROUTE /N$1267
VIA via_s030_040 3550.000 425.000 ALL -1 via120
VIA via_s030_040 8900.000 350.000 ALL -1 via121
ROUTE /N$1268
VIA via_s030_040 3550.000 475.000 ALL -1 via122
VIA via_s030_040 8900.000 400.000 ALL -1 via123
```

4. Import setting

4.1 Pin function assignment

In order to correctly execute the CAD file import, this assignment table must be filled.

In order to correctly test some polarized devices such as diodes, bipolar transistors, etc., it is basic to correctly identify the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table are described below:

Field	Description
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Pin Function	Function concerning the Pin.
Pin Name	Pin reference.
Cad Pin	Pin reference in Cad file.

4.2 Drawing ref. initials/device type assignment

The Gencad file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the point of view of the test program generation.

The fields contained in the table are described below:

Field	Description
Drawing Reference	Initial letter identifying the **Device Type**.
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Default Tol+, Tol-	Value and tolerance of the device only if required (as for resistors).

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.

5. Component Properties Identification

The ATPG Software of the SPEA Systems requires to identify the following data for each component:

Passive Components:

- **Component Family**
- **Part Number**
- **Component Value**
- **Tolerance + and -**

Other Components:

- **Component Family**
- **Part Number**
- **Device Name** (commercial name)

The **Component Family** is not specified in the Part List file so, it is required to fill a table containing the assignment between Drawing Reference initials and Component Family and the CAD Type before executing the import process.

The table contains also the default tolerance for the specified family of components.

Example:

Device Type	Drawing. ref. initials	Default Tol+	Default Tol-
Capacitor	C	20	20
Resistor	R	10	10
Connector	J		
Digital IC	IC		

For polarized components such as diodes, it is important to identify the pin function (e.g. Anode) of each pin.
Before running the import, it is necessary to edit the pin Id/pin function table.

Example:

Device Type	Pin Function	Cad Pin Id
Diode	Anode	ANOTHER
Diode	Cathode	CATHODE
Polarized Capacitor	Positive	PLUS
Polarized Capacitor	Negative	MINUS

6. Component properties default value

The SPEA Import software automatically assigns a default value if all component properties or part of them are not available in the CAD file.

In this case a further manual ending can be done to perform the required modifications by using the Board Data editor.

The default values are shown in the following table:

Property	Default Value
Component Family	Not identified
Value of component	0
Tolerance	0
Device Name	None