CadPack

Import from TXF - OUT

Software tool for import part/net list from TXF - OUT

Technical Info

Version : 2
Code : 81190418.144

SPEA SpA
16, Via Torino
10088 Volpiano - Italy
Tel.: + 39 011 9825 400
Fax: + 39 011 9825 405
E-mail: info@spea.com
Web: www.spea.com

Contents

Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The Import from TXF-OUT software tool converts the CAD data files of the Board from the TXF-OUT format to the SPEA Board data format.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

SPEA SpA
Ufficio Documentazione
16, Via Torino
10088 Volpiano – Italy
Tel.: +39 011 9825400
Fax: +39 011 9825405
Email: info@spea.com
Web: www.spea.com

1. TXF-OUT file data

With the “TXF-OUT CAD files” words we refer to the output information generated by the TXF-OUT CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “TXF-OUT CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movement for Flying Probes).

Information can be grouped in 4 different categories and typically are related to the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is the presentation of the electrical diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information mentioned above SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: - **Top** (Component side) - **Bottom** (Soldering side) - **Not mounted Top** - **Not mounted Bottom**
Rotation [1]	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code [1]	Device package (case) code.

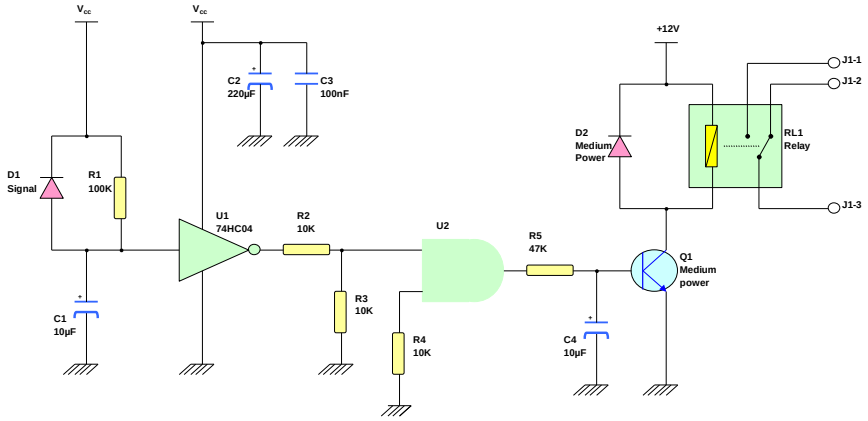
[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: - **Top** (Device side access). - **Bottom** (Soldering side access). - **Not accessible** - **All** (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

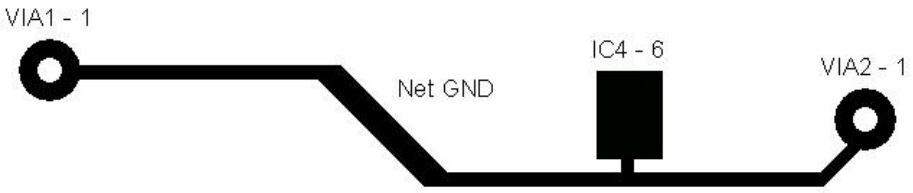
1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



[1] **Optional data**

2. TXF-OUT file generalities

The TXF-OUT file required is: **<File Name>.TXF**

It contains the Part list and the Net list.

The SPEA system is based on a PC platform operating in MS-Windows environment.

The files need to be stored into a directory defined by the user.

The SPEA Import from TXF-OUT software tool can retrieve the TXF-OUT file from each defined disk and directory.

3. TXF-OUT file format

The TXF-OUT file contains different data which can be design data or library component descriptions. The TXF-OUT file consists of several sections describing specific type of data.

A TXF-OUT file consists of the following main sections:

- **Component List**
- **Net List**
- **Track List**
- **Variant List**

3.1 Extracts of typical TXF-OUT output files

The TXF-OUT file listed below are a significant example of the format that the file must have to be converted into SPEA format:

```
component
  {
  din {"R100"}                                  Drawing reference
  shape
   {
   name {"RMS1S"}                               Package name


   pivot {38.5763, 33.8138}                     Component barycenter
   rotation {-180}                              Component rotation
   layer {1}                                    Mounting side
   fixed {0}
   typ {"13K"}                                  Component type name
   part_code {"14544200.072"}                   Component Part Number
   comment {"............."}
   use_text_link {1}
   }
  symbol
   {
   name {""}
   pivot {-54.61, 0}
   page {0}
   rotation {360}
   mirror {0}
   use_text_link {0}
   }
  }


shape                                           Shape data identifier
  {
  name {"RMS1S"}                                Component name
  size {9.36625, 4.445}
  pivot {2.30505, 2.2225}
  elements
   {
   point
    {
    typ {pin_1}
    coor {0, 0}
    layer
     {
     plan {1}
     }
```

```
    }
   place_holder
    {
    typ {din}
    pivot {-2.2733, 2.5654}
    size {5.6642, 1.69545}
    rotation {0}
    layer
     {
     plan {1}
     }
    }
   pin
    {
    pivot {0, 0}
    rotation {0}
    name {"1"}
    pad
     {
     std_pad {10}
     layer
      {
      track {0}
      track {1}
      soldermask {0}
      soldermask {1}
      drill {0}
      }
     }
    drill {7}
    }
   pin                                    Pin identifier
    {
    pivot {5.715, 0}                      Pin offset
    rotation {0}                          Rotation of the pin
    name {"2"}                            Pin name
    pad
     {
     std_pad {10}
     layer
      {
      track {0}
      track {1}
      soldermask {0}
      soldermask {1}
      drill {0}
      }
     }
    drill {7}
    }
   circle
    {
    coor {0, 0}
    radius {2.03835}
    index {8}
    layer
     {
     plan {1}
     }
    }
   line
    {
    start {0, 0}
    end {5.715, 0}
    index {8}
    layer
     {
     plan {1}
     }
```

```
    }
   }
  }
```

`net`	Net identifier
`  {`	
`  name {"1N20"}`	Net name
`  supply {0}`	
`  distance {0.50165}`	
`  width {1}`	
`  pin_list`	
`   {`	
`   pin`	Pin identifier
`    {`	
`    din {"R100"}`	Drawing reference
`    name {"1"}`	Pin name

```
    slpname {"1"}
    element_class {0}
    gate_class {0}
    pin_class {0}
    index {1}
    typ {other}
    }
   pin
    {
    din {"TP22"}
    name {"1"}
    slpname {"1"}
    element_class {0}
    gate_class {1}
    pin_class {1}
    index {1}
    typ {in}
    }
   pin
    {
    din {"V1"}
    name {"1"}
    slpname {"1"}
    element_class {0}
    gate_class {1}
    pin_class {1}
    index {1}
    typ {other}
    }
   }
  }

  net
   {
   name {"1N1110"}
   track
    {
    start {105.042, 46.0375}
    end {105.093, 45.9867}
    index {8}
    layer
     {
     track {0}
     }
    }
   track
    {
    start {105.093, 44.6596}
    end {105.093, 45.9867}
```

```
    index {13}
    layer
     {
     track {0}
     }
    }


   via                                  Via identifier
    {
    coor {98.1329, 36.7792}             Via coordinates
    index {2}
    }


{
net_list
{
  net
  {
   name { "1V5_1" }                     Net name
   track                                Track identifier
   {
    start { 14.399683,34.696400 }       Track start coordinates
    end { 14.399683,32.899350 }         Track end coordinates
    width { 0.198967 }                  Track width
    layer
    {
     track { 1 }                        Layer
    }
   }
   track
   {
    start { 14.399683,32.899350 }
    end { 13.900150,32.399817 }
    width { 0.198967 }
    layer
    {
     track { 1 }
    }
   }
   track
   {
    start { 13.900150,29.599467 }
    end { 13.900150,32.399817 }
    width { 0.198967 }
    layer
    {
     track { 1 }
    }
```

3.2 Extracts of "Variant" TXF-OUT output files

The TXF-OUT files listed below are a significant example of the format that the file must have to be converted into SPEA format:

```
variant_list                                    Variant list identifier
 {
  name { "Variant1" }                           Variant name
  name { "Standard" }
  active { "alle Varianten" }
 }



component
 {
  din { "D20" }                                 Drawing reference
  symbol
  {
   name { "Diode" }
   pivot { 175.000000,104.000000 }
   rotation { 180.000000 }
   mirror { 0 }
   id { "A" }
   placed { placed }
   Elements
   {
    place_holder
    {
     typ { technology }
     pivot { 172.000000,108.000000 }
     size { 18.930000,1.500000 }
     rotation { 180.000000 }
     hidden { 0 }
     adjust { topcenter }
    }
    place_holder
    {
     typ { din }
     pivot { 172.480000,101.010000 }
     size { 3.510000,1.800000 }
     rotation { 180.000000 }
     hidden { 0 }
     adjust { topcenter }
    }
    terminal
    {
     name { "K" }
     pivot { 169.000000,104.000000 }
     offset { 0.000000,0.000000 }
     size { 1.200000,1.500000 }
     rotation { 180.000000 }
     hidden { 1 }
     adjust { topright }
     aspect_ratio { 0.800000 }
     offset2 { -0.800000,-0.400000 }
     size2 { 1.200000,1.500000 }
     rotation2 { 180.000000 }
     hidden2 { 1 }
     adjust2 { topright }
     aspect_ratio2 { 0.800000 }
     typ { other }
     pin_class { 12 }
     element_class { 0 }
    }
    terminal
    {
     name { "A" }
```

```
     pivot { 175.000000,104.000000 }
     offset { 0.000000,0.000000 }
     size { 1.260000,1.500000 }
     rotation { 180.000000 }
     hidden { 1 }
     adjust { topright }
     aspect_ratio { 0.800000 }
     offset2 { 3.000000,-0.400000 }
     size2 { 1.260000,1.500000 }
     rotation2 { 180.000000 }
     hidden2 { 1 }
     adjust2 { topright }
     aspect_ratio2 { 0.800000 }
     typ { other }
     pin_class { 11 }
     element_class { 0 }
    }
   }
  }
  Shape                                          Shape data identifier
  {
   name { "SOD123" }                             Component name
   mapping { "A" }
   pivot { 6.000750,13.699067 }                  Component barycenter
   rotation { 270.000000 }                       Component rotation
   layer { 1 }                                   Mounting side
   placed { placed }
   variant_list
   {
    variant
    {
     name { "Variant1" }
     place { 0 }
     typ { "Diode" }                             Component type name
     part_code { "AA000220" }                    Component Part Number
     technology { "MBR0520LT1" }
     reference { "" }
     comment { "" }
    }
    variant
    {
    name { "Standard" }
     place { 0 }
     typ { "Diode" }
     part_code { "AA000238" }
     technology { "MBR0520LT1" }
     reference { "" }
     comment { "" }
    }
   }
   lib_name { "c:\cad\integra\lib\a.lib" }
   class { "D" }
   elements
   {
    place_holder
    {
     pivot { 6.000750,13.699067 }
     size { 10.085917,0.999067 }
     rotation { 270.000000 }
     width { 0.099483 }
     adjust { centercenter }
     aspect_ratio { 0.800000 }
     typ { technology }
     layer
     {
      plan { 1 }
     }
    }
    place_holder
```

```
    {
     pivot { 6.000750,13.699067 }
     size { 1.562100,0.999067 }
     rotation { 270.000000 }
     width { 0.099483 }
     adjust { centercenter }
     aspect_ratio { 0.800000 }
     typ { din }
     layer
     {
      plan { 1 }
     }
    }
   }
  }
 }


{
net_list
{
  net
  {
   name { "1V5_1" }                          Net name
   track                                     Track identifier
   {
    start { 14.399683,34.696400 }            Track start coordinates
    end { 14.399683,32.899350 }              Track end coordinates
    width { 0.198967 }                       Track width
    layer
    {
     track { 1 }                             Layer
    }
   }
   track
   {
    start { 14.399683,32.899350 }
    end { 13.900150,32.399817 }
    width { 0.198967 }
    layer
    {
     track { 1 }
    }
   }
   track
   {
    start { 13.900150,29.599467 }
    end { 13.900150,32.399817 }
    width { 0.198967 }
    layer
    {
     track { 1 }
    }
```

4. Import settings

The options to be checked and/or modified are listed below.

Cad Type	Category		Description
TXF-OUT	Options	Value identifier	Label identifying the components value.
		Net identifier for pins not connected	Label identifying the nets with non-connected pins.

4.1 Pin function assignment

This assignment table must be filled, in order to execute correctly the CAD file import.

In order to test correctly some polarized devices such as diodes, bipolar transistors, etc., it is basic to identify correctly the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table are described below:

Field	Description
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Pin Function	Function concerning the Pin.
Pin Name	Pin reference.
Cad Pin	Pin reference in Cad file.

4.2 Drawing ref. initials/device type assignment

The TXF-OUT file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the test program generation point of view.

The fields contained in the table are described below:

Field	Description
Drawing Reference	Initial letter identifying the **Device Type**.
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Default Tol+, Tol-	Value and tolerance of the device only if required (as for resistors).

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.

5. Component Properties Identification

The ATPG Software of the SPEA Systems requires to identify the following data for each component:

Passive Components:

- **Component Family**
- **Part Number**
- **Component Value**
- **Tolerance + and -**

Other Components:

- **Component Family**
- **Part Number**
- **Device Name** (commercial name)

The **Component Family** is not specified in the Part List file so it is necessary to fill a table containing the assignment between Drawing Reference initials and Component Family and the CAD Type before executing the import process.

The table contains also the default tolerance for the specified family of the components.

Example:

Device Type	Prefix	Default Tol+	Default Tol-	CAD Type
Capacitor	C	20	20	Capacitor
Resistor	R	10	10	Resistor
Connector	J			Connector
Digital IC	IC			Digital IC

For polarized components such as diodes, it is important to identify the pin function (e.g. Anode) of each pin.
Before running the import it is necessary to edit the pin Id/pin function table.

Example:

Device Type	Pin Function	CAD Pin Id
Diode	Anode	ANODE
Diode	Cathode	CATHODE
Polarized Capacitor	Positive	PLUS
Polarized Capacitor	Negative	MINUS

6. Component properties default value

The SPEA Import software automatically assigns a default value if all or part of the component properties that are not available in the CAD file.

In this case a further manual ending can be done to perform the necessary modifications by using the Board Data editor.

The default values are shown in the following table:

Property	**Default Value**
Component Family	Not identified
Value of component	0
Tolerance	0
Device Name	None