

CadPack

Import from Fabmaster

Software tool for import part/net list from Fabmaster

Technical Info

Version 2
Code : 81190405.113



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Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The Import from Fabmaster software tool converts the CAD data files of the Board from the Fabmaster format to the SPEA Board data format.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

Registered trademarks

SPEA is a registered trademark of SPEA SpA.

All other product and company names are trademarks or trade names of their respective companies.

This manual can be updated in accordance with the evolution of the system and associated software. It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

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Revisions

Version	Data	Remarks
2	23/06/2014	Updated "Mounting Side" in chapter 4.3; updated "Pin Access Side" in chapter 4.5.

1. Fabmaster file data

With the “Fabmaster CAD files” words we refer to the output information generated by the Fabmaster CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Fabmaster CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movement for Flying Probes).

Information can be grouped in 4 different categories and typically concern the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is presentation of the electrical diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information above mentioned SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”. The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10K Ω , 10 μ F, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: <ul style="list-style-type: none">- Top (Component side)- Bottom (Soldering side)- Not mounted Top- Not mounted Bottom
Rotation ¹	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions ¹	Device dimensions.
Case code ¹	Device package (case) code.

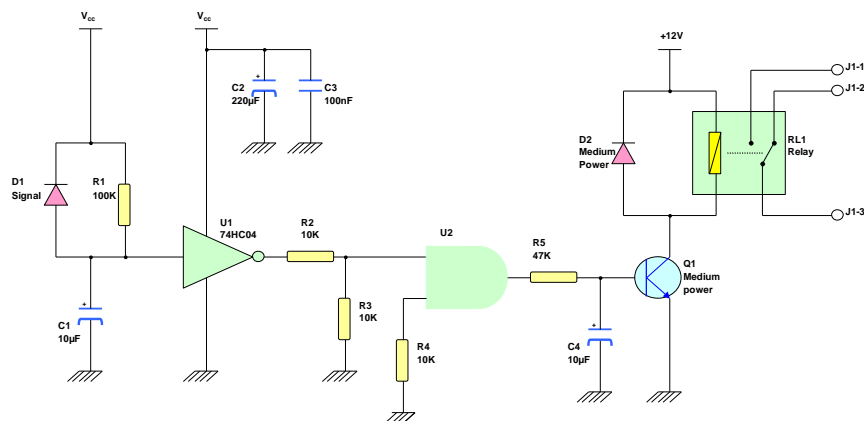
¹ Optional data (not yet managed)

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list. This list must contain the interconnection between devices, including pad and via. Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: <ul style="list-style-type: none"> - Top (Device side access). - Bottom (Soldering side access). - Not accessible - All (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre ¹	Device X barycentre.
Y barycentre ¹	Device Y barycentre.

1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



¹ Optional data

2. Fabmaster file generalities

The Fabmaster required file is: **<FileName>.CAD**

Containing the Part list and the Net list.

The SPEA system is based on a PC platform operating in MS-Windows environment.

The files need to be stored into a directory defined by the user.

The SPEA Import from Fabmaster software tool can retrieve the Fabmaster file from each defined disk and directory.

3. Fabmaster file format

This is an example of a Fabmaster output ASCII text file:

```
:CADFILEINFO
2.20
:ENDCADFILEINFO

:BOARDINFO
DEMOBOARD ,800020AB001,4000 ,3000 ,8400 ,6500 ,08/05/97,1.00 ,MILS,120 ,4
:ENDBOARDINFO

:PARTLIST
0 ,R1 ,14544200AB02 ,4500 ,5400 ,T,180
0 ,R2 ,14544200AB04 ,5500 ,5400 ,T, 0
0 ,D2 ,22001200AB04 ,6500 ,2400 ,T, 0
0 ,IC1 ,40008600AB02 ,7900 ,6000 ,T, 0
0 ,TP1 ,TEST_POINT ,6000 ,3400 ,B, 0
0 ,TP2 ,TEST_POINT ,6800 ,4000 ,B, 0
0 ,VIA1 ,VIA_100 ,6400 ,4000 ,B, 0
0 ,VIA2 ,VIA_100 ,6100 ,4000 ,B, 0
:ENDPARTLIST

:PNDATA
14544200AB02 , 1, ,10 ,10 ,10 ,RESSTD
14544200AB04 , 1, ,0.470 ,20 ,20 ,8025
22001200AB04 , 30,1N4148 , , , ,8025
40008600AB02 ,200,74LS00 , , , ,DIL300
TEST_POINT ,800, , , , ,TP
VIA_100 ,802, , , , ,VIA_100
:ENDPNDATA

:NETLIST
1 ,GND ,R1 ,1 ,4400 ,5400 ,N,1
2 ,VCC ,R1 ,2 ,4600 ,5400 ,N,1
1 ,GND ,D2 ,A ,6400 ,5400 ,N,1
3 ,NET_A ,D2 ,K ,6600 ,5400 ,N,1
3 ,NET_A ,R2 ,1 ,4400 ,5400 ,N,1
2 ,VCC ,R2 ,2 ,4600 ,5400 ,N,1
1 ,VCC ,IC1 ,14 ,7600 ,6150 ,B,2
2 ,GND ,IC1 ,7 ,8400 ,5850 ,B,2
4 ,NET_B ,IC1 ,1 ,7600 ,5850 ,B,2
3 ,NET_A ,IC1 ,2 ,7700 ,5850 ,B,2
5 ,NET_C ,IC1 ,3 ,7800 ,5400 ,B,2
6 ,SNC1 ,IC1 ,4 ,7900 ,5400 ,B,2
7 ,SNC2 ,IC1 ,5 ,8000 ,5400 ,B,2
8 ,SNC3 ,IC1 ,6 ,8100 ,5400 ,B,2
9 ,SNC4 ,IC1 ,7 ,8200 ,5400 ,B,2
9 ,SNC5 ,IC1 ,8 ,8200 ,6150 ,B,2
9 ,SNC6 ,IC1 ,9 ,8100 ,6150 ,B,2
9 ,SNC7 ,IC1 ,10 ,8000 ,6150 ,B,2
9 ,SNC8 ,IC1 ,11 ,7900 ,6150 ,B,2
9 ,SNC9 ,IC1 ,12 ,7800 ,6150 ,B,2
9 ,SNC10 ,IC1 ,13 ,7700 ,6150 ,B,2
2 ,VCC ,TP1 ,1 ,6000 ,3400 ,B,3
2 ,GND ,TP2 ,1 ,6800 ,4000 ,B,3
2 ,GND ,VIA1 ,1 ,6400 ,4000 ,A,4
2 ,GND ,VIA2 ,1 ,6100 ,4000 ,A,4
:ENDNETLIST
```

```

:TESTPOINT
1 ,TP1-1 ,VCC ,TP1 ,1 ,M ,6 ,6000 ,3400 ,B
2 ,IC1-14 ,VCC ,IC1 ,14 ,K ,4 ,7600 ,6150 ,B
3 ,TP2-1 ,GND ,TP2 ,1 ,M ,6 ,6800 ,4000 ,B
4 ,VIA1-1 ,GND ,VIA1 ,1 ,K ,3 ,6400 ,4000 ,B
5 ,VIA2-1 ,GND ,VIA2 ,1 ,K ,3 ,6100 ,4000 ,B
6 ,IC1-4 , $NC1 ,IC1 ,4 ,M ,4 ,7900 ,5400 ,B
7 ,IC1-5 , $NC2 ,IC1 ,5 ,M ,4 ,8000 ,5400 ,B
8 ,IC1-6 , $NC3 ,IC1 ,6 ,M ,4 ,8100 ,5400 ,B
9 ,IC1-7 , $NC4 ,IC1 ,7 ,M ,4 ,8200 ,5400 ,B
10 ,IC1-8 , $NC5 ,IC1 ,8 ,M ,4 ,8200 ,6150 ,B
11 ,IC1-9 , $NC6 ,IC1 ,9 ,M ,4 ,8100 ,6150 ,B
12 ,IC1-10 , $NC7 ,IC1 ,10 ,M ,4 ,8000 ,6150 ,B
13 ,IC1-11 , $NC8 ,IC1 ,11 ,M ,4 ,7900 ,6150 ,B
14 ,IC1-12 , $NC9 ,IC1 ,12 ,M ,4 ,7800 ,6150 ,B
15 ,IC1-13 , $NC10 ,IC1 ,13 ,M ,4 ,7700 ,6150 ,B
16 ,IC1-2 ,NET_A ,IC1 ,2 ,M ,4 ,7700 ,5850 ,B
17 ,IC1-1 ,NET_B ,IC1 ,1 ,M ,4 ,7600 ,5850 ,B
18 ,IC1-3 ,NET_C ,IC1 ,3 ,M ,4 ,7800 ,5400 ,B
:ENDTESTPOINT

:PACKAGES
SOT23 ,TH ,400,600,100
DIL300 ,SMD,700,300,120
TP ,SMD,50,50,0
VIA_100 ,TH,100,75,0
:ENDPACKAGES

:PAD
1 ,PAD1 ,RECT ,50,150,25,75
2 ,PAD2 ,RECT ,150,100,75,50
3 ,PAD3 ,CIRCLE,50,50.25,25
4 ,PAD4 ,CIRCLE,50,50,25,25
:ENDPAD

```

The Import from Fabmaster CAD driver can correctly identify and use the following sections:

- ◆ **File format info**
- ◆ **Board general info**
- ◆ **Part list**
- ◆ **Part Number Data**
- ◆ **Net list**
- ◆ **Test point**
- ◆ **Variants**
- ◆ **Panel of board**
- ◆ **Case types**
- ◆ **Package pins**
- ◆ **Pads**
- ◆ **Wiring**
- ◆ **Routing**
- ◆ **Board Outline**

In the next paragraphs it is provided a short description for each section.

3.1 The SPEA Cad/Fabmaster Ascii File (File version 2.20)

The neutral ASCII file is an ASCII file containing all data required to automatically generate a test program for a SPEA system.

The file is organized in sections; labels delimit the sections.

The section identifier labels begin with a ":" (e.g.: PARTLIST ... :ENDPARTLIST).

In each section data are organized by row and data fields are separated by comma ",".

The "," comma character cannot be part of a field.

Each field can optionally be right padded to the field length with blanks to improve readability.

If the not mandatory datum is not filled, it must be replaced with blanks.

The file can contain user defined remarks. A remark row begins with a ";".

3.2 Changes from rel. 2.00 to rel. 2.10

1. The **File format info**, **Case types** and **Pads** sections have been added.
2. The case dimensions have been moved from the **Part Number Data** section to the case type section.
3. The **Case code** field in the part number section has been replaced with the **Case name**.
4. The **Pad code** field has been added to the net list section.
5. The **Device Type** table has been updated with some new codes (151, 152, 601, 657, 658, 659).

3.3 Changes from rel. 2.10 to rel. 2.20

1. The **Wirings** and **Routing** sections have been added.
2. The **Package Pins** section has been added.
3. The **Board Outline** section has been added.

4. File sections

4.1 File format info

This section contains the release of the file format.

```
:CADFILEINFO  
2.20  
:ENDCADFILEINFO  
*****
```

The section is delimited by:

- ◆ **CADFILEINFO**
- ◆ **ENDCADFILEINFO**

This section contains only one row.

The following fields are defined:

Field No.	Field name	Type	
1	Data release	Num 2.2	Mandatory

4.2 Board general info

This section contains general info such as the board name, the unit of measurement and the board dimensions.

```

*****
:BOARDINFO
DEMOBOARD ,800020AB001,4000 ,3000 ,8400 ,6500 ,08/05/97,1.00 ,MILS,120 ,4
:ENDBOARDINFO
*****

```

The section is delimited by:

- ◆ **BOARDINFO**
- ◆ **ENDBOARDINFO**

This section contains only one row.

The following fields are defined:

Field no.	Field name	Type	
1	Board name	Char * 12	Mandatory
2	Part Number	Char * 25	
3	Minimum X	Num 10.3	
4	Minimum Y	Num 10.3	
5	Maximum X	Num 10.3	
6	Maximum Y	Num 10.3	
7	Date of creation	Char 8	Mandatory
8	Board release	Num 5.0	
9	Unit of measurement	Char 4	
10	Thickness	Num 10.3	
11	Layers	Num 2	

Units of measurement

Unit of Measurements	Description
MM	Millimeter
UMM	Millimeter /100 (micron)
INCH	Inch
MILS	Mils

4.3 Part list

This section contains the Part list, and the mounting info of each component.

```

.....
:PARTLIST
0 ,R1      ,14544200AB02      ,4500      ,5400      ,T,180
0 ,R2      ,14544200AB04      ,5500      ,5400      ,T, 0
0 ,D2      ,22001200AB04      ,6500      ,2400      ,T, 0
0 ,IC1      ,40008600AB02      ,7900      ,6000      ,T, 0
0 ,TP1      ,TEST_POINT      ,6000      ,3400      ,B, 0
0 ,TP2      ,TEST_POINT      ,6800      ,4000      ,B, 0
0 ,VIA1      ,VIA_100      ,6400      ,4000      ,B, 0
0 ,VIA2      ,VIA_100      ,6100      ,4000      ,B, 0
:ENDPARTLIST
.....

```

The section is delimited by:

- ◆ **PARTLIST**
- ◆ **ENDPARTLIST**

This section contains one row for each component present in the board.
The following fields are defined:

Field No.	Field name	Type	
1	Variant code	Num 3.0	Mandatory
2	Drawing reference	Char * 12	Mandatory
3	Part Number	Char * 24	Mandatory
4	X-Barycentre	Num 10.3	
5	Y-Barycentre	Num 10.3	
6	Mounting side	Char * 1	Mandatory
7	Rotate	Num 3.0	

Mounting Side

Mounting side	Description
T	Top Board Side
B	Bottom Board Side
P	Not mounted Top
M	Not mounted Bottom
F	Frame Top
R	Frame Bottom

For a standard board the **Variant code** has to be filled with "0".

4.4 Part Number Data

This section contains data concerning the Part Numbers.

```

.....
:PNDATA
14544200AB02      , 1,      ,10      ,10      ,10      ,RESSTD
14544200AB04      , 1,      ,0.470    ,20      ,20      ,8025
22001200AB04      , 30,1N4148  ,      ,      ,      ,8025
40008600AB02      ,200,74LS00  ,      ,      ,      ,DIL300
TEST_POINT        ,800,      ,      ,      ,      ,TP
VIA_100           ,802,      ,      ,      ,      ,VIA_100
:ENDPNDATA
.....

```

The section is delimited by:

- ◆ **PNDATA**
- ◆ **ENDPNDATA**

This section contains one row for each Part Number present in the board.

The following fields are defined:

Field No.	Field name	Type	
1	Part Number	Char * 24	Mandatory
2	Device type code	Num 3.0	Mandatory
3	Device name	Char * 12	Mandatory
4	Not used	Char *1	Mandatory
5	Value	Num 15.7	Mandatory
6	Tolerance pos.	Num 3.0	Mandatory
7	Tolerance neg.	Num 3.0	Mandatory
8	Case name	Char 16	Mandatory

The **Value**, **Tolerance pos** and **Tolerance neg** are **mandatory** for passive components such as Resistors, Capacitors Inductors and for Zeners.

The **Device name** is **mandatory** for all the other components (Diodes, Digital ICs, Transistors, etc.).

The **VALUE** field must be written according to the following rules:

- ◆ **Resistor** The Value is expressed in Kohm (150 ohm -> 0.150)
- ◆ **Capacitor** The Value is expressed in uF (250nF -> 0.250)
- ◆ **Inductor** The Value is expressed in mH (10mH -> 10)

Device type table

Device type code	Description
0	Not Testable
1	Resistor
2	Potentiometer
4	Varistor
10	Capacitor
11	Capacitor Polar.
20	Inductor
21	Transformer
30	Diode
31	Zener
32	Transzorb
33	Diac
40	NPN Trans/Darl
41	PNP Trans/Darl
50	Scr
51	Triac
58	Mosfet P
59	Mosfet N
60	Mos
61	Fet
62	JFet P
63	JFet N
70	Crystal Oscill.
71	Oscillator
80	Led
81	Opto Coupler
82	Display
90	Battery
100	Analog Device
150	Linear IC
151	Operation. Ampl.
152	Comparator
153	Voltage reg.
200	Digital IC
201	PAL
300	DAC
400	ADC
500	Relay
600	Link
601	Open
651	Resistor Array
652	Capacitor Array
653	Inductor Array
654	Diode Array
655	NPN Trans Array
656	PNP Trans Array
657	Switch Array
658	Jumper Array
659	Transistor Array
660	Led Array
661	Mosfet P Array
662	Mosfet N Array

Device type code	Description
663	Custom Array
664	Jfet P Array
665	Jfet N Array
666	Transform. Array
667	Zener Array
668	Display Array
669	Linear IC Array
670	Opto Coupl
671	Diac Array
672	Scr Array
673	Tranzorb Array
674	Triac Array
675	Varistor Array
700	Connector
750	Switch
751	Jumper
760	Fuse
800	Test Point
801	PAD
802	VIA
805	Fiducial
900	Not Identified
910	Mechanical part
999	Manually Test

4.5 Net list

This section contains the Net list and pins coordinates.

```

.....
:NETLIST
1 ,GND ,R1 ,1 ,4400 ,5400 ,N,1
2 ,VCC ,R1 ,2 ,4600 ,5400 ,N,1
1 ,GND ,D2 ,A ,6400 ,5400 ,N,1
3 ,NET_A ,D2 ,K ,6600 ,5400 ,N,1
3 ,NET_A ,R2 ,1 ,4400 ,5400 ,N,1
2 ,VCC ,R2 ,2 ,4600 ,5400 ,N,1
1 ,VCC ,IC1 ,14 ,7600 ,6150 ,B,2
2 ,GND ,IC1 ,7 ,8400 ,5850 ,B,2
4 ,NET_B ,IC1 ,1 ,7600 ,5850 ,B,2
3 ,NET_A ,IC1 ,2 ,7700 ,5850 ,B,2
5 ,NET_C ,IC1 ,3 ,7800 ,5400 ,B,2
6 ,$NC1 ,IC1 ,4 ,7900 ,5400 ,B,2
:ENDNETLIST
.....

```

The section is delimited by:

- ◆ **NETLIST**
- ◆ **ENDNETLIST**

This section contains one row for each component pin in the board.

The following fields are defined:

Field No.	Field name	Type	
1	Net number	Num 5	
2	Net name	Char * 254	Mandatory
3	Drawing reference	Char * 12	Mandatory
4	Pin name	Char * 5	Mandatory
5	X position	Num 10.3	Mandatory
6	Y position	Num 10.3	Mandatory
7	Pin access side	Char * 1	Mandatory
8	Pad code	Num 5	

* refer to the **Pads** paragraph 4.11.

Pin Access Side

Pin access side	Description
T	Top Board Side
B	Bottom Board Side
N	Not accessible
A	Accessible from Top and Bottom
F	Frame Top
R	Frame Bottom
L	Frame All

The **Pin name** is the component pin number for not polarized components.
In case of polarized components the **Pin name** must be filled as follows:

Device type	Pin function	Pin name
Polarized Capacitor	Positive	P
	Negative	N
Diode	Anode	A
	Catode	K
Zener	Anode	A
	Catode	K
Transistor NPN	Base	B
	Collector	C
	Emitter	E
Transistor PNP	Base	B
	Collector	C
	Emitter	E
Mosfet P	Drain	D
	Source	S
	Gate	G
Mosfet N	Drain	D
	Source	S
	Gate	G
Jfet P	Drain	D
	Source	S
	Gate	G
Jfet N	Drain	D
	Source	S
	Gate	G
SCR	Anode	A
	Catode	K
	Gate	G
Triac	Anode 1	A1
	Anode 2	A2
	Gate	G
Potentiometer	1	1
	2	2
	Cursor	CR
Led	Anode	A
	Catode	K

4.6 Test point

This section contains data concerning the Test points such as Tp numbering, position,

```

.....
:TESTPOINT
1      ,TP1-1      ,VCC      ,TP1      ,1      ,M      ,6      ,6000      ,3400      ,B
2      ,IC1-14     ,VCC      ,IC1      ,14     ,K      ,4      ,7600      ,6150      ,B
3      ,TP2-1      ,GND      ,TP2      ,1      ,M      ,6      ,6800      ,4000      ,B
4      ,VIA1-1     ,GND      ,VIA1     ,1      ,K      ,3      ,6400      ,4000      ,B
5      ,VIA2-1     ,GND      ,VIA2     ,1      ,K      ,3      ,6100      ,4000      ,B
6      ,IC1-4      ,$NC1     ,IC1      ,4      ,M      ,4      ,7900      ,5400      ,B
7      ,IC1-5      , $NC2     ,IC1      ,5      ,M      ,4      ,8000      ,5400      ,B
:ENDTESTPOINT
.....

```

The section is delimited by:

- ◆ **TESTPOINT**
- ◆ **ENDTESTPOINT**

This section contains one row for each defined Test point.
The following fields are defined:

Field No.	Field name	Type	
1	Test point number	Num 5.0	Mandatory
2	Test point name	Char * 12	Mandatory
3	Net name	Char * 254	Mandatory
4	Drawing reference	Char * 12	Mandatory
5	Pin name	Char * 5	Mandatory
6	Test point type code	Num 3.0	Mandatory
7	Contact type code	Num 3.0	Mandatory
8	X position	Num 10.3	Mandatory
9	Y position	Num 10.3	Mandatory
10	Contact side	Char * 1	Mandatory

The **Drawing reference** and the **Pin name** describe the component pin where the Test point is placed.

The **Test point name** is a label used to identify the TP, by default it can be the **Test point number** or the combination of the **Drawing reference** and **Pin name**.

Test point type codes

Test point type code	Description
M	Master (the 1 st TP defined on a net)
K	Kelvin (all the other TP on the net)
MU	Master not positioned
KU	Kelvin not positioned

Contact type codes

Code	Description
1	Through Hole Pin
2	SMD Pin
3	Pad
4	Via
8	Connector
10	Test point

Contact sides

Side	Description
T	Top
B	Bottom

① Note: In case of Panel of boards, the Test point list will contain all the TPs of the panel.

4.7 Variants

This section contains data concerning the variants of the board.

```
.....  
:VARIANT  
0, STANDARD  
:ENDVARIANT  
.....
```

The section is delimited by:

- ◆ **VARIANT**
- ◆ **ENDVARIANT**

This section contains one row for each defined variant.
The following fields are defined:

Field No.	Field name	Type	
1	Variant code	Num 3.0	Mandatory
2	Variant name	Char * 12	Mandatory

① **Note:** This section is present in the file only in case of variant board.

4.8 Panel of board

This section contains data concerning the Panel of boards.

The section is delimited by:

- ◆ **PANEL**
- ◆ **ENDPANEL**

This section contains one row for each board defined in the panel.
The following fields are defined:

Field No.	Field name	Type	
1	Panel ID	Num 3.0	Mandatory
2	Offset X	Num 10.3	Mandatory
3	Offset Y	Num 10.3	Mandatory
4	Rotation	Num 3.0	Mandatory
5	Offset TP	Num 5.0	Mandatory

① **Note:** This section is present in the file only in case of Panel of board.

4.9 Case types

This section contains data concerning the Case types.

```

.....
:PACKAGES
SOT23      ,TH ,400,600,100
DIL300     ,SMD,700,300,120
TP         ,SMD,50,50,0
VIA_100    ,TH,100,75,0
:ENDPACKAGES
.....

```

The section is delimited by:

- ◆ **PACKAGES**
- ◆ **ENDPACKAGES**

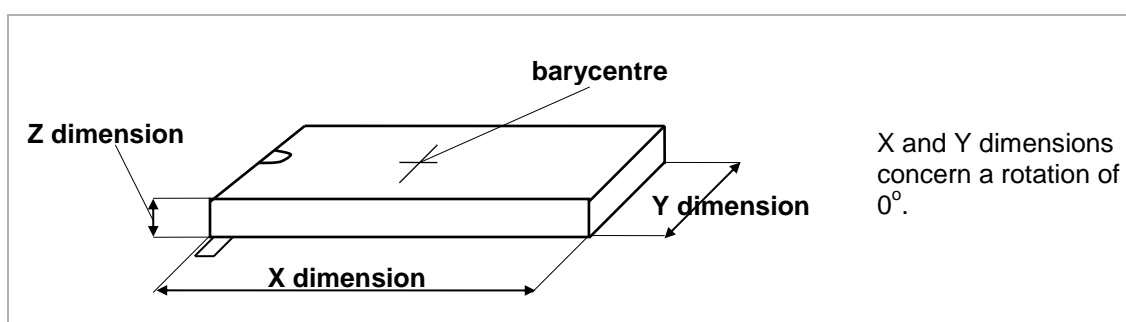
This section contains one row for each defined variant.
The following fields are defined:

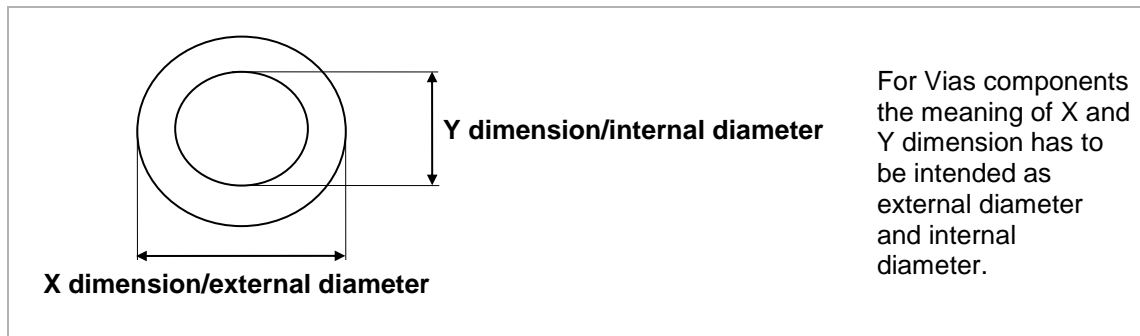
Field No.	Field name	Type	
1	Case name	Char 16	Mandatory
2	Package type	Char 3	Mandatory
3	Component X dimension	Num 10.3	Mandatory
4	Component Y dimension	Num 10.3	Mandatory
5	Component Z dimension	Num 10.3	Mandatory

Package type

Package type	Description
TH	Through Hole
SMD	SMD

Component dimensions



Component dimensions for Vias

4.10 Package pins

This section contains data concerning pins coordinates of the Case types.

```

.....
:PACKAGE_PINS
C_100_90 ,1          ,A1          ,100          ,-1500          ,200
C_100_90 ,2          ,A2          ,100          ,-1400          ,200
C_100_90 ,3          ,A3          ,100          ,-1300          ,200
C_100_90 ,4          ,A4          ,100          ,-1200          ,200

C_100_90 ,30         ,A30         ,100          ,1500          ,200
C_100_90 ,31         ,B1          ,100          ,-1500          ,200
C_100_90 ,32         ,B2          ,100          ,-1400          ,400
C_100_90 ,33         ,B3          ,100          ,-1300          ,200
C_100_90 ,34         ,B4          ,100          ,-1200          ,400

C_100_90 ,60         ,B30         ,100          ,1500          ,200
:ENDPACKAGE_PINS
.....

```

The section is delimited by:

- ◆ **PACKAGE_PINS**
- ◆ **ENDPACKAGE_PINS**

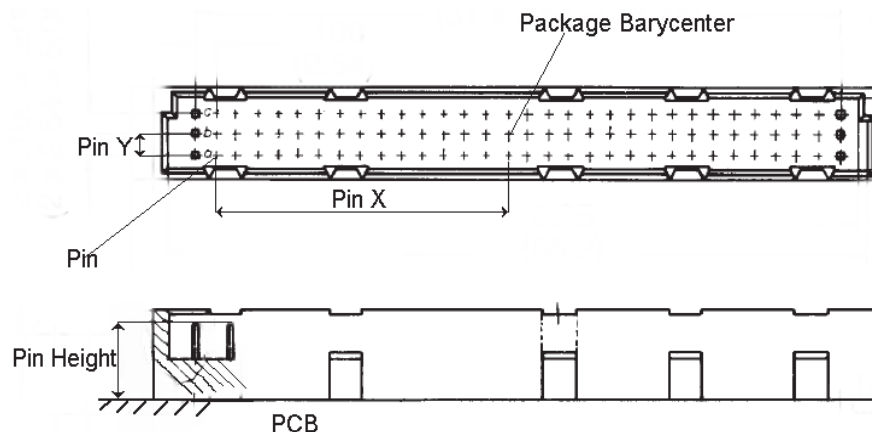
This section contains one row for each defined variant.

The following fields are defined:

Field No.	Field name	Type	
1	Case name	Char 16	Mandatory
2	Pin ID	Num 5	Mandatory
3	Pin name	Char 5	Mandatory
4	Pin X	Num 10.3	Mandatory
5	Pin Y	Num 10.3	Mandatory
6	Pin height	Num 10.3	Mandatory

Pin X and **Pin Y** are the coordinates offset concerning the package barycenter at 0 degrees rotation.

Pin height specifies the height of the pin concerning the board surface.



4.11 Pads

This section contains data concerning the Pads.

```

.....
:PAD
1 ,PAD1          ,RECT ,50,150,25,75
2 ,PAD2          ,RECT ,150,100,75,50
3 ,PAD3          ,CIRCLE,50,50.25,25
4 ,PAD4          ,CIRCLE,50,50,25,25
:ENDPAD
.....

```

The section is delimited by:

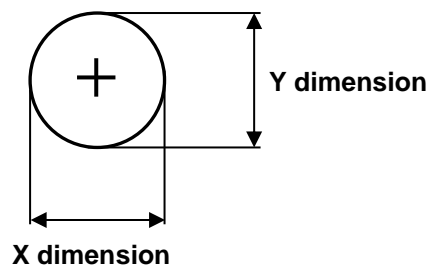
- ◆ **PAD**
- ◆ **ENDPAD**

This section contains one row for each defined Pad.
The following fields are defined:

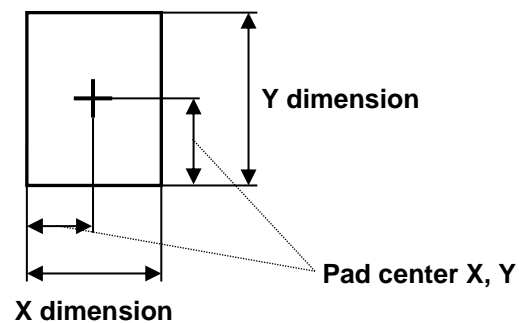
Field No.	Field name	Type	
1	Pad code	Num 5	Mandatory
2	Pad name	Char 16	Mandatory
3	Pad shape	Char 6	Mandatory
4	Pad X dimension	Num 10.3	Mandatory
5	Pad Y dimension	Num 10.3	Mandatory
6	Pad center X	Num 10.3	Mandatory
7	Pad center Y	Num 10.3	Mandatory

Pad shape

Pad shape	Description
CIRCLE	Circle
RECT	Rectangle



For Oval Pads $X \neq Y$



For Square Pads $X = Y$

4.12 Wiring

This section contains the list of net segment and the data concerning the wirings.

```
.....  
:WIRING  
GND      ,VIA1      ,1      ,IC4      ,6      ,1  
GND      ,VIA2      ,1      ,IC4      ,6      ,2  
:ENDWIRING  
.....
```

The section is delimited by:

- ◆ **WIRING**
- ◆ **ENDWIRING**

This section contains one row for each defined Wiring.
The following fields are defined:

Field No.	Field name	Type	
1	Net name	Char * 254	Mandatory
2	Drawing start	Char * 12	Mandatory
3	Pin start	Char * 5	Mandatory
4	Drawing end	Char * 12	Mandatory
5	Pin end	Char * 5	Mandatory
6	Route index	Num 6	Mandatory

4.13 Routing

This section contains the coordinates and size of each segment and the data concerning the routing coordinates.

```

:ROUTING
1      ,1000      ,5600      ,8000      ,5600      ,50      ,1
1      ,8000      ,5600      ,9000      ,4600      ,100      ,1
1      ,9000      ,4600      ,12000     ,4600      ,50      ,1
1      ,12000     ,4600      ,12000     ,4800      ,50      ,1
2      ,12000     ,4600      ,16000     ,4600      ,50      ,1
2      ,16000     ,4600      ,17000     ,5000      ,50      ,1
:ENDROUTING

```

The section is delimited by:

- ◆ **ROUTING**
- ◆ **ENDROUTING**

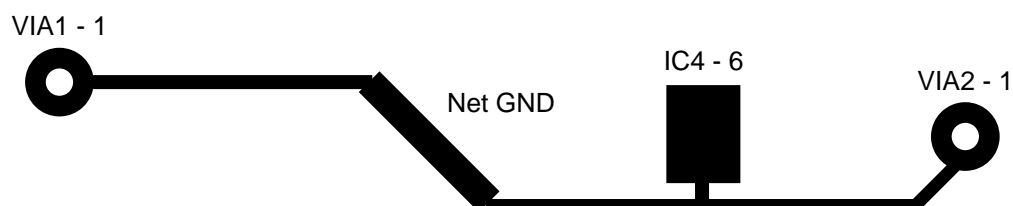
This section contains one row for each defined Routing.
The following fields are defined:

Field no.	Field name	Type	
1	Route index	Num 6	Mandatory
2	X start	Num 10.3	Mandatory
3	Y start	Num 10.3	Mandatory
4	X end	Num 10.3	Mandatory
5	Y end	Num 10.3	Mandatory
6	Width	Num 10.3	Mandatory
7	Layer	Num 4	Mandatory

Layer 1 is the **TOP** layer, **layer 2** is the **BOTTOM** layer.

Layer 3 to **layer <n>** are internal layers from the **TOP** to the **BOTTOM**.

Example:



4.14 Board Outline

This section contains data concerning routing coordinates.

```

.....
:BOARDOUTLINE

1,      1000      ,100      ,5000      ,100
1,      1000      ,100      ,5000      ,100
3,      5000      ,6000      ,200      ,6000
4,      200      ,6000      ,200      ,1500
5,      200      ,1500      ,1000      ,100

:ENDBOARDOUTLINE
.....

```

The section is delimited by:

- ◆ **BOARDOUTLINE**
- ◆ **ENDBOARDOUTLINE**

This section contains one row for each defined Board Outline.
The following fields are defined:

Field No.	Field name	Type	
1	Line ID	Num 5	Mandatory
2	X start	Num 10.3	Mandatory
3	Y start	Num 10.3	Mandatory
4	X end	Num 10.3	Mandatory
5	Y end	Num 10.3	Mandatory

Example:

