CadPack

Import from Ariadne

Software tool for import from Ariadne Cad format

Technical Info

Version : 2
Code : 81190399.202

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Contents

Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

Both Bed of Nails and Flying Probe testers, require the circuit information available on CAD format, in order to generate the ICT test program in a short time and without errors.

The Import from Ariane CAD import driver allows to import data present in Ariadne CAD file and convert them in SPEA Board data format.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

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1. Ariadne file data

With the “Ariadne CAD files” words we refer to the output information generated by the Ariadne CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Ariadne CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movements for Flying Probes).

Information can be grouped in 4 different categories and typically concern the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is presentation of the electrical diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information above mentioned SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: - **Top** (Component side) - **Bottom** (Soldering side) - **Not mounted Top** - **Not mounted Bottom**
Rotation [1]	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code [1]	Device package (case) code.

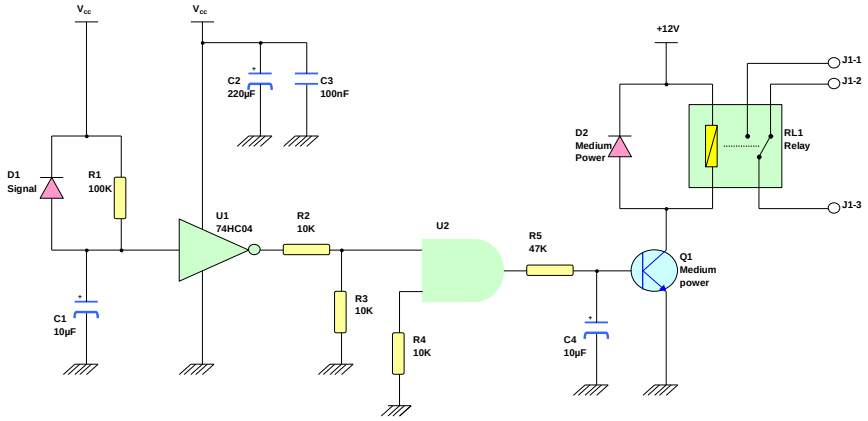
[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagram.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: - **Top** (Device side access). - **Bottom** (Soldering side access). - **Not accessible** - **All** (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

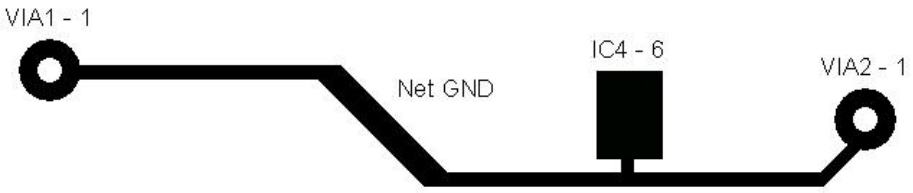
1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



[1] **Optional data**

2. Ariadne file generalities

2.1 Ariadne file name

The Ariadne Neutral file name has to have the **.PCA** extension.
It is an ASCII text file and it contains the information related to the board, device and their connections.

2.2 Ariadne file conversion from Unix to MS-DOS

When the diagram entry has been entered and checked on the Ariadne CAD workstation, the Ariadne **.PCA** file should be made available for the SPEA system.

The SPEA system is based on a PC platform operating in a Windows® environment, this means that the CAD import driver can manage ASCII Text file in MS-DOS format.

Due to the fact that the Ariadne workstation typically uses the Unix operating system, the output ASCII text file has to be converted from Unix to MS-DOS format.

In order to perform the conversion, please refer to appendix A – **Note about the Ariadne ASCII text file format**.

3. Ariadne file format

This is a partial extract of an example of an Ariadne output ASCII text file:

```
*ARIADNE*  DATEI INFORMATIONEN

*VERSION* 8.5 pcb
*UNIT* mm
……


*PARTDECAL*  TEILE
*REMARK*   Name Anz.-Terminals Anz.-Padbeschr. Breite Typ Bestückungspunkt(X/Y)
*REMARK*   Art [<Option>] "LINE" or "FULL"
*REMARK*   X-Pos. Y-Pos. ["ARC" Radius]
*REMARK*   Bezugspunkt(X-Koord.,Y-Koord) Drehung Spiegelung Höhe Breite Lage
*REMARK*   T X-Pos. Y-Pos. 0 Pinname(X-Pos. Y-Pos. Orientation [Mirror])
*REMARK*   PAD PIN FINGER
*REMARK*   EBENE GROESSE FORM F-NP F-LAENGE F-VERSATZ BOHRUNG
*REMARK*   EBENE GROESSE FORM BOHRUNG

@ELKOC    2 1 0.1016 <SMD> 0 0
NN -1.8034 -2.9718 0 N 1.27 0.254
NT -1.8034 -4.3688 0 N 1.27 0.254
N1 0 0 0 N 1.9812 0.254
N2 0 0 0 N 1.9812 0.254
N3 0 0 0 N 1.9812 0.254
TS 1.905 0.254
T -2.65 0 0 -3.1072 1.4478 0
T 2.65 0 0 2.1166 1.524 0
……

END

@SOD80-DI-ZD 2 1 0.1016 <SMD> 0 0
NN -2.1844 -3.3274 0 N 1.27 0.254
NT -2.159 -4.8768 0 N 1.27 0.254
N1 0 0 0 N 1.9812 0.254
N2 0 0 0 N 1.9812 0.254
N3 0 0 0 N 1.9812 0.254
TS 1.9812 0.254
T -1.36 0 0 -1.8426 1.8542 0
T 1.36 0 0 0.9536 1.905 0
……

END

@SO8      8 1 0.1016 <SMD> -0.0254 0
NN 0 -8.128 0 N 1.905 0.254
NT 0 -10.668 0 N 1.905 0.254
N1 0 0 0 N 0 0
N2 0 0 0 N 0 0
N3 0 0 0 N 0 0
TS 1.905 0.254
T -1.905 -2.413 0 -2.54 -5.588 0
T -0.635 -2.413 0 -1.27 -5.588 0
T 0.635 -2.413 0 0 -5.588 0
T 1.905 -2.413 0 1.27 -5.588 0
T 1.905 2.413 0 1.905 3.937 0
T 0.635 2.413 0 0 3.937 0
T -0.635 2.413 0 -1.905 3.937 0
T -1.8796 2.413 0 -3.7846 3.937 0
……

END

@0805-DI  2 1 0.1016 <SMD> 0 0
NN -1.7526 -2.1844 0 N 1.27 0.254
NT -1.8542 -4.1656 0 N 1.27 0.254
N1 0 0 0 N 1.9812 0.3048
N2 0 0 0 N 1.9812 0.3048
N3 0 0 0 N 1.9812 0.3048
TS 1.9812 0.3048
T -0.9652 0.0254 0 -1.5748 1.4224 0
T 0.9398 0.0254 0 0.508 1.3716 0
……
END
```

```
……


*PARTTYPE*  TEILE
*REMARK*   Name Technologie Familie Zusatzzeilen Anzahl-Bauformen Anzahl-Gatter
*REMARK*   Gatter-Typ Tausch-Gruppe Anzahl-Pins
*REMARK*   Symbol-Pinnr.,Decal-Pinnr.,Pin-Name,Tausch-Gruppe,Pin-Typ,Signal,Breite

@ZMM39    ANA ZDIODE 1 1 1
#Zdiode-2,7V
:SOD80-DI-ZD
G 0 2   :ZDIODE-DI
1,1,K,0,u,
2,2,A,0,u,

@TDE1707  DRIVER ENDSTUFE 1 1 1
#NPN/PNP Endstufe
:SO8
G 0 8   :TDE1707
1,6,6,0,o,
2,5,5,0,i,
3,3,3,0,i,
4,4,4,0,g,GND
5,2,2,0,o,
6,8,8,0,i,
7,1,1,0,o,
8,7,7,0,i,

@10U      ANA 0! 2 19 1
# Class: C
# Date : 16. DEC 93
:C010B010:C020B010:C050B010:0805-W:0805-R:1206-W:1206-R
:C020B015:1210-R:1210-W:C020B018:C020X028:CK05-CK06:1812-R
:1812-W:ELKOA:ELKOB:ELKOC:ELKOD
G 0 2   :C-X:C-Y
1,1,1,1,U,
2,2,2,1,U,

@10K      ANA 0! 2 15 1
# Class: R
# Date : 18. JAN 93
:R040B010:R050B010:1206-R:1206-W:0805-R:0805-W:R030B010
:MINIMELF-R:MINIMELF-W:R020B017:MCR03-R:MCR03-W:R020B010
:0805-DI:1206-DI
G 0 2   :R-X:R-Y
1,1,1,1,U,
2,2,2,1,U,

……




*PART*  TEILE
*REMARK*   BAUTEIL-NM BAUTYP-NM  X Y NP FIX SPIEGELN  NM-X NM-Y NM-NP
@D2       ZMM39:SOD80-DI-ZD 34.189264 11.57 0 M F
NN -0.400736 1.46 0 N 0.8 0.08
NT -2.159 -4.8768 0 N 1.27 0.254
N1 0 0 0 N 1.9812 0.254
N2 0 0 0 N 1.9812 0.254
N3 0 0 0 N 1.9812 0.254
TS 1.9812 0.254
@IC2      TDE1707:SO8 8.484972 6.751366 180 M F
NN 0.555028 -0.308634 180 N 0.8 0.08
NT 0 -10.668 0 N 1.905 0.254
N1 0 0 0 N 1.9812 0.3048
N2 0 0 0 N 1.9812 0.3048
N3 0 0 0 N 1.9812 0.3048
TS 1.905 0.254
@C17      10U:ELKOC 42.65 26.48 90 M F
NN -0.47 0.55 270 N 0.8 0.08
NT -1.8034 -4.3688 0 N 1.27 0.254
N1 0 0 0 N 1.9812 0.254
N2 0 0 0 N 1.9812 0.254
N3 0 0 0 N 1.9812 0.254
TS 1.905 0.254
@R7       10K:0805-DI 24.581206 4.167932 270 M U
NN 0.447932 -0.408794 90 N 0.8 0.08
NT -1.8542 -4.1656 0 N 1.27 0.254
N1 0 0 0 N 1.9812 0.3048
N2 0 0 0 N 1.9812 0.3048
N3 0 0 0 N 1.9812 0.3048
TS 1.9812 0.3048
```

```
……….


*ROUTE*  LEITERBAHN
*REMARK*   *SIGNAL*  SIGNALNAME MIT FLAGS
*REMARK*   BAUTEILNAME.PIN BAUTEILNAME.PIN
*REMARK*   X-Pos. Y-Pos. [Via-Nr/Type]Ebene SEGMENTBREITE
*SIGNAL* $155 0.3048
R1.1 R2.1 R
 12.94445 4.39323 L2
 12.94445 4.390944
 12.940132 4.390944 END
IC2.8 R2.1 R
 6.605372 4.338366 L2
 6.605372 3.185968
 6.928714 2.88828
 11.403432 2.88828
 11.81923 3.439714
 11.81923 3.852464
 12.36279 4.396024
 12.49868 4.260134
 12.940132 4.390944 END
*SIGNAL* GND 0.3048
<JP> 1 <JP> 1 R
 32.735368 12.57 L1 0.2
 32.735368 12.69 0.3048
 35.811054 12.69
 36.16259 12.36375
 36.16259 11.272566
 36.179608 11.189508 END
<JP> 1 <JP> 1-2 R
 32.735368 12.57 L1 0.2
 32.84 12.58 0.3048
 32.83 12.69
 31.58 12.69
 31.33786 12.506498 VS1 END
……….

*END*  der ASCII-OUTPUT Datei
```

The Import from Ariadne CAD driver can correctly identify and use the following sections:

- **Unit**
- **Part**
- **Part decal**
- **Part type**
- **Route**

In the next paragraphs, a short description for each section is provided.

3.1 Unit

The **UNIT** identifier is used to specify the used unit of measurement for coordinates and dimensions.

Valid values are:

- **MM** to specify that all the coordinates and dimensions are expressed in millimeter
- **INCH** to specify that all the coordinates and dimensions are expressed in inches
- **MIL** to specify that all the coordinates and dimensions are expressed in mils (inches/1000)
- **CMIL** to specify that all the coordinates and dimensions are expressed in cent of mils (inches/100000)
- **MY** to specify that all the coordinates and dimensions are expressed in micrometer (mm/1000)
- **NM** to specify that all the coordinates and dimensions are expressed in nanometer (mm/100000)

The following example shows the used syntax for the **UNIT** identifier:

```
……….
UNIT mm
……….
```

3.2 Part

The component section is introduced by the ***PART*** keyword.

Basically this section contains the part list and mounting data of each single device present in the Ariadne CAD file; data are separated by blanks.

Every single row of the Ariadne file, in this section, contains the following information:

1. **Drawing reference**
2. **Part number**
    - Value of Device name
    - Package name
3. **X-coordinate**
4. **Y-coordinate**
5. **Rotation**
6. **Mount side**
7. Not used

The following example shows the syntax used for the **Part** section:

1	2		3	4	5	6	7
Drawing ref.	Part number		X-coord.	Y-coord.	Rotation	Mounting side	Not used
	Value or Device name	Package name					
IC2	TDE1707:S08		34.189264	11.57	0	M	F
	TDE1707	S08					
C17	10U:ELKOC		42.65	26.48	90	M	
	10u	ELKOC					

Part section is shown in the following example:

```
.....
*PART*  TEILE
*REMARK*   BAUTEIL-NM BAUTYP-NM  X Y NP FIX SPIEGELN  NM-X NM-Y NM-NP
@IC2      TDE1707:SO8 8.484972 6.751366 180 M F
NN 0.555028 -0.308634 180 N 0.8 0.08
NT 0 -10.668 0 N 1.905 0.254
N1 0 0 0 N 1.9812 0.3048
N2 0 0 0 N 1.9812 0.3048
N3 0 0 0 N 1.9812 0.3048
@C17      10U:ELKOC 42.65 26.48 90 M
NN -0.47 0.55 270 N 0.8 0.08
NT -1.8034 -4.3688 0 N 1.27 0.254
N1 0 0 0 N 1.9812 0.254
N2 0 0 0 N 1.9812 0.254
N3 0 0 0 N 1.9812 0.254
TS 1.905 0.254
.....
```

3.3 Part decal

The Part decal section is introduced by the ***PARTDECAL*** keyword.

This section is used to describe the package properties (name, number of pins, type); data are separated by blanks in a row of the Ariadne file.

The “Import from Ariadne” import CAD driver manages the following data:

1. **Package name**
2. **Pin count**
3. Not used
4. Not used
5. **Package type**
6. Not used
7. Not used

The coordinates of the pins are described in a section part. This part is introduced by the **T** keyword.
This line contains the offset of the pin. This offset is referred to the package barycentre.

The following example shows the syntax used for the **Part decal** section:

1	2	3	4	5	6	7
Package name	Pin count	Not used	Not used	Package type	Not used	Not used
SO8	8	1	0.1016	<SMD>	-0.0254	0

The following example shows the syntax used for the **Terminal** section:

1	2	3	4	5	6	7
Not used	X offset	Y offset	Not used	Not used	Not used	Not used
T	-1.905	-2.413	0	-2.54	-5.588	0
T	-0.635	-2.413	0	-1.27	-5.588	0
T	0.635	-2.413	0	0	-5.588	0
T	1.905	-2.413	0	1.27	-5.588	0
T	1.905	2.413	0	1.905	3.937	0
T	0.635	2.413	0	0	3.937	0
T	-0.635	2.413	0	-1.905	3.937	0
T	-1.8796	2.413	0	-3.7846	3.937	0

Part decal section is shown in the following example:

```
.....
@SO8       8 1 0.1016 <SMD> -0.0254 0
NN 0 -8.128 0 N 1.905 0.254
NT 0 -10.668 0 N 1.905 0.254
N1 0 0 0 N 0 0
N2 0 0 0 N 0 0
N3 0 0 0 N 0 0
TS 1.905 0.254
T -1.905 -2.413 0 -2.54 -5.588 0
T -0.635 -2.413 0 -1.27 -5.588 0
T 0.635 -2.413 0 0 -5.588 0
T 1.905 -2.413 0 1.27 -5.588 0
T 1.905 2.413 0 1.905 3.937 0
T 0.635 2.413 0 0 3.937 0
T -0.635 2.413 0 -1.905 3.937 0
T -1.8796 2.413 0 -3.7846 3.937 0
.....
END
.....
```

3.4 Part type

The Part type section is introduced by the ***PARTTYPE*** keyword.

This section is used to describe the device pin properties (pin name); data are separated by blanks in a row of the Ariadne file.

The “Import from Ariadne” import CAD driver manages the following data:

1. **Part type**
2. Not used
3. Not used
4. Not used
5. Not used
6. Not used

In this section there is the **G** keyword that indicates the number of gates. The following lines contain the pin properties.

The “Import from Ariadne” import CAD driver manages the following data:

1. Not used
2. **Pin number**
3. **Pin name**
4. Not used
5. Not used
6. Not used

The following example shows the syntax used for the **Part type** section:

1	2	3	4	5	6
Part type	Not used	Not used	Not used	Not used	Not used
ZMM39	ANA	ZDIODE	1	1	1

The following example shows the syntax used for the **Gate** section:

1	2	3	4	5	6
Not used	Pin number	Pin name	Not used	Not used	Not used
1	1	K	0	u	
2	2	A	0	u	

Part type section is shown in the following example:

```
.....
@ZMM39    ANA ZDIODE 1 1 1
#Zdiode-2,7V
:SOD80-DI-ZD
G 0 2   :ZDIODE-DI
1,1,K,0,u,
2,2,A,0,u,
.....
```

3.5 Route

The track section is introduced by the ***ROUTE*** keyword.

This section is used to specify the properties for the tracks data (layer name, net coordinates, net width, net name).

Data are separated by blanks in a row of the CAD file and the “Import from Ariadne” import CAD driver manages the following labels:

1. **Drawing reference start**
2. **Pin name start**
3. **Drawing reference end**
4. **Pin name end**
5. **X coordinate**
6. **Y coordinate**
7. **Layer**
8. **Net width**

ⓘ Notes:

- The **VS1** keyword indicates the presence of the via, in the current coordinates.
- The **JP** keyword is an arbitrary point where some routes run together. It isn’t a via or a component.

Each list of items is introduced by a ***SIGNAL*** keyword which specifies the signal net they refer to and optional a width which becomes the minimum track width for routes to connect the items following.

The data are separated by blanks in a row of the CAD file and the “Import from Ariadne” import CAD driver manage the following labels:

1. **Net name**
2. **Net width**

The following example shows the syntax used for the **Route** section:

1	2	3	4	5	6	7	8
Drawing ref. start	Pin name start	Drawing ref. end	Pin name end	X-coord.	Y-coord.	Net width	Layer
R1	1	R2	1				
				12.94445	4.39323		L2
<JP>	1	<JP>	1				
				32.735368	12.69	0.3048	

The following example shows the syntax used for the **Signal** section:

1	2
Net name	Net width
$155	0.3048

Route section is shown in the following example:

```
……
*ROUTE*  LEITERBAHN
*REMARK*   *SIGNAL*  SIGNALNAME MIT FLAGS
*REMARK*   BAUTEILNAME.PIN BAUTEILNAME.PIN
*REMARK*   X-Pos. Y-Pos. [Via-Nr/Type]Ebene SEGMENTBREITE
*SIGNAL* $155 0.3048
R1.1 R2.1 R
 12.94445 4.39323 L2
 12.94445 4.390944
 12.940132 4.390944 END
IC2.8 R2.1 R
 6.605372 4.338366 L2
 6.605372 3.185968
 6.928714 2.88828
 11.403432 2.88828
 11.81923 3.439714
 11.81923 3.852464
 12.36279 4.396024
 12.49868 4.260134
 12.940132 4.390944 END
*SIGNAL* GND 0.3048
<JP> 1 <JP> 1 R
 32.735368 12.57 L1 0.2
 32.735368 12.69 0.3048
 35.811054 12.69
 36.16259 12.36375
 36.16259 11.272566
 36.179608 11.189508 END
<JP> 1 <JP> 1-2 R
 32.735368 12.57 L1 0.2
 32.84 12.58 0.3048
 32.83 12.69
 31.58 12.69
 31.33786 12.506498 VS1 END
……
```

4. Import setting

4.1 Pin function assignment

This assignment table must be filled, in order to correctly execute the CAD file import.

In order to correctly test some polarized devices such as diodes, bipolar transistors, etc., it is basic to correctly identify the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table, are described below:

Field	Description
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Pin Function	Function concerning the Pin.
Pin Name	Pin reference.
Cad Pin	Pin reference in Cad file.

4.2 Drawing ref. initials/device type assignment

The Ariadne file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the test program generation point of view.

The fields contained in the table are described below:

Field	Description
Drawing Reference	Initial letter identifying the **Device Type**.
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Default Tol+, Tol-	Value and tolerance of the device only if required (as for resistors).

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.

A. Note about the Ariadne ASCII text file format

The Ariadne CAD-CAE typically runs under Unix operating system and generates its neutral ASCII output file in Unix format.

The Unix ASCII text files use the "$0a_{hex}$"ASCII character as end of line identifier.
The Windows® (MS-DOS) operating system uses the "$0d_{hex}$" and "$0a_{hex}$" ASCII characters as end of line identifier for ASCII text files.
This means that output ASCII text files may require an ASCII format conversion (from Unix to Windows® format).

This operation can be performed using "WordPad", a standard text file editor.
Open the Ariadne ASCII file with this editor and save it, this operation will automatically perform the conversion from ASCII Unix format to ASCII Windows® format.