CadPack

Import from Mentor

Software tool for import from Mentor Cad format

Technical Info

Version : 2
Code : 81190409.145

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Contents

Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The Import from Mentor CAD import driver allow to import the data present in the Mentor CAD file and convert them in the SPEA Board data format.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

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1. Mentor file data

With the “Mentor CAD files” words we refer to the output information generated by the Mentor CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Mentor CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movement for Flying Probes).

Information can be grouped in 4 different categories and typically concern the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is presentation of the electrical diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information above mentioned SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: - **Top** (Component side) - **Bottom** (Soldering side) - **Not mounted Top** - **Not mounted Bottom**
Rotation [1]	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code [1]	Device package (case) code.

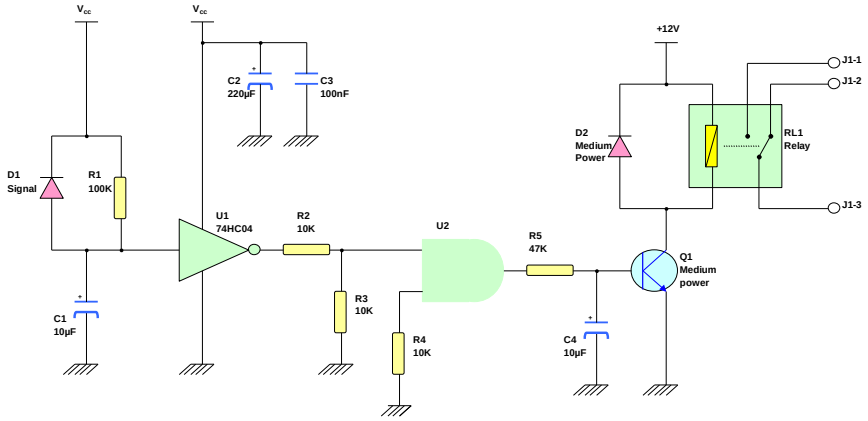
[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: - **Top** (Device side access). - **Bottom** (Soldering side access). - **Not accessible** - **All** (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

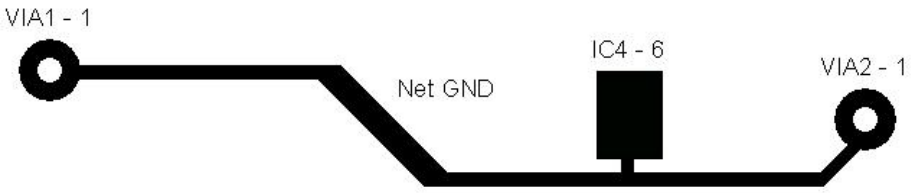
1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



[1] **Optional data**

2. Mentor file generalities

2.1 Mentor file name

The Mentor Neutral file name has to have the **.CMP** extension.
It is an ASCII text file and it contains the information concerning the board, devices and their connections.

It is possible to import the tracks of the board by using the Mentor track file with **.TRC** extension.
It is an ASCII text file and it contains the information concerning the Wiring and Routing list of the board.

ⓘ **Note:** If the **.TRC** file is not present, only Part List and Net List will be loaded.

2.2 Mentor file conversion from Unix to MS-DOS

When the diagram entry has been performed and checked on the Mentor CAD workstation, the Mentor file **.CMP** should be made available for the SPEA system.

The SPEA system is based on a PC platform operating in a Windows® environment, this means that the CAD import driver can manage ASCII Text file in MS-DOS format.

Due to the fact that the Mentor workstation typically uses the Unix operating system, the output ASCII text file has to be converted from Unix to MS-DOS format.

In order to perform the conversion, please refer to appendix A – **Note about the Mentor ASCII text file format**.

3. Mentor "CMP" file format

This is a partial extract of an example of a Mentor output ASCII text file:

```
B_UNITS Inches
B_ATTR 'DRILL_ORIGIN' ''  0.0 0.0
B_ATTR 'MILLING_ORIGIN' ''  0.0 0.0
B_ATTR 'BOARD_PLACEMENT_KEEPOUT' 'place_2'  2.81496 1.2874 2.81496 1.23228 2.84646 1.20079
2.90157 1.20079 2.93307 1.23228 2.93307 1.2874 -
2.90157 1.3189 2.84646 1.3189 2.81496 1.2874
B_ATTR 'BOARD_PLACEMENT_KEEPOUT' 'place_2'  4.0748 2.70472 4.0748 2.64961 4.1063 2.61811 4.16142
2.61811 4.19291 2.64961 4.19291 2.70472 -
4.16142 2.73622 4.1063 2.73622 4.0748 2.70472
B_ATTR 'BOARD_PLACEMENT_KEEPOUT' 'place_2'  2.81496 2.70472 2.81496 2.64961 2.84646 2.61811
2.90157 2.61811 2.93307 2.64961 2.93307 2.70472 -
2.90157 2.73622 2.84646 2.73622 2.81496 2.70472
……
##############################################
###Nets Information
##############################################
NET +10V
N_PROP  (PCB_BA_NAME,"+10V")
N_PIN Z7-1 0.25 2.25 pad_060 0
N_PIN R198-1 0.81 5.125 s40x62   1
N_PIN R220-1 0.41 5.0 s40x62   1
N_PIN C164-2 0.31 5.0 s48x76   1
N_PIN V29-1 0.225 5.16 s90x100   1
N_VIA 0.225 5.075 via_030   1  10
N_VIA 0.75 5.125 via_030   1  10
N_TEST PIN 0.25 2.25 BOT pad_060 Z7-1
……
##############################################
###Component Information
##############################################
COMP C1 3CE101 100n c050802e  4.3      2.65     1   0
C_PROP (DES,"X7R") (TOLL,"20-20") (SPEA,"10") (VALUE,"100n")
C_PIN C1-1 4.3      2.65     0  1  0 pad_10_22_sx /N$130
C_PIN C1-2 4.5      2.65     0  1  0 pad_10_22_dx GROUND
COMP C2 3CE101 Kiie42 c050802e  0.55     0.3      0 270
C_PROP (TOLL,"20-20") (SPEA,"10") (VALUE,"100n")
C_PIN C2-1 0.55     0.3      0  1 270 pad_10_22_sx GROUND
C_PIN C2-2 0.55     0.1      0  1 270 pad_10_22_dx /N$124
COMP C3 3CE100 10n c050802e  1.55     0.1      1 180
C_PROP (VALUE”100n")  (TOLL,"20-20") (SPEA,"10")
C_PIN C3-1 1.55     0.1      0  1 180 pad_10_22_sx 12V
C_PIN C3-2 1.35     0.1      0  1 180 pad_10_22_dx GROUND
COMP C4 3CE101 100n c050802e  2.1      0.1      1 180
C_PROP (VALUE”100n") (TOLL,"20-20") (SPEA,"10")
C_PIN C4-1 2.1      0.1      0  1 180 pad_10_22_sx GROUND
……
##############################################
###Pad Information
##############################################
PAD PIN chip0805_b Surf none PHYSICAL_1 PHYSICAL_1 PHYSICAL_14 PHYSICAL_14
P_SHAPE chip0805_b PHYSICAL_1 RECTANGLE 1.21 1.01
P_SHAPE chip0805_b PHYSICAL_14 RECTANGLE 1.42 1.22
PAD PIN chip0805_t Surf none PHYSICAL_1 PHYSICAL_1 PHYSICAL_14 PHYSICAL_14
P_SHAPE chip0805_t PHYSICAL_1 RECTANGLE 1.22 1.02
P_SHAPE chip0805_t PHYSICAL_14 RECTANGLE 1.42 1.22
PAD PIN chip1206_b Surf none PHYSICAL_1 PHYSICAL_1 PHYSICAL_14 PHYSICAL_14
P_SHAPE chip1206_b PHYSICAL_1 RECTANGLE 1.58 1.28
P_SHAPE chip1206_b PHYSICAL_14 RECTANGLE 1.78 1.48
……
```

```
##########################################
###Board Added Part Information
##########################################
B_ADDP  fiducial 'fiducial' 12.45 2.5    0   1   1   1
B_ADDP  fiducial 'fiducial' 0.2 2.5    0   1   1   1
B_ADDP  fiducial 'fiducial' 0.2 -2.5    0   1   1   1
##########################################
###TESTPOINTS
##########################################
FIXTURE GENERIC_FIXTURE_BOTTOM 0.0 0.0 BOT 0 None
F_ATTR 'TEST_FIXTURE_IS_MAPPED' ''   1
FIXTURE GENERIC_FIXTURE_TOP 0.0 0.0 TOP 0 None
T_TEST VIA /LCT 3.520 -2.41 BOT v026rd_040_tp INSERTED []
[TP16(IN,0.0,0.0,0,TL,0.1,0.1,0.01,std,1)]
T_TEST VIA /N$58 5.456 2.075 BOT v02rd_04_tp INSERTED []
[TP168(IN,0.0,0.0,0,TL,0.1,0.1,0.01,std,1)]
T_TEST VIA /VID 7.612 -1.9 BOT v02rd_04_tp INSERTED []
[TP149(IN,0.0,0.0,0,TL,0.15,0.15,0.01,std,1)]
T_TEST VIA /N$60 6.429 2.6 BOT v02rd_04_tp INSERTED []
[TP1(IN,0.0,0.0,0,TL,0.15,0.15,0.01,std,1)]
T_TEST PIN /COMMAND(8) 6.1 -0.1 BOT t050rd IC29-20 []
[TP71(IN,0.0,0.0,0,BL,0.15,0.15,0.01,std,1)]
T_TEST PIN /COMMAND(5) 6.1 0.1 BOT t050rd IC29-22 []
[TP70(IN,0.0,0.0,0,BL,0.15,0.15,0.01,std,1)]
T_TEST PIN /ADR(3) 5.5 0.0 BOT t050rd IC29-8 [] [TP68(IN,0.0,0.0,0,BL,0.15,0.15,0.01,std,1)]
T_TEST PIN /N$1138 7.2 1.9 BOT t050rd I2-1 [] [TP21(IN,0.0,0.0,0,BL,0.15,0.15,0.01,std,1)]
```

The Import from Mentor CAD driver can correctly identify and use the following labels (identifiers):

- **COMP**
- **C_PROP**
- **C_PIN**
- **B_UNITS**
- **T_TEST VIA**
- **T_TEST PIN**
- **PAD PIN**
- **P_SHAPE**
- **N_VIA**
- **N_TEST VIA**
- **N_TEST PIN**
- **B_ADDP**

In the next paragraphs, a short description for each label (identifier) is provided.

3.1 COMP

Basically, the **COMP** identifier contains the part list and mounting data of each single device present in the Mentor CAD file; data are separated by spaces.

Every single row of the Mentor file starting with the **COMP** label contains the following information:

- Drawing reference
- Part number
- Value/Device name
- Package type
- Not used
- Mounting side
- Rotation

The following example shows the syntax used for the **COMP** identifier:

	Drawing ref.	Part number	Value/Device name	Package type	Not used		Mounting side	Rotation
COMP	C1	3CE101	100n	c050802e	4.3	2.65	1	0
COMP	C2	3CE221	220n	c050802e	0.55	0.3	0	270
COMP	C3	3CE100	10n	c050802e	1.55	0.1	1	180
...	...	...	...	...	...	...	...	...

```
……….
##############################################
##Component Information
##############################################
COMP C1 3CE101 100n c050802e  4.3      2.65     1   0
C_PROP (DES,"X7R") (TOLL,"20-20") (SPEA,"10") (VALUE,"100n")
C_PIN C1-1 4.3      2.65     0  1  0 pad_10_22_sx /N$130
C_PIN C1-2 4.5      2.65     0  1  0 pad_10_22_dx GROUND
COMP C2 3CE221 220n c050802e  0.55     0.3      0  270
……….
```

3.2 C_PROP

Basically, the **C_PROP** identifier contains for every single device its own properties; data are identified by labels and separated by spaces in a row of the Mentor file.

The “Import from Mentor” import CAD driver manages the following fields and labels:

- **SPEA** Identifies the code of the “component family” as defined by SPEA. This identifier can be optionally present in the output ASCII text file.
- **TOLL** Identifies the positive and negative device tolerances.
- **VALUE** Identifies the device value, if not yet specified with the **COMP** identifier.
- **MULTY_ASSY** Identifies the composition name in case of a variant board.

The following example shows the syntax used for the **C_PROP** identifier:

```
……
C_PROP (DES,"X7R") (TOLL,"20-20") (SPEA,"10") (VALUE,”100n")
……
C_PROP (VALUE,”100n") (TOLL,"20-20") (SPEA,"10")
……
```

Typically, the **C_PROP** identifier follows the **COMP** identifier, as shown in the following example:

```
……
##############################################
###Component Information
##############################################
COMP C1 3CE101 100n c050802e  4.3      2.65     1   0
C_PROP (DES,"X7R") (TOLL,"20-20") (SPEA,"10") (VALUE,”100n")
……
```

3.3 C_PIN

The **C_PIN** identifier is used to describe the device pin properties (pin name, pin access side and coordinates, …); data are separated by blanks in a row of the Mentor file.

The “Import from Mentor” import CAD driver manages the following data:

- Drawing reference-pin name
- Pin X-coordinate
- Pin Y-coordinate
- Pin access side
- Not used
- Pad identifier
- Net Name

The following example shows the syntax used for the **C_PIN** identifier:

	Drawing ref.–pin name	X-coord.	Y-coord.	Access side	Not used		Pad identifier	Net name
C_PIN	C1-1	4.33	2.65	0	1	0	Pad_10_22_sx1	/N$130
...	...	...	...	...	...	...	...	...

Typically, the **C_PIN** identifier follows the **C_PROP** identifier, as shown in the following example:

```
……….
##############################################
###Component Information
##############################################
COMP C1 3CE101 100n c050802e  4.3      2.65     1   0
C_PROP (DES,"X7R") (TOLL,"20-20") (SPEA,"10") (VALUE,"100n")
C_PIN C1-1 4.33      2.65     0  1  0 pad_10_22_sx /N$130
……….
```

3.4 B_UNITS

The **B_UNITS** identifier is used to specify the used unit of measurement for coordinates and dimensions.

Valid values are:

- **MM**, to specify that all the coordinates and dimensions are expressed in millimeters
- **INCHES**, to specify that all the coordinates and dimensions are expressed in inches
- **MILS**, to specify that all the coordinates and dimensions are expressed in mils (inches/1000)

The following example shows the syntax used for the **B_UNITS** identifier:

```
……….
B_UNITS Inches
……….
```

3.5 T_TEST VIA

The **T_TEST VIA** identifier is used to specify the properties for the via holes that can be used as test points; the decision to use a via hole as test point can be taken during the PCB development in Mentor.

Data are separated by blanks in a row of the CAD file and the “Import from Mentor” import CAD driver manages the following labels:

- Net name
- X-Coordinate
- Y-Coordinate
- Access side
- Not used
- Test point number

The following example shows the syntax used for the **T_TEST VIA** identifier:

	Net name	X coord.	Y coord	Access side	Not used			Test point number
T_TEST VIA	/V12	8.87	2.4	BOT	V0_04_tp	Xxctr	[]	[TP173(IN,0,0,0,TL,5,1,std,1)]
...	...	...	...	...	...	...	..	...

```
……..
##############################################
###Board Added Part Information
##############################################
##############################################
###TESTPOINTS
##############################################
T_TEST VIA /LCT 3.520 -2.41 BOT v026rd_040_tp INSERTED []
[TP16(IN,0.0,0.0,0,TL,0.1,0.1,0.01,std,1)]
T_TEST VIA /N$58 5.456 2.075 BOT v02rd_04_tp INSERTED []
[TP168(IN,0.0,0.0,0,TL,0.1,0.1,0.01,std,1)]
T_TEST VIA /VID 7.612 -1.9 BOT v02rd_04_tp INSERTED []
[TP149(IN,0.0,0.0,0,TL,0.15,0.15,0.01,std,1)]
T_TEST VIA /N$60 6.429 2.6 BOT v02rd_04_tp INSERTED []
[TP1(IN,0.0,0.0,0,TL,0.15,0.15,0.01,std,1)]
……..
```

3.6 T_TEST PIN

The **T_TEST PIN** identifier is used to specify the properties for the test point placed on a device pin; this decision can be get during the PCB development in Mentor.

Data are separated by spaces in a row of the CAD file and the “Import from Mentor” import CAD driver manages the following labels:

- Net name
- X-Coordinate
- Y-Coordinate
- Access side
- Not used
- Test point number

The following example shows the syntax used for the **T_TEST PIN** identifier:

	Net name	X coord.	Y coord	Access side	Not used			Test point number
T_TEST PIN	ADR3	5.5	0.0	BOT	T050rd	IC29-8	[]	[TP68(IN,0,0,0,BL,5,1,std,1)]
...	...	...	...	...	...	...	..	...

```
……
##############################################
###Board Added Part Information
##############################################
##############################################
###TESTPOINTS
##############################################
T_TEST VIA /LCT 3.520 -2.41 BOT v026rd_040_tp INSERTED []
[TP16(IN,0.0,0.0,0,TL,0.1,0.1,0.01,std,1)]
……
T_TEST PIN /COMMAND(8) 6.1 -0.1 BOT t050rd IC29-20 []
[TP71(IN,0.0,0.0,0,BL,0.15,0.15,0.01,std,1)]
……
```

3.7 B_ADDP

The **B_ADDP** identifier is used to specify the board added part information.
This identifier is used by SPEA to recognize the board fiducial.

Data are separated by spaces in a row of the CAD file and the “Import from Mentor” import CAD driver manages the following labels:

- Identifier
- Part Number
- X-Coordinate
- Y-Coordinate
- Rotate
- Not used
- Mounting side/Access side

The following example shows the syntax used for the **B_ADDP** identifier:

	Identifier	Part number	X-coord.	Y-coord.	Rotate	Not used		Mounting side/Access side
B_ADDP	Fiducial	fiducial	12.45	-2.5	0	1	1	1
B_ADDP	fiducial	Fiducial	12.45	-2.5	0	1	1	1
...	...	...	...	...	...	...	...	...

Notes:

- The **Identifier** label corresponds to the **Fiducial Label** item defined in the **Import settings**.
- The value defined in the **Mounting side/Access side** label is "**1**" if it is **Top** side, it is "**2**" if it is **Bottom** side.

```
.....
##############################################
###Board Added Part Information
##############################################
.....
B_ADDP  fiducial 'fiducial' 12.45 -2.5    0   1   1   1
B_ADDP  fiducial 'fiducial' 12.45 -2.5    0   1   1   1
.....
```

4. Mentor "TRC" file format

This is a partial extract of an example of a Mentor output ASCII text file:

```
UNITS TN
ST 26287600 4032284 6 6450
XRF   1 SIGNAL_1
XRF   2 SIGNAL_2
XRF   3 SIGNAL_3
XRF   4 SIGNAL_4
XRF   5 SIGNAL_5
XRF   6 SIGNAL_6

# NET '/AT'
ANT  2 18046700 1562100 18046700 1562100
SEG 18046700 1562100 3 via_nullvier
SEG 18046700 1562100 1 0
WIR  2 18046700 1562100 18046700 1562100
SEG 18046700 1562100 4 via_nullvier
SEG 18046700 1562100 3 0
ANT  2 17716500 2247900 17716500 2247900
SEG 17716500 2247900 4 via_nullvier
SEG 17716500 2247900 1 0
WIR  4 17716500 2247900 18046700 1562100
SEG 17716500 2247900 4 25400
SEG 17881600 2082800 4 25400
SEG 17881600 1727200 4 25400
SEG 18046700 1562100 4 0
```

The Import from Mentor CAD driver can correctly identify and use the following labels (identifiers):

- **XRF**
- **NET**
- **ANT**
- **SEG**
- **WIR**
- **INC**

In the next paragraphs a short description for each label (identifier) is provided.

4.1 XRF

The **XRF** identifier defines the layers.

Data are separated by blanks in a row of the CAD file and the “Import from Mentor” import CAD driver manages the following labels:

- Layer number
- Layer name

The following example shows the syntax used for the **XRF** identifier:

	Layer number	Layer name
XRF	1	SIGNAL_1
XRF	2	SIGNAL_2
...	...	...

```
NITS TN
ST 26287600 4032284 6 6450
XRF   1 SIGNAL_1
XRF   2 SIGNAL_2
XRF   3 SIGNAL_3
XRF   4 SIGNAL_4
XRF   5 SIGNAL_5
XRF   6 SIGNAL_6
……..
```

4.2 NET

The **NET** identifier identifies the name of the net.

Data are separated by spaces in a row of the CAD file and the “Import from Mentor” import CAD driver manages the **Net name** labels.

The following example shows the syntax used for the **NET** identifier:

	Net name
NET	'/AT'
...	...

```
……..
# NET '/AT'
……..
```

4.3 WIR

The **WIR** identifier identifies a branch of the net.

Data are separated by spaces in a row of the CAD file and the “Import from Mentor” import CAD driver manages the following labels:

- Segment number
- Segment Start X–coodinate
- Segment Start Y–coodinate
- Segment End X–coodinate
- Segment End Y–coodinate

The following example shows the syntax used for the **WIR** identifier:

	Segment number	Start X-coord.	Start Y-coord.	End X-coord.	End Y-coord.
WIR	2	18046700	1562100	18046700	1562100
WIR	4	17716500	2247900	18046700	1562100
...	...	...	...	...	...

```
.....
ANT  2 18046700 1562100 18046700 1562100
SEG 18046700 1562100 3 via_nullvier
SEG 18046700 1562100 1 0
WIR  2 18046700 1562100 18046700 1562100
SEG 18046700 1562100 4 via_nullvier
SEG 18046700 1562100 3 0
ANT  2 17716500 2247900 17716500 2247900
SEG 17716500 2247900 4 via_nullvier
SEG 17716500 2247900 1 0
WIR  4 17716500 2247900 18046700 1562100
SEG 17716500 2247900 4 25400
.....
```

4.4 SEG

The **SEG** identifier identifies all the coordinates of the net branch.

Data are separated by spaces in a row of the CAD file and the “Import from Mentor” import CAD driver manages the following labels:

- X-Coordinate
- Y-Coordinate
- Layer number
- Track width

The following example shows the syntax used for the **SEG** identifier:

	X-coord.	Y-coord.	Layer number	Track width
SEG	18046700	1562100	3	via_nullvier
SEG	18046700	1562100	1	0
...	...	...	...	...

```
.....
ANT  2 18046700 1562100 18046700 1562100
SEG 18046700 1562100 3 via_nullvier
SEG 18046700 1562100 1 0
WIR  2 18046700 1562100 18046700 1562100
.....
```

5. Import settings

The options to be checked and/or modified are listed below.

Cad Type	Category		Description
MENTOR	Component properties identifiers	Value Label	Label identifying the components value.
		Tolerance Label	Label identifying the components tolerance.
		Device type identifier Label	Label identifying the components device type.
		Part number identifier Label	Label identifying the components Part Number.
		Fiducial Label	Label identifying the board Fiducials.
	Options	Extract values from the Part Number	If enabled, it extracts the Part Number component value.
		Load Test point section of MENTOR file	Enables the import of the test points section into the file.
		Load All vias	Enables the import of the vias section into the file.

5.1 Component properties identifiers

Typically, the component properties identifiers are present in a specific section of the Mentor CAD file.

The CAD-CAE Mentor allows the designer to customize some fields in the ASCII text output file using identifiers.

The component properties identifiers could be defined in the Mentor file using custom identifiers that allow using them instead of the standard.

During the CAD import execution, it is possible to specify the label used for this customization.

In the next paragraphs some settings examples and how they can influence the imported data are listed.

5.1.1 All fields are filled

The result of the import contains information about **Value**, **Tolerance**, **Device type**, **Part Number** and **Fiducial** with the specified custom identifier.

5.1.2 All fields are empty

The import result does not contain information about **Value** and **Tolerance**.

The **Part Number** is read in the Mentor ASCII file on the standard position, this means that it is read as the second field in the rows starting with **COMP** identifier, as reported in the following example.

```
……
COMP C10 V39392-F2106-M elko1 ATACHIPB__1  67.6275 53.6575 1  90
C_PROP (INSTPAR,"10u") (MULTI_ASSY,"all,a1") (KIND,"tantal") (FORM,"smd") (MAX_VOLTAGE,"6.3")
C_PROP (DESC,"KOND 10 UF SMD") (MVERS,"0") (REFLOC,"MM,-0.9525,-
3.4925,0,BL,1.6,0.8,0.3,std,1,ASSEMBLY")
……
```

This is the imported part number

5.1.3 Filled "Value" and "Tolerance" labels and empty "Part Number"

The import result contains information about **Value** and **Tolerance** with the specified custom identifier and **Part Number** read in the Mentor ASCII file on the standard position.

This means that it is read as the second field in the rows starting with the **COMP** identifier.

If the file structure is similar to the following:

```
……
COMP R153 V39243-W5221-F100 res1 A0805__1  154.6225 120.3325 2   0
C_PROP (VALUE,"100K") (TOLERANCE,"5") (PINS_OUT,"1")
C_PROP (SPEC_HEAT,"800") (MASS_DENSITY,"5500") (INSTPAR,"221") (MULTI_ASSY,"all,a1")
(KIND,"metal"
……
```

the **Value Label** has to be set with the **VALUE** identifier and the **Tolerance Label** has to be set with the **TOLERANCE** identifier.

5.1.4 Device type identifier label

The CAD-CAE Mentor allows the designer to add custom attributes for specific uses.

One application could be added to the SPEA code to identify the **Device type** using the **SPEA** label as identifier, such as reported in the following example:

```
COMP C10 V39392-F2106-M elko1 ATACHIPB__1  67.6275 53.6575 1  90
C_PROP (INSTPAR,"10u") (MULTI_ASSY,"all,a1") (KIND,"tantal") (FORM,"smd") (MAX_VOLTAGE,"6.3")
(SPEA "10")
C_PROP (DESC,"KOND 10 UF SMD") (MVERS,"0") (REFLOC,"MM,-0.9525,-
3.4925,0,BL,1.6,0.8,0.3,std,1,ASSEMBLY")
……
COMP R100 V39243-W5332-F200 res1 A0805__1  135.5725 126.6825 2 180
C_PROP (SPEC_HEAT,"800") (MASS_DENSITY,"5500") (INSTPAR,"3.32k") (MULTI_ASSY,"all,a1")
(KIND,"metal")
C_PROP (FORM,"smd0805") (MAX_CURRENT,"0") (NUMBER_ELEMENTS,"1") (TOLERANCE,"1") (DESC,"WID 3.32
KOHM SMD") (SPEA "1")
C_PROP (MVERS,"0") (REFLOC,"MM,-4.445,-0.635,0,BL,1.2,0.6,0.2,std,1,ASSEMBLY")
```

This is the device type identifier used by SPEA

5.2 Options

In order to import correctly data present in the Mentor CAD file, the items named **Extract values from the Part Number**, **Load Test Point section of MENTOR file** and **Load All vias** have to be set according to the contained information.

During the CAD import it is possible to enable these check boxes in different ways in order to obtain different results after the import.

5.2.1 "Extract values from the Part Number" check box enabled

Sometimes the board designer assigns to the device a “Dummy” Part Number containing data concerning Value and Tolerance. For example he uses the “R10K” part number to identify a resistor with 10KΩ value.

In this specific case the **Value Label** item has to be empty and the **Extract values from the Part Number** check box has to be enabled.

The “Dummy” Part Number present in the CAD files is stored in the Part Number Library.

5.2.2 Both "Load Test Point section of MENTOR file" and "Load All vias" disabled

During the import only vias identified with the **N_TEST VIA** identifier are imported, any other via present in the CAD file is ignored.

Typically, these are the only vias contactable present in the CAD file.

5.2.3 "Load Test Point section of MENTOR file" enabled and "Load All vias" disabled

Some CAD Mentor file could have a **TEST POINT** section. This means that during the PCB design the designer can place in some contact points a test point to be used to test the board.

At the end of the import these points will be identified with the **TPxx** drawing reference prefix.

5.2.4 Both "Load Test Point section of MENTOR file" and "Load All vias" enabled

If both the check boxes are enabled, the import works as only the **Load Test Point section of Mentor file** is enabled to and **Load all vias** disabled.

5.2.5 "Load Test Point section of Mentor file" disabled and "Load All vias" enabled

The result of an import with this settings is that all vias present in the Mentor CAD file are imported; including the via used to connect the “internal” vias.

When the **Load all vias** check box is enabled, the number of the layers present in the PCB has to be defined in the file named **Max Layer**.

Typically, the information about the number of layers of the PCB is a known data or it can be read in the Mentor CAD file.

5.3 Pin function assignment

In order to execute correctly the CAD file import, this assignment table must be filled,.

In order to correctly test some polarized devices such as diodes, bipolar transistors, etc., it is basic to correctly identify the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table are described below:

Field	Description
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Pin Function	Function concerning the Pin.
Pin Name	Pin reference.
Cad Pin	Pin reference in Cad file.

5.4 Drawing ref. initials/device type assignment

The Mentor file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the point of view of the test program generation.

The fields contained in the table are described below:

Field	Description
Drawing Reference	Initial letter identifying the **Device Type**.
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Default Tol+, Tol-	Value and tolerance of the device only if required (as for resistors).

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.

A. Note about the Mentor ASCII text file format

The Mentor CAD-CAE typically runs under Unix operating system and generates its neutral ASCII output file in Unix format.

The Unix ASCII text files use as end of line identifier, the "$0a_{hex}$" ASCII character.
The Windows® (MS-DOS) operating system uses as end of line identifier for ASCII text files, the "$0d_{hex}$" and "$0a_{hex}$" ASCII characters.
This means that output ASCII text files may require an ASCII format conversion (from Unix to Windows® format).

This operation can be performed using "WordPad", a standard text file editor.
Open the Mentor ASCII file with this editor and save it, this operation will automatically perform the conversion from ASCII Unix format to ASCII Windows® format.