CadPack

Import from ACCEL-PCAD

Software tool for import from ACCEL-PCAD Cad format

Technical Info

Version : 2
Code : 81190638.170

SPEA SpA
16, Via Torino
10088 Volpiano - Italy
Tel.: + 39 011 9825 400
Fax: + 39 011 9825 405
E-mail: info@spea.com
Web: www.spea.com

Contents

Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The “Import from ACCEL-PCAD” CAD import driver allows to import the data present in the ACCEL-PCAD CAD file and convert them in the SPEA Board data format.

Conventions, symbols and abbreviations

In the document, the  symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

SPEA SpA
Ufficio Documentazione
16, Via Torino
10088 Volpiano – Italy
Tel.: +39 011 9825400
Fax: +39 011 9825405
Email: info@spea.com
Web: www.spea.com

1. ACCEL-PCAD file data

With the “ACCEL-PCAD files” words we refer to the output information generated by the ACCEL-PCAD programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “ACCEL-PCAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movement for Flying Probes).

Information can be grouped in 4 different categories and typically concern the printed circuit:

- **Part List**
  It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
- **Net list**
  It is also called wiring list, containing device interconnection data; basically it is presentation of the electrical diagram.
- **Coordinate and access list**
  It is the list containing the devices coordinates, concerning their barycentre and pins.
- **Wiring and Routing list**
  It is the list containing the path of the Net tracks in the PCB.

For the import of the information above mentioned SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List, all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: ♦ **Top** (Component side) ♦ **Bottom** (Soldering side) ♦ **Not mounted Top** ♦ **Not mounted Bottom**
Rotation [1]	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code [1]	Device package (case) code.

Table 1 – Part List

[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list. This list must contain the interconnection between devices, including pad and via.

Basically, it is the representation of the electrical diagrams.

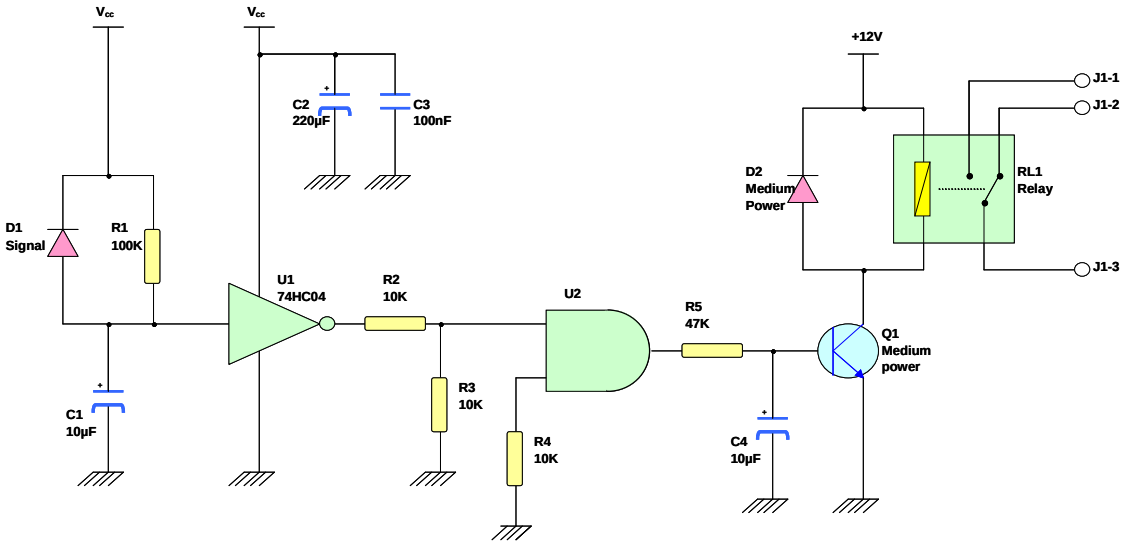

Figure 1 – Electrical diagram example

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: ♦ **Top** (Device side access) ♦ **Bottom** (Soldering side access). ♦ **Not accessible** ♦ **All** (both top and bottom side access)

Table 2 – Net List

1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

Table 3 – Coordinates and access list

1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Table 4 – Wiring and Routing list

Example:

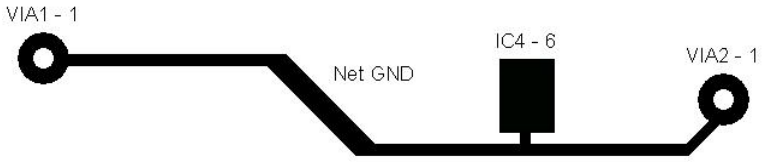

Figure 2 – Net track example

[1] **Optional data**

2. ACCEL-PCAD file generalities

ACCELL-PCAD file represents a complete electrical design and fully documented machine-readable format. With this file, the design files are easy to read.

2.1 ACCELL-PCAD file name

The ACCELL-PCAD file name has to have the **.PCB** extension.
It is an ASCII text file and provides an interface for third-party applications. It contains the information concerning PCB designs, schematic designs and libraries.

In order to import correctly the ACCELL-PCAD file in SPEA software, it has to contain the following sections:

- **ACCELL_ASCII**
- **asciiHeader**
- **compDef**
- **netlist**

A short description for each section is provided in the next chapter of the document.

3. ACCEL-PCAD file format

3.1 ACCELL_ASCII section

ACCELL_ASCII is the top-level keyword for PCAD ASCII files.

ACCELL_ASCII ::= 'ACCELL_ASCII'
asciiNameDef
asciiHeader
[library]
[netlist]
[pcbDesign | schematicDesign]

Following this keyword is the name of the file and a header of generic information. The file then optionally contains: a *library* of style, pattern, symbol, and component definitions; a *netlist* of component instances and nets; and a *pcbDesign* or a *schematicDesign* with design-specific and placement information.

3.2 “asciiHeader” section

This section provides ASCII format version and design file information.

asciiHeader ::= '(' 'asciiHeader'
asciiVersion
[written]
{ headerString }
FileUnits
')'

This is a partial extract of an example of a ACCEL-PCAD file:

```
ACCEL_ASCII "demo.pcb"

(asciiHeader
  (asciiVersion 3 0)
  (timeStamp 2004 11 8 10 41 9)
  (program "P-CAD 2002 PCB" "17.01.22")
  (copyright "Copyright © 1991-2003 Altium Limited")
  (fileAuthor "not used")
  (headerString "")
  (fileUnits Mil)
  (guidString "{59C2D2ED-F0E3-4070-A9C3-11B93B470DB8}")
)
...
```

3.3 “compDef” section

A compDef is a component template. The information in this template is used to create components of the same type in a Schematic or PCB design by providing the logical design information.

compDef ::= '(' 'compDef'
componentNameDef
originalName
compHeader
{ compPin }
{ attachedSymbol }
{ attachedPattern }
{ attr }
')'

This is a partial extract of an example of a ACCEL-PCAD file:

```
...
  )
  (compDef "R0805V_1"
    (originalName "R0805V")
    (compHeader
      (sourceLibrary "77792978.LIB")
      (numPins 2)
      (numParts 1)
      (alts (ieeeAlt False) (deMorganAlt False))
      (refDesPrefix "R")
    )
    (compPin "1" (pinName "1") (partNum 1) (symPinNum 1) (gateEq 1) (pinEq 0) (pinType Passive)
)
    (compPin "2" (pinName "2") (partNum 1) (symPinNum 2) (gateEq 1) (pinEq 0) (pinType Passive)
)
    (attachedSymbol (partNum 1) (altType Normal) (symbolName "RESV") )
    (attachedPattern (patternNum 1) (patternName "0805MIL")
      (numPads 2)
      (padPinMap
        (padNum  1) (compPinRef "1")
        (padNum  2) (compPinRef "2")
      )
    )
  )
  (compDef "T491-AV_1"
    (originalName "T491-AV")
...
```

3.4 “netlist” section

This section lists the component, net, net class, and net class to net class information for a design.

```
netlist ::= '(' 'netlist'
        netlistNameDef
        [globalAttrs]
        { compInst }
        { net }
        { netClass }
        { classToClass
        {variant}
        ')'
```

This is a partial extract of an example of a ACCEL-PCAD file:

```
...
(netlist "Netlist_1"
  (globalAttrs
    (attr "SilkscreenClearance" "10.0mil" (isVisible True) (textStyleRef "(Default)")
(constraintUnits mil) )
    (attr "HoleToHoleClearance" "13.0mil" (isVisible True) (textStyleRef "(Default)")
(constraintUnits mil) )
    (attr "BoardEdgeClearance" "15.0mil" (textStyleRef "(Default)") (constraintUnits mil) )
  )
  (compInst "C47"
    (compRef "CAPP_CASED_1")
    (originalName "CAPP_CASED")
    (compValue "470uF")
  )
  (compInst "C46"
    (compRef "C0805V_1")
    (originalName "C0805V")
    (compValue "1000pF")
  )
  (compInst "C45"
    (compRef "T491-AV_1")
    (originalName "T491-AV")
    (compValue "3.3uF")
    (attr "value2" "16V" (rotation 270.0) (isFlipped True) (textStyleRef "(Default)") )
  )
  (compInst "C44"
    (compRef "C0805V_1")
    (originalName "C0805V")
    (compValue "0.1uF")
  )
...
```