CadPack

Import from Orcad Layout

Software tool for import part/net list from Orcad Layout

Technical Info

Version : 2
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Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The Import from Orcad Layout CAD import driver allow to import the data present in the Orcad Layout CAD file and convert them in the SPEA Board data format.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

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1. Orcad Layout file data

With the “Orcad Layout CAD files” words we refer to the output information generated by the Orcad Layout CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Orcad Layout CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movement for Flying Probes).

Information can be grouped in 4 different categories and typically are related to the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is presentation of the electrical diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information mentioned above, SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: - **Top** (Component side) - **Bottom** (Soldering side) - **Not mounted Top** - **Not mounted Bottom**
Rotation	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code	Device package (case) code.

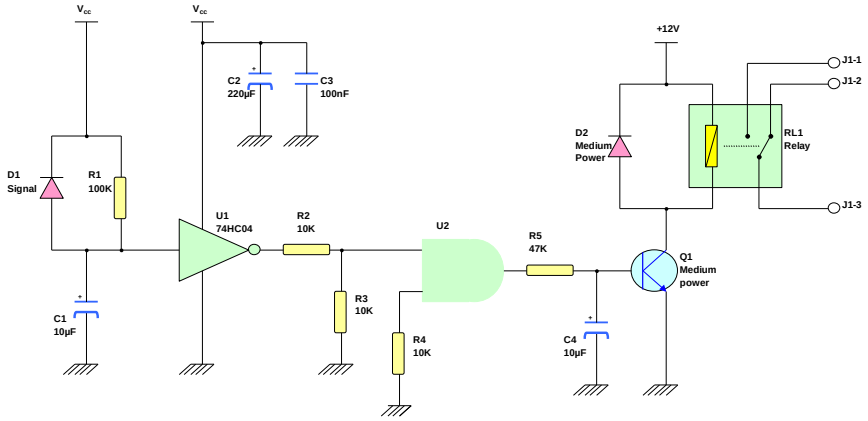
[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: - **Top** (Device side access). - **Bottom** (Soldering side access). - **Not accessible** - **All** (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

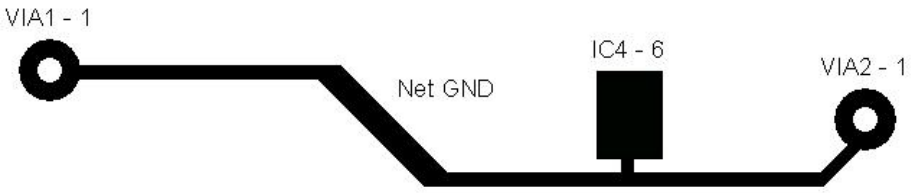
1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



[1] **Optional data**

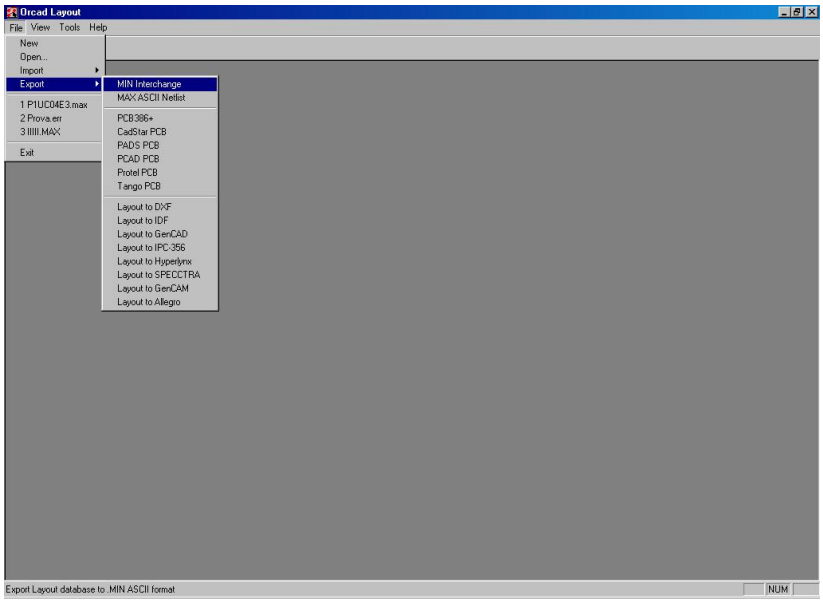
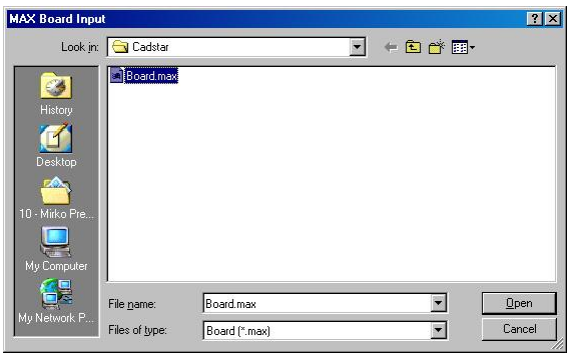
2. Orcad Layout file generalities

2.1 Orcad Layout file name

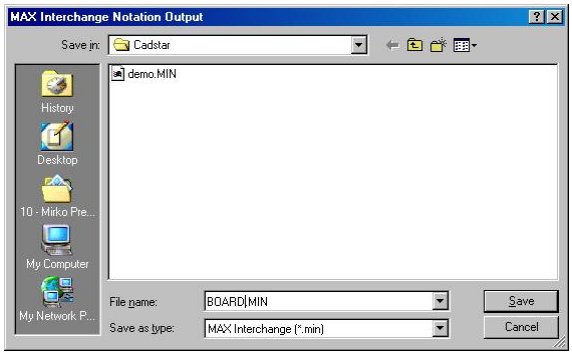
The Orcad Layout file name has to have the ***.MIN** extension.

It is an ASCII text file and it contains the information concerning the board, components and their connections.

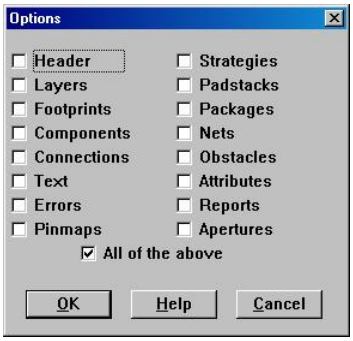
2.2 Extracting Orcad Layout file

1	Select **File > Export > MIN Interchange**. 
2	Select the **Board.max** file and click **Open** button. 

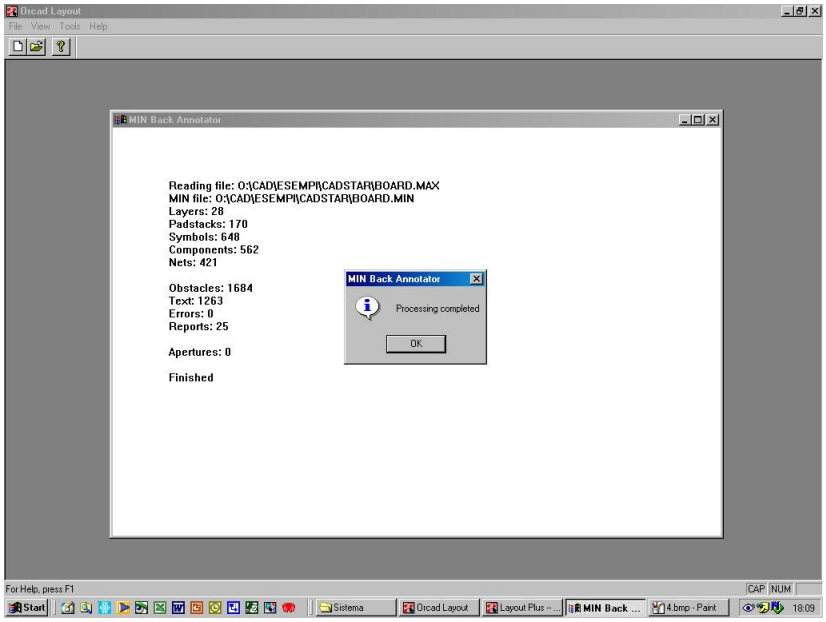
3 Click **Save** button to save the *.MIN file.



4 Select the **All of the above** check box and click **Ok** button.



The following window is displayed:



3. Orcad Layout file format

This is a partial extract of an example of a Orcad Layout output ASCII text file:

```
(MIN
(Version 9100)
(MajorRev 9)(MinorRev 1)
(L 28)(V 16)
(Begin
(Header
  (Grid 636)
  (ViaGrid 635)
  (UserDiv 10)
  (DisplayGrid 0)
  (PlaceGrid 635 635)
  (DetailGrid 635 635)
  (DotGrid 635 635)
  (DisplayPrecision 2540)
  (Origin -6393975 4598680)
  (InchFactor 0.00000393700787401575)
  (View -5671980 5363855 1300480 1300480)
  (OffGrid)(MultiVia Off)(Metric)(ConnectThruPours)
  (BackupSweep)(BackupInterval 10)(TimeUsed 354919859)
  (RotateAngle 5400)
  (AngleSnap 1)
(THRU 7(N "VIA7")(Uid -34)(TestPt Off)(NonPlated Off)
  (LgThermal Off)(DirectHit Off)
  (L 1(UNDEF))
  (L 2(UNDEF))
  (L 3(UNDEF))
  (L 4(UNDEF))
  (L 5(UNDEF))
  (L 6(UNDEF))
  (L 7(UNDEF))
  (L 8(UNDEF))
  (L 9(UNDEF))
  (L 10(UNDEF))
  (L 11(UNDEF))
  (L 12(UNDEF))
  (L 13(UNDEF))
  (L 14(UNDEF))
  (L 15(UNDEF))
  (L 16(UNDEF))
  (L 17(UNDEF))
  (L 18(UNDEF))
  (L 19(UNDEF))
  (L 20(UNDEF))
  (L 21(UNDEF))
  (L 22(UNDEF))
  (L 23(UNDEF))
  (L 24(UNDEF))
  (L 25(UNDEF))
  (L 26(UNDEF))
  (L 27(UNDEF))
  (L 28(UNDEF))
  )
(SYM 2(N "SO8")(Uid -914 449 656 0 0)(Derived 0)
  (P 1(N "1") 0 0 20(ExitRule "Std"))
  (P 2(N "2") 12700 0 20(ExitRule "Std"))
  (P 3(N "3") 25400 0 20(ExitRule "Std"))
  (P 4(N "4") 38100 0 20(ExitRule "Std"))
  (P 5(N "5") 38100 55880 20(ExitRule "Std"))
  (P 6(N "6") 25400 55880 20(ExitRule "Std"))
  (P 7(N "7") 12700 55880 20(ExitRule "Std"))
  (P 8(N "8") 0 55880 20(ExitRule "Std"))
  )
```

```
(SYM 3(N "RC1206")(Uid -119420 16510 0 0 0)(Derived 0)
  (P 1(N "1") 0 0 134(ExitRule "Std"))
  (P 2(N "2") 33020 0 134(ExitRule "Std"))
  )
(SYM 4(N "LED 5")(Uid -934 296 0 0 0)(Derived 0)
  (P 1(N "A") 0 0 22(ExitRule "Std"))
  (P 2(N "K") 25497 0 22(ExitRule "Std"))
  )
(SYM 5(N "MELF")(Uid -121105 -26035 0 0 0)(Derived 0)
  (P 1(N "C") 0 0 23(ExitRule "Std"))
  (P 2(N "A") -52070 0 23(ExitRule "Std"))
  )
(COMP 1(N "122")(N "0")(Uid -3502)(Fixed)(NonElectric) (-6245860 4613910)
  (Value "0")(Sym 160))
(COMP 2(N "123")(N "0")(Uid -3528)(Fixed)(NonElectric) (-5044440 4615180)
  (Value "0")(Sym 161))
(COMP 3(N "124")(N "0")(Uid -3529)(Fixed)(NonElectric) (-5044440 5483860)
  (Value "0")(Sym 162))
(COMP 4(N "125")(Uid -3530)(Fixed)(NonElectric) (-6245860 5814060)
  (Value "")(Sym 163))
(COMP 5(N "126")(N "0")(Uid -3531)(Fixed)(NonElectric) (-6295390 4963160)
  (Value "0")(Sym 164))
(COMP 6(N "127")(N "0")(Uid -3532)(Fixed)(NonElectric) (-5645150 5034280)
  (Value "0")(Sym 165))
(COMP 7(N "128")(Uid -104158)(NonElectric) (-5650230 5814060)
  (Value "")(Sym 436))
(COMP 8(N "129")(Uid -104159)(NonElectric) (-5044440 5814060)
  (Value "")(Sym 437))
(COMP 9(N "586")(Uid -115140) (-5187950 5829300)(Value "")
  (Sym 459))
(COMP 10(N "B1")(N "BORNE4")(Uid 11841) (-6246420 4512310)(R 10800)
  (Value "BORNE4")(Sym 478)(Package 59))
(COMP 11(N "B2")(N "BORNE4")(Uid 11814) (-5846420 4512310)(R 10800)
  (Value "BORNE4")(Sym 479)(Package 59))
(COMP 18(N "C4")(N "CHIM")(Uid 10463)(Mirrored) (-6003290 4786630)
  (R 16200)(Value "47UF")(Sym 327)(Package 26))
(COMP 19(N "C5")(N "CAP")(Uid 11285)(Mirrored) (-5481940 5286520)
  (R 5400)(Value "10NF")(Sym 129)(Package 2))
(COMP 20(N "C6")(N "CHIM")(Uid 9994) (-5656580 5111750)(R 5400)
  (Value "22UF/25V")(Sym 394)(Package 26))
(COMP 21(N "C7")(N "CHIM")(Uid 9972)(Mirrored) (-5734050 5275580)
  (R 5400)(Value "2")(Sym 390)(Package 26))
(COMP 22(N "C8")(N "C")(Uid 9759)(Mirrored) (-5544820 4936000)
  (R 5400)(Value "150PF")(Sym 385)(Package 5))
```

The Import from Orcad Layout CAD driver is able to correctly identify and use the following sections:

- **Part list**
- **Net list**
- **Pin Coordinates**
- **Vias**
- **Track Coordinates**

4. Import setting

4.1 Pin function assignment

In order to execute correctly the CAD file impor, this assignment table must be filled.

In order to correctly test some polarized devices such as diodes, bipolar transistors, etc., it is basic to correctly identify the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table are described below:

Field	Description
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Pin Function	Function concerning the Pin.
Pin Name	Pin reference.
Cad Pin	Pin reference in Cad file.

4.2 Drawing ref. initials/device type assignment

The Orcad Layout file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the point of view of the test program generation.

The fields contained in the table are described below:

Field	Description
Drawing Reference	Initial letter identifying the **Device Type**.
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Default Tol+, Tol-	Value and tolerance of the device only if required (as for resistors).

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.