CadPack

Import from Fatf

Software tool for import part/net list from Faft

Technical Info

Version : 2
Code : 81190406.121

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Contents

Introduction

CAD files are the base for the automatic generation of test program for InCircuit of any technology.

In order to generate the ICT test program in a short time and without errors, both Bed of Nails and Flying Probe testers require the circuit information available in CAD format.

The Import from Fatf CAD import driver allow to import the data present in the Fatf CAD file and convert them in the SPEA Board data format.

Conventions, symbols and abbreviations

In the document, the ⓘ symbol is used to highlight information or notes useful to the reader.

This manual can be updated in accordance with the evolution of the system and associated software.
It may contain preliminary contents or it may not be entirely updated with the latest versions used in the system.

Any remarks on errors and imperfections, or suggestions, can be addressed to:

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1. Fatf file data

With the “Fatf CAD files” words we refer to the output information generated by the Fatf CAD-CAE programs for the electrical diagrams design and PCB development, used to develop a test application (test program and adapter design).

Information stored in the “Fatf CAD files” concern an electronic board and can be used by an appropriate program to generate a test program and its test adapter design (Bed of Nails or list of movement for Flying Probes).

Information can be grouped in 4 different categories and typically are related to the printed circuit:

Part List
It is the list of all used devices, it must contain: devices drawing reference, part numbers, value, tolerances, device type, etc.
Net List
It is also called wiring list, containing device interconnection data; basically it is presentation of the electrical diagram.
Coordinate and access list
It is the list containing the devices coordinates, concerning their barycentre and pins.
Wiring and Routing list
It is the list containing the path of the Net tracks in the PCB.

For the import of the information above mentioned SPEA has developed the specific program for the translation, stored in a specified format, to its common data bank called “Board Data”.
The name of this type of program is “CAD import driver”.

For the required information, see the list in the following paragraphs.

1.1 Part List

The Part List is an ASCII text file, containing the list of all the parts used to assemble the board; sometimes it can be called **Bill of Material** (BOM).

In the Part List all information concerning the mounted and not mounted parts must be present.
For every part the following information must be defined:

Information	Description
Drawing Reference	Reference designator (e.g. U10, R105, D23, etc.).
Part Number	Device code (e.g. 132549.012, C4QW08, 001-58-AA, etc.).
Value	Device value (e.g. 10KΩ, 10µF, 1mH, etc.).
Tolerance	Positive and negative device tolerances (e.g. 1%, 5%, etc.).
Mounting side	The legal values for this item can be: - **Top** (Component side) - **Bottom** (Soldering side) - **Not mounted Top** - **Not mounted Bottom**
Rotation	Device mounting rotation angle (e.g. 0°, 180°, etc.).
Dimensions [1]	Device dimensions.
Case code	Device package (case) code.

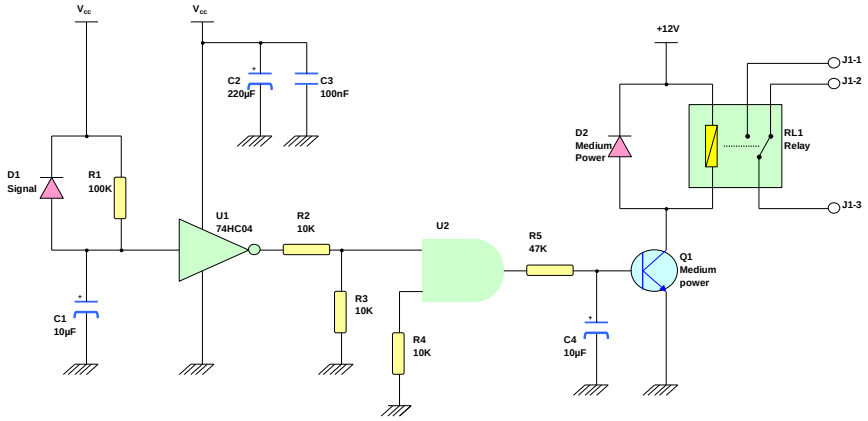
[1] **Optional data (not yet managed)**

1.2 Net List

The Net List is an ASCII text file containing the device interconnection data; it is also called wiring list.
This list must contain the interconnection between devices, including pad and via.
Basically, it is the representation of the electrical diagrams.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
Drawing reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin access side	Access side for the device pin, legal values are: - **Top** (Device side access). - **Bottom** (Soldering side access). - **Not accessible** - **All** (both top and bottom side access)



1.3 Coordinates and access list

The Coordinates and access list is an ASCII text file containing the devices coordinates concerning their barycentre and pins. Below, the required information:

Information	Description
Drawing Reference	Reference designator of the device connected to the net (e.g. U10, R105, D23, etc.).
Pin name	Name of the device pin connected to the net (e.g. 1, 15, Anode, K, Negative, etc.).
Pin X position	Pin X-coordinate.
Pin Y position	Pin Y-coordinate.
X barycentre [1]	Device X barycentre.
Y barycentre [1]	Device Y barycentre.

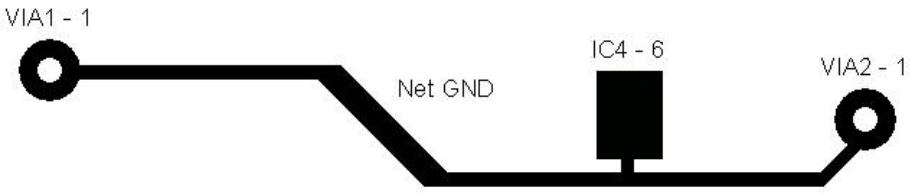
1.4 Wiring and Routing list

The Wiring and Routing list is an ASCII text file that contains all the coordinates of the Net tracks on the PCB and the link with the Net List. So the path of each net on the PCB is described in this file.

For every net the following information must be defined:

Information	Description
Net name	Net identifier (e.g. +5V, RESET, A01, etc.).
X Start	Track segment start X-coordinate.
Y Start	Track segment start Y-coordinate.
X End	Track segment end X-coordinate.
Y End	Track segment end Y-coordinate.
Width	Net segment thickness.
Layer	Layer the segment belongs to.

Example:



[1] **Optional data**

2. Fatf file generalities

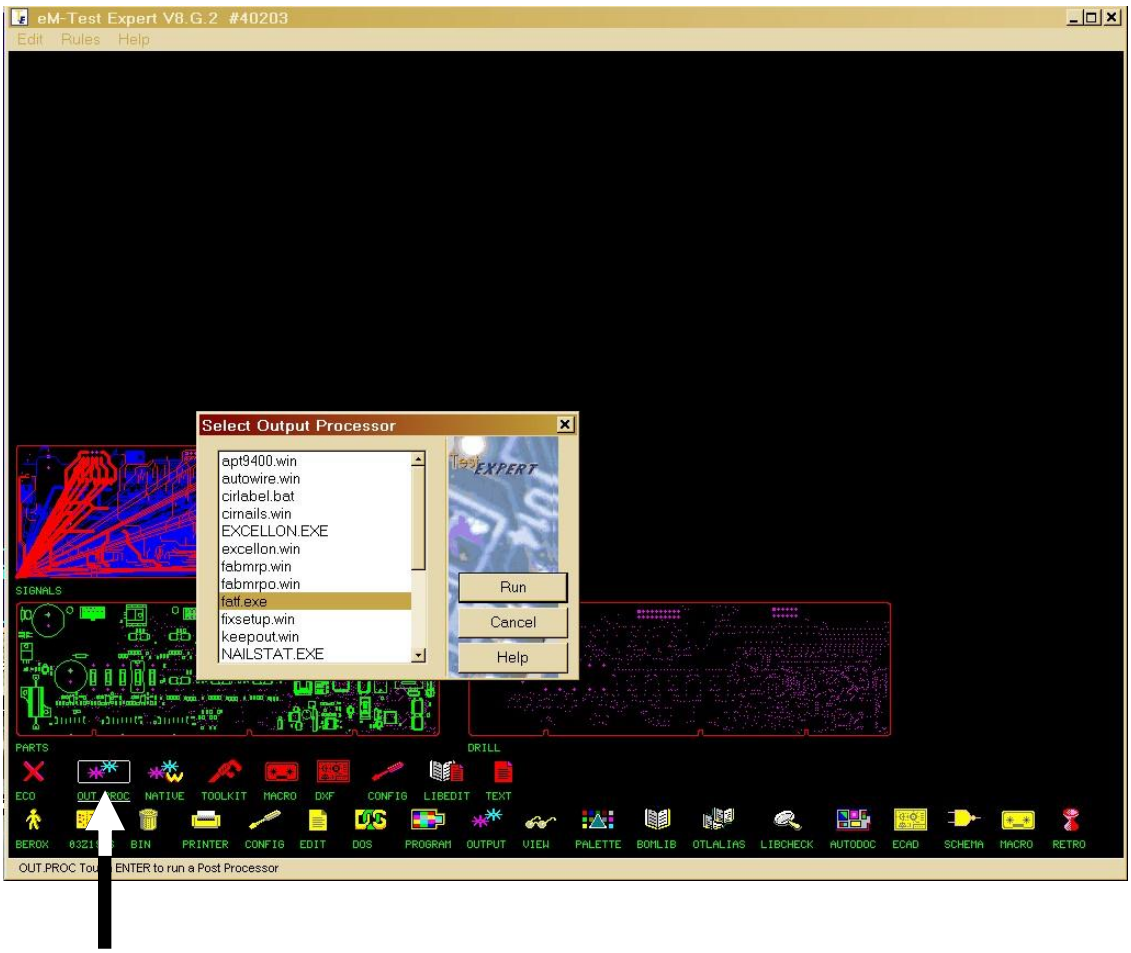
2.1 Fatf Layout file name

The Fatf file name has to have the ***.FAT** extension.

It is an ASCII text file and it contains the information concerning the board, components and their connections.

2.2 Extracting Fatf file

The ***.FAT** file can be generated by **Test Expert** (also known as **FabMaster**) by clicking the **OUT.PROC** icon and selecting the Fatf processor.



3. Fatf file format

This is a partial extract of an example of a Fatf output ASCII text file:

```
:FABMASTER FATF REV 11.0;
:UNITS = 1/1000 INCH;
:NOAUTOROTATE

:BOARD_DATA
1,"JOB"         ("E1_T1",1.0,14-05-2001,17-05-2001);
2,CONTOUR ((11513,3615,0),(11801,3615,0));
3,CONTOUR ((11801,3615,0),(11801,490,0));
4,CONTOUR ((11801,490,0),(11601,490,0));
5,CONTOUR ((11601,490,0),(11601,190,0));
6,CONTOUR ((11601,190,0),(4426,190,0));
7,CONTOUR ((4426,190,0),(4426,40,0));
8,CONTOUR ((4426,40,0),(3876,40,0));
:EOD

:PARTS
1,"C1","10UF_10V_1206/2","1206/1",4330,3770,900,T;
2,"C2","100N_0603_Y5V/1","0603/1",4420,3645,900,T;
3,"C3","100N_0603_Y5V/1","0603/1",1645,3575,1800,T;
4,"C4","100N_0603_Y5V/1","0603/1",1710,3575,1800,T;
5,"C5","100N_0603_Y5V/1","0603/1",4130,3550,1800,T;
6,"C6","10UF_10V_1206/2","1206/1",1515,3495,1800,T;
7,"C7","100N_0603_Y5V/1","0603/1",4425,3570,0,T;
:EOD

:LAYER_NAMES
1,"COMMON",COMMON,0,ELECTRICAL;
2,"TOP",TOP,3,ELECTRICAL;
3,"BOTTOM",BOTTOM,2,ELECTRICAL;
4,"INNER1",TRANSPARENT,2,ELECTRICAL;
5,"INNER2",TRANSPARENT,2,ELECTRICAL;
:EOD

:LAYER_SETS
1,"ALL_LAYERS",(1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20);
2,"TOP",(2);
3,"BOTTOM",(3);
:EOD

:PAD_SYMBOLS
1,TRACK (55,(-45,0)(45,0));
2,P_BLOCK (-15,-15,15,15);
3,P_BLOCK (-20,-20,20,20);
4,TRACK (40,(-37,0)(37,0));
5,TRACK (60,(-60,0)(60,0));
6,P_ROUND (30);
7,P_ROUND (26);
:EOD

:PAD_STACKS
1,PST1,27,P,((1,1));
2,PST2,15,P,((1,2));
3,PST3,20,P,((1,3));
4,PST4,20,P,((1,4));
5,PST5,30,P,((1,5));
6,PST6,15,P,((1,6));
7,PST7,8,P,((1,7));
8,PST8,24,P,((1,8));
9,PST9,40,P,((1,9));
10,PST10,7,P,((1,10));
11,PST11,20,P,((1,11));
12,PST12,40,P,((1,12));
```

```
13,PST13,45,P,((1,13));
14,PST14,45,P,((1,9));

:EOD
:PACKAGES
1,"14SMX",0,0,0,0
(PINS(1,"",0,0,T)(2,"",0,100,T)(3,"",250,100,T)(4,"",250,0,T))
(1, LAYER(2 (BLOCK (-45,-27,45,27)))
2, LAYER(2 (BLOCK (-45,73,45,127)))
3, LAYER(2 (BLOCK (205,73,295,127)))
4, LAYER(2 (BLOCK (205,-27,295,27)))
0, LAYER(22 (TRACK (0,(-25,-50),(275,-50),(275,150),(-25,150),(-25,-50)),
TRACK (0,(35,-10),(32,0),(25,7),(15,10),(5,7),(-2,0),(-5,-10),
(-2,-20),(5,-27),(15,-30),(25,-27),(32,-20),(35,-10)),
TRACK (0,(275,150),(-25,150)),
TRACK (0,(275,-50),(-25,-50)),
TRACK (0,(60,150),(60,-20),(90,-50)),
TRACK (0,(190,-50),(190,150)))));
2,"0402/1",0,0,0,0
(PINS(1,"",0,0,T)(2,"",0,-45,T))
(1, LAYER(2 (BLOCK (-15,-15,15,15)))
2, LAYER(2 (BLOCK (-15,-60,15,-30)))
0, LAYER(22 (TRACK (0,(-11,-2),(11,-2),(11,-43),(-11,-43),(-11,-2)))));
:EOD

:NETS
1,"+3.3VA",S,
((177,3),(177,1),(177,5),(178,1),(177,7),(103,1),(178,3),(178,5),(178,7),
(1228,8),(112,1),(113,1),(493,1),(481,2),(506,2),(114,1),(478,2),(1230,162),(1074,1),
(463,2),(458,2),(440,2),(452,2),(91,1),(445,2),(83,1),(1230,133),(125,1),(1230,1),
(1131,1),(1230,14),(130,1),(77,1),(92,1),(371,1),(367,2),(372,2),(382,2),(403,2),
(405,2),(419,2),(397,1),(1230,117),(93,1),(426,2),(427,2),(1230,100),(1222,27),(71,1),
(368,2),(60,1),(356,2),(348,2),(347,1),(322,2),(341,2),(59,1),(1222,3),(56,1),
(311,2),(334,1),(310,2),(282,1),(283,1),(320,2),(330,1),(55,1),(318,1),(1224,75),
(53,1),(165,1),(297,2),(290,1),(162,1),(169,1),(1224,93),(1224,71),(377,2),(402,2),
(1224,91),(1224,92),(1224,124),(1224,130),(1224,164),(1224,177),(1224,182),(78,1),(79,1),(80,1),
(173,1),(175,1),(404,2),(174,1),(1224,186),(172,1),(407,2),(411,2),(1224,66),(412,2),
(72,1),(342,2),(357,2),(383,2),(85,1),(1210,4),(38,2),(39,2),(40,2),(41,2),
(73,1),(1210,2),(656,1),(43,2),(42,2),(176,2),(191,1),(192,1),(193,1),(194,1),
(74,1),(75,1),(57,1),(349,2),(323,2),(303,1),(362,2),(369,2),(62,1),(373,2),
(378,2),(418,2),(424,2),(423,2),(417,2),(422,2),(416,2),(421,2),(415,2),(420,2),
(414,2),(428,2),(429,2),(430,2),(431,2),(432,2),(89,1),(441,2),(1230,53),(1230,56),
(1230,70),(97,1),(437,2),(1230,32),(1230,45),(131,1),(117,1),(126,1),(120,1),(1230,85),
(811,1),(484,2),(514,2),(500,2),(499,2),(495,2),(490,2),(496,2),(487,2),(491,2),
(482,2),(488,2),(483,2),(480,2),(476,2),(475,2),(470,2),(464,2),(471,2),(459,2),
(465,2),(453,2),(460,2),(454,2),(1224,80),(24,1),(25,1),(36,1),(559,1),(258,1),
(262,2),(12,1),(1209,20),(27,1),(261,2),(1224,176),(1224,165),(160,1),(161,1),(168,1),
(1224,133),(1224,191),(26,1),(1224,128),(179,2),(33,1),(1213,14),(47,1),(312,2),(1,1)
);
2,"+3.3VB",S,
((44,1),(1221,16),(557,1),(49,1),(20,1),(1221,132),(15,1),(21,1),(22,1),
(63,1),(23,1),(1221,122),(158,1),(1221,192),(54,1),(1221,201),(88,1),(1221,157),(1221,159),
(163,1),(166,1),(1221,2),(1221,78),(61,1),(68,1),(1221,96),(1221,118),(170,1),(171,1),
(962,1),(98,1),(388,2),(413,2),(84,1),(1227,17),(1227,41),(101,1),(1227,9),(159,1),
(1221,100),(167,1),(1221,59),(1221,61),(164,1),(389,2),(926,1),(111,1),(1229,4),(191,2),
(192,2),(193,2),(194,2),(105,2),(108,2),(106,2),(1227,29),(1229,2),(973,1),(73,2),
(74,2),(72,2),(75,2),(107,2),(109,2),(110,2),(122,1),(123,1),(1092,1),(104,1)
);
:EOD

:PADS
1,41,((1100,980),(1190,980),(2125,1108),(2290,770),(2355,895),(2440,950),(2265,280),
               (2590,810),(2440,1220),(2440,1330),(2440,1440),(2580,1565),(2575,1840),(2645,485),
               (2995,515),(2630,1985),(3005,1935),(3080,1840),(3090,1610),(2650,2160),(2650,2270),
               (2545,2275),(2650,2325),(2880,1935),(2205,2060),(3310,1565),(3300,1730),(3405,1720),
               (2045,2140),(2770,2425),(2645,2480),(2550,2540),(2645,2590),(2650,2700),(2465,2425),
               (2770,2645),(2365,2750),(2235,2915),(2180,2915),(2010,2710),(1875,2658),(1415,2730),
               (1250,2695));
1,42,((2980,2879));
```

```
1,41,((2770,2855),(2645,2800),(2645,2910));
1,42,((3130,2980),(3075,2680));
1,41,((2575,2915));
:EOD

:LAYERS
1,LAYER (2 (TRACK (10,(18,745),(-82,745))));
1,LAYER (2 (TRACK (10,(118,745),(18,745))));
1,LAYER (2 (TRACK (10,(218,745),(118,745))));
1,LAYER (2 (TRACK (10,(18,545),(-82,545))));
1,LAYER (2 (TRACK (10,(118,545),(18,545))));
1,LAYER (2 (TRACK (10,(218,545),(118,545))));
1,LAYER (2 (TRACK (10,(2175,930),(2200,930),(2235,895),(2245,895))));
1,LAYER (2 (TRACK (10,(2245,895),(2305,895))));
1,LAYER (2 (TRACK (10,(2290,770),(2245,770))));
1,LAYER (2 (TRACK (10,(2305,895),(2355,895))));
1,LAYER (2 (TRACK (10,(2440,950),(2480,950))));
1,LAYER (2 (TRACK (10,(2265,280),(2300,280))));
1,LAYER (2 (TRACK (10,(2480,950),(2480,1005))));
:EOD
```

The Import from Fatf CAD driver can correctly identify and use the following sections:

- **Part list**
- **Net list**
- **Pin Coordinates**
- **Vias**
- **Track Coordinates**

4. Import setting

The options to be checked and/or modified are listed below.

Cad Type	Category		Description
FATF	Options	Load Tracks for undefined nets	Enables the addition of the tracks for which it has not been determined a net inside the file.

4.1 Pin function assignment

In order to execute correctly the CAD file import, this assignment table must be filled.

In order to test correctly some polarized devices such as diodes, bipolar transistors, etc., it is basic to correctly identify the pin function (i.e. anode, base, etc.) of each pin.

The fields contained in the table, are described below:

Field	Description
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Pin Function	Function concerning the Pin.
Pin Name	Pin reference.
Cad Pin	Pin reference in Cad file.

4.2 Drawing ref. initials/device type assignment

The Fatf file typically contains all information about the devices, such as value, tolerances and type; which are fundamental from the point of view of the test program generation.

The fields contained in the table are described below:

Field	Description
Drawing Reference	Initial letter identifying the **Device Type**.
Device Type	Identifies the type of device (example: Resistors, Capacitors, Digital Devices, Diodes etc.).
Default Tol+, Tol-	Value and tolerance of the device only if required (as for resistors).

It could happen that in the CAD file they are missing. For each drawing reference initial, the displayed table enables to define the following data default values:

- Device type
- Default positive tolerance
- Default negative tolerance

This means that if, for any reason, the CAD file does not contain the information mentioned above, the default values will be used.