

Prof Simon McIntosh-Smith

Isambard PI

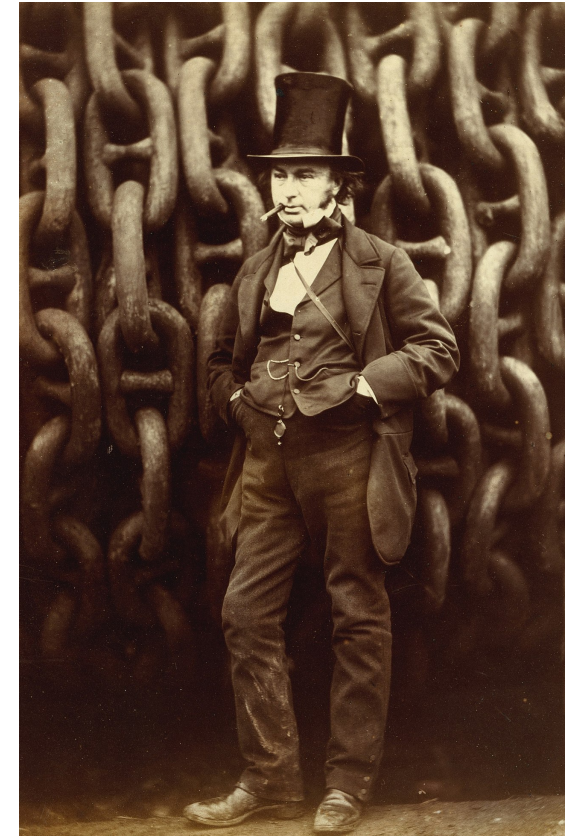
University of Bristol /

GW4 Alliance



Isambard: The world's first production 64-Bit Arm
supercomputer

'Isambard' is a new UK Tier 2 HPC service from GW4



Isambard Kingdom Brunel
1804-1859



The tiered model of HPC provision

Tier 0: international



Tier 1: national



Tier 2: regional

TIER 2 HPC CENTRES

Edinburgh Cambridge UCL
Loughborough Bristol Oxford

Tier 3



Isambard system specification

- **10,752** Armv8 cores (168 x 2 x 32)
 - **Cavium ThunderX2 32core 2.1GHz**
- Cray XC50 Scout form factor
- High-speed **Aries** interconnect
- Cray HPC optimised software stack
 - **CCE, CrayPAT, Cray MPI, math libraries, ...**
- **Technology comparison:**
 - **x86, Xeon Phi, Pascal GPUs**
- Phase 1 installed March 2017
- Phase 2 (the Arm part) arrives July 2018
- £4.7m total project cost over 3 years



Isambard's core mission: evaluating Arm for production HPC

Starting by optimizing the top 10 most heavily used codes on Archer

- **VASP**, **CASTEP**, **GROMACS**, **CP2K**, **UM**,
HYDRA, **NAMD**, **Oasis**, **SBLI**, **NEMO**
- Note: most of these codes are written in FORTRAN

Additional important codes for project partners:

- **OpenFOAM**, **OpenIFS**, WRF, CASINO, LAMMPS, ...

RED = codes optimised at the first Isambard hackathon

BLUE = codes optimised at the second hackathon



RAISING STEAM

1ST ISAMBARD HACKATHON - BRISTOL
NOVEMBER 2ND & 3RD 2017



STOKING THE FIRE

2ND ISAMBARD HACKATHON-BRISTOL
MARCH 19TH & 20TH 2018



Open  CFD®



UNIVERSITY OF
Southampton



ETH Zürich



UNIVERSITY
OF VIENNA

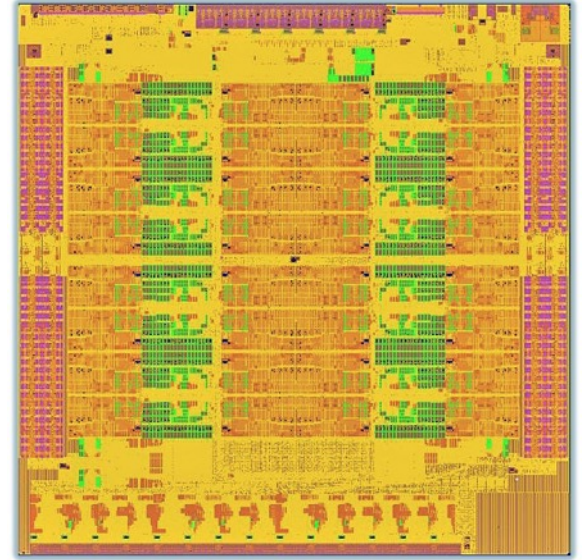


EPSRC

GW⁴

Cavium ThunderX2, a seriously beefy CPU

- 32 cores at up to 2.5GHz
- Each core is 4-way superscalar, Out-of-Order
- 32KB L1, 256KB L2 per core
- Shared 32MB L3
- Dual 128-bit wide NEON vectors
 - Compared to Skylake's 512-bit vectors, and Broadwell's 256-bit vectors
- 8 channels of 2666MHz DDR4
 - Compared to 6 channels on Skylake, 4 channels on Broadwell
 - AMD's EPYC also has 8 channels



Processor	Cores	Clock speed GHz	TDP Watts	FP64 TFLOP/s	Bandwidth GB/s
Broadwell	2 × 22	2.2	145	1.55	154
Skylake Gold	2 × 20	2.4	150	3.07	256
Skylake Platinum	2 × 28	2.1	165	3.76	256
Knights Landing	1 × 64	1.3	215	2.66	~490
ThunderX2	2 × 32	2.2	175	1.13	320

BDW 22c

Intel Broadwell E5-2699 v4, **\$4,115** each (near top-bin)

SKL 20c

Intel Skylake Gold 6148, **\$3,078** each

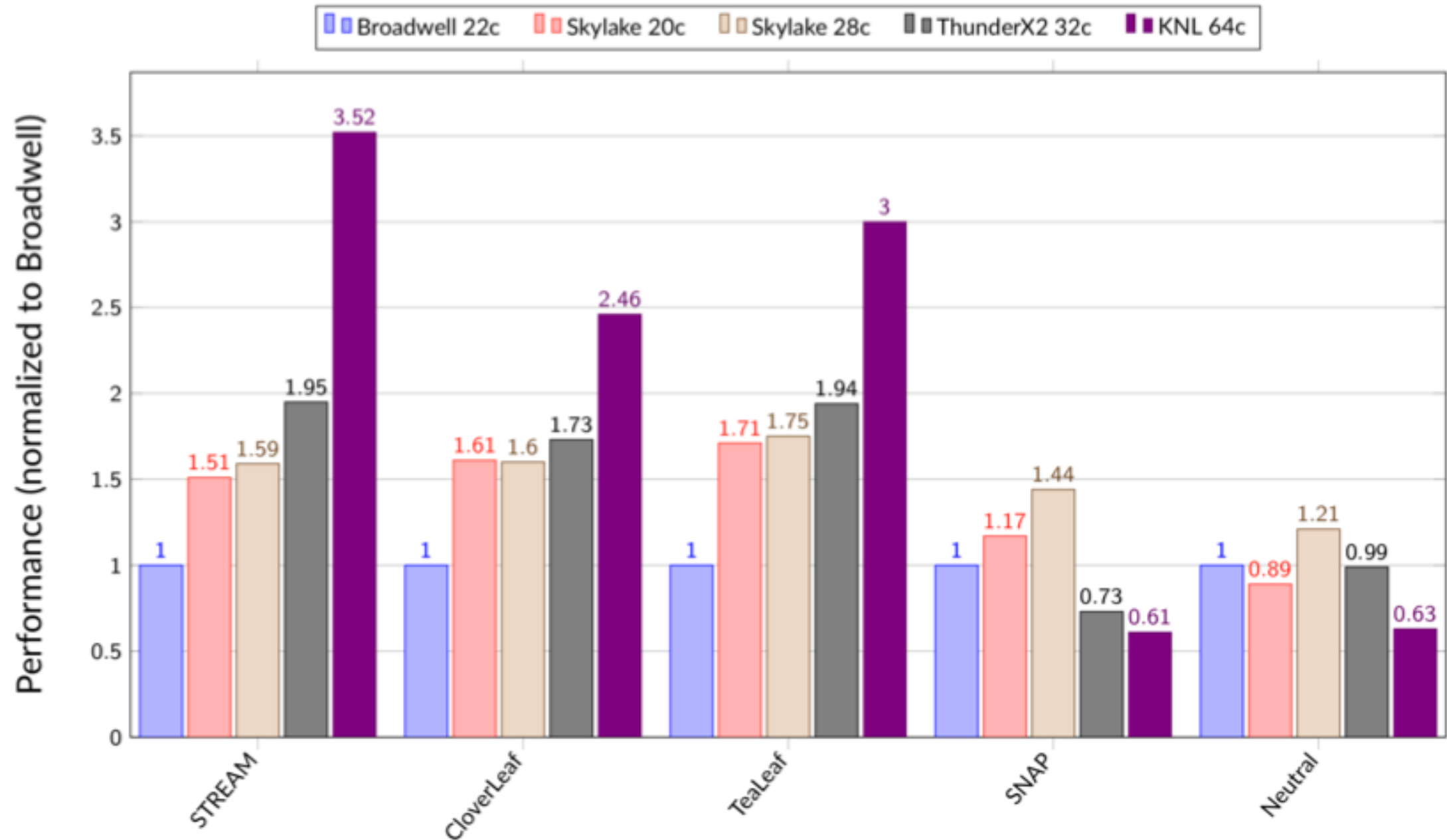
SKL 28c

Intel Skylake Platinum 8176, **\$8,719** each (near top-bin)

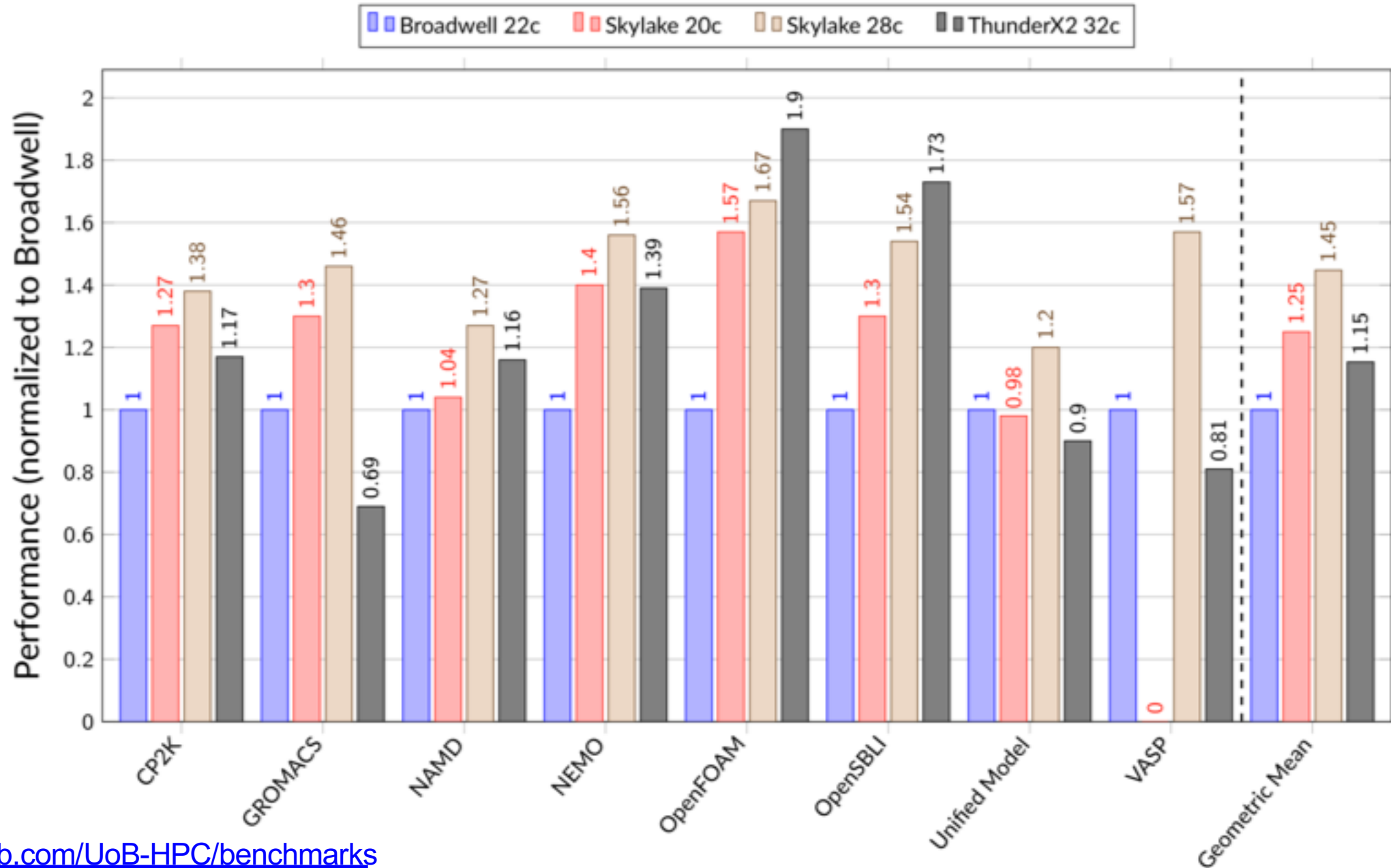
TX2 32c

Cavium ThunderX2, **\$1.795 each** (near top-bin)

Performance on mini-apps (node level comparisons)



Performance on heavily used applications from Archer



Benchmark	ThunderX2	Broadwell	Skylake	Xeon Phi
STREAM	GCC 8	Intel 18	Intel 18	Intel 18
CloverLeaf	CCE 8.7	Intel 18	Intel 18	Intel 18
TeaLeaf	GCC 7	Intel 18	Intel 18	Intel 18
SNAP	CCE 8.6	Intel 18	Intel 18	Intel 18
Neutral	GCC 8	Intel 18	Intel 18	Intel 18
CP2K	GCC 8	GCC 7	GCC 7	—
GROMACS	GCC 7	GCC 7	GCC 7	—
NAMD	Arm 18.2	GCC 7	Intel 18	—
NEMO	CCE 8.7	CCE 8.7	CCE 8.7	—
OpenFOAM	GCC 7	GCC 7	GCC 7	—
OpenSBLI	CCE 8.7	Intel 18	Intel 18	—
UM	CCE 8.6	CCE 8.5	CCE 8.6	—
VASP	CCE 8.7	Intel 17	Intel 17	—

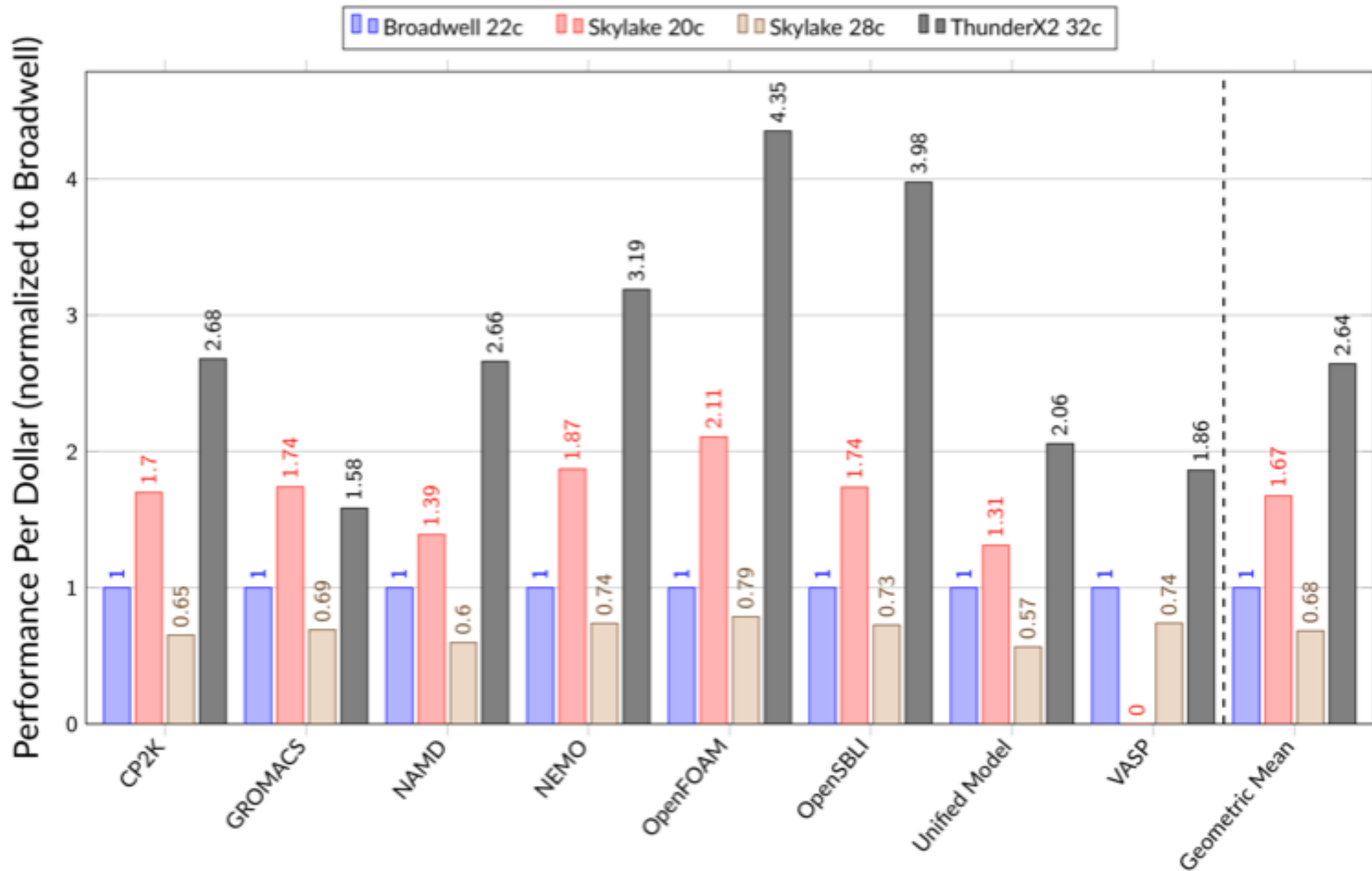
Comparison of compilers on Arm

STREAM	99%	100%	99%	98%
CloverLeaf	93%	94%	95%	100%
TeaLeaf	100%	95%	95%	99%
SNAP	82%	86%	100%	100%
Neutral	98%	100%	92%	83%
CP2K	98%	100%	BUILD	CRASH
GROMACS	99%	100%	89%	CRASH
NAMD	83%	CRASH	100%	BUILD
OpenFOAM	100%	BUILD	96%	BUILD
	GCC 7	GCC 8	Arm 18.3	CCE 8.7

Comparing Performance per Dollar

- Hard to do this rigorously
 - RRP is not what anyone pays
 - Whole system cost has to be taken into account
 - Purchase price vs. TCO
- However, we *can* form some useful intuition
 - The following charts were generated by taking the performance results, dividing by the official published list prices of the CPUs only, then renormalizing to Broadwell

Performance per Dollar: applications



What about Arm CPUs with Infiniband?

- Bristol also collaborating with HPE to host an Apollo70 “Catalyst” system:
 - 64 dual socket ThunderX2 nodes (4,096 cores)
 - Mellanox EDR Infiniband interconnect
- Will enable scaling comparisons across Cray Aries and IB
- Hoping to share results at SC18, Denver

Conclusions

- Early results show **ThunderX2 performance is competitive with current high-end server CPUs**, while **performance per dollar is compelling**
- **The software tools ecosystem is already in good shape**
- The full Isambard XC50 Arm system is due to be installed in July 2018, aiming to **open for science by the end of the summer**
- The signs are that **Arm-based systems are now real alternatives for HPC**, reintroducing much needed competition to the market
- Added benefits include **real opportunity for co-design**

For more information

Comparative Benchmarking of the First Generation of HPC-Optimised Arm Processors on Isambard

S. McIntosh-Smith, J. Price, T. Deakin and A. Poenaru, CUG 2018, Stockholm

<http://uob-hpc.github.io/2018/05/23/CUG18.html>

Bristol HPC group: <https://uob-hpc.github.io/>

Isambard: <http://gw4.ac.uk/isambard/>

Twitter: [@simonmcs](https://twitter.com/simonmcs)