ECE532S Digital Systems Design

Lab Test 1 Description - Individual Project

Last Updated: July, 2019

The purpose of this test is to show that you have mastered some of the basics of using Vivado. In advance of the test you should prepare the following two tasks. Although you may work on these tasks as a group, each person in the group should be prepared to demonstrate and answer questions about any part of any of these tasks. Individual grades will be assigned based on your familiarity with the tasks and on three questions that each of you will be asked. The questions will come from what you did and learned in the tutorials, from the tasks described below and basic Verilog (HDL) programming.

This is worth 10% of your final grade. If you do not have this exercise prepared in advance, you will be assigned a grade of 0%. Please ensure that you have signed up for a demo time slot. Contact your TA if you do not have one yet or do not remember your time.

1 Microblaze System

Build a MicroBlaze system that writes a 32-bit value to the base address of an AXI BRAM memory and then reads the value back for display in hexadecimal on the eight 7-segment displays of the Nexys4 DDR board. You will need to consult the Nexys4 DDR manual to learn how the displays work. When constructing the block design, constrain the pins manually without the board files as you did in the first MicroBlaze tutorial. You may use a GPIO to connect to the displays.

2 Simple Module and Simulation

Build a module using the HDL of your choice that inputs a stream of 4-bit numbers and outputs the largest of the numbers currently input. Assume all numbers are positive integers. The block has the following ports:

clk (input) the clock
reset_b (input) an active low reset signal
InputValid (input) value at data input is valid
DataInput[3:0] (input) data input
Largest[3:0] (output) the largest of the input values so far

The block operates as follows:

1. The **reset_b** signal is set to 0 for a few cycles to reset the state ma .
2. On a positive clock edge, if **InputValid** is true, then **DataInput[3:0]** has the next valid input.

3. The output **Largest[3:0]** is 0 after reset and then shows the largest of the numbers that have been input so far. This output changes one cycle after the corresponding number has been input.

4. The circuit continues to operate until a reset.

Your task is to:

1. Simulate this block using the Vivado simulator, or Modelsim. Note that Modelsim will require some extra configuration.

2. Demonstrate the use of a simple test bench using your HDL that exercises your module.

3. Develop enough tests to convince someone that your circuit is working.

4. Show the results of some tests with a waveform viewer.

5. Use Vivado to synthesize the block and show that it can synthesize without errors. You do not need to actually load a chip and show this working on the hardware.