Report generated on 2025-10-17 13:12 GMT by riscof v

Environment

Riscof Version	1.25.3
Riscv-arch-test Version/Commit Id	-
DUT	uemu
Reference	sail c simulator
ISA	RV64IMAFDCSUZicsr_Zifencei
User Spec Version	2.3
Privilege Spec Version	1.10

Yaml

Show all details / Hide all details

Name
/home/sn/workspace/uemu/verif/riscof_work/uemu_isa_checked.yaml *(show details)*
/home/sn/workspace/uemu/verif/riscof_work/uemu_platform_checked.yaml *(show details)*

Please visit YAML specifications for more information.

Summary

1202Passed, 0Failed

Results

Show all details / Hide all details

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b10-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b10-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b11-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b11-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b12-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b12-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b13-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b13-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fclass.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fclass.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.w_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.w_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.w_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.w_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.wu_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.wu_b25-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.wu_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.wu_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.s.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.s.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.s.d_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.s.d_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.s.d_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.s.d_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.s.d_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.s.d_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.s.d_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.s.d_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.s.d_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.s.d_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.s.d_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.s.d_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.w.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.w.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.w.d_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.w.d_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.w.d_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.w.d_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.w.d_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.w.d_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.w.d_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.w.d_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.w.d_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.w.d_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.w.d_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.w.d_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.wu.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.wu.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.wu.d_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.wu.d_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.wu.d_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.wu.d_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.wu.d_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.wu.d_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.wu.d_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.wu.d_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.wu.d_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.wu.d_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.wu.d_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.wu.d_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b20-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b20-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b21-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b21-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b6-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b6-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fdiv.d_b9-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fdiv.d_b9-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/feq.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/feq.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/feq.d_b19-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/feq.d_b19-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fld-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fld-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fle.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fle.d_b1-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fle.d_b19-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fle.d_b19-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/flt.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/flt.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/flt.d_b19-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/flt.d_b19-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b14-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b14-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-001.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-002.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-003.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-004.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-005.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-006.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-007.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-008.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-009.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-010.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-011.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-012.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-013.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-014.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-015.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-016.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-017.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-018.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-019.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-022.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
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Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-034.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-035.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-036.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-037.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-038.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-039.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-040.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-054.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-056.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-069.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad

Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-071.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-088.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-089.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-090.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-091.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-092.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-093.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-094.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-095.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-096.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-097.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-098.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-099.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-100.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-101.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-102.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-103.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-104.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-105.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-106.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-107.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-108.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-109.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-110.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-111.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-112.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-113.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-114.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-115.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-116.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-117.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-118.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-119.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-120.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-121.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-122.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-123.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-124.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-125.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-126.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-127.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-128.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-129.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-130.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-131.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-132.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b15/fmadd.d_b15-133.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b15/fmad
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b16-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b16-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b17-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b17-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b18-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b18-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b6-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b6-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmadd.d_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmadd.d_b8-01.S

Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmax.d_b19-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmax.d_b19-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmin.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmin.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmin.d_b19-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmin.d_b19-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b14-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b14-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-001.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-002.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-003.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-004.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-005.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-006.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-007.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-008.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-009.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-010.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-011.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-012.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-013.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-014.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-015.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-017.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
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Test	Result	Path
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Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-088.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-089.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-090.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-091.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-092.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-093.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-094.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-096.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
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Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-108.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-126.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b15/fmsub.d_b15-127.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b15/fmsu
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fmsub.d_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fmsub.d_b7-01.S

Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-006.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 006.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-007.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 007.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-008.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 008.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-009.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 009.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-010.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 010.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-011.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 011.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-012.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 012.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-013.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 013.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-014.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 014.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-015.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 015.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-016.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 016.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-017.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 017.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-018.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 018.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-019.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 019.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-020.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 020.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-021.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 021.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-022.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 022.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-023.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 023.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-024.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 024.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-025.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 025.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-026.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 026.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-027.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 027.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-028.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 028.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-029.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 029.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-030.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 030.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-031.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 031.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-032.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 032.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-033.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 033.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-034.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 034.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-035.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 035.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-036.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 036.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-037.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 037.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-038.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 038.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-039.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 039.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-040.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 040.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-041.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 041.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-042.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 042.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-043.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 043.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-044.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 044.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-045.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 045.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-046.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 046.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-047.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 047.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-048.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 048.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-049.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 049.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-050.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 050.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-051.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 051.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-052.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 052.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-053.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 053.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-054.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 054.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-055.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 055.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-056.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 056.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-057.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 057.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-058.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 058.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-059.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 059.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-060.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 060.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-061.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 061.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-062.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 062.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-063.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 063.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-064.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 064.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-065.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 065.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-066.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 066.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-067.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 067.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-068.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 068.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-069.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 069.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-070.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 070.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-071.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 071.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-072.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 072.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-073.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 073.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-074.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 074.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-075.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 075.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-076.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 076.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-077.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 077.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-078.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 078.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-079.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 079.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-080.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 080.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-081.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 081.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-082.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 082.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-083.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 083.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-084.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 084.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-085.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 085.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-086.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 086.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-087.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 087.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-088.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 088.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-089.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 089.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-090.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 090.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-091.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 091.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-092.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 092.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-093.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 093.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-094.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 094.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-095.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 095.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-096.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 096.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-097.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 097.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-098.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 098.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-099.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 099.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-100.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 100.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-101.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 101.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-102.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 102.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-103.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 103.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-104.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 104.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-105.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 105.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-106.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 106.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-107.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 107.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-108.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 108.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-109.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 109.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-110.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 110.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-111.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 111.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-112.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 112.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-113.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 113.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-114.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 114.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-115.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 115.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-116.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 116.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-117.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 117.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-118.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 118.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-119.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 119.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-120.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 120.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-121.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 121.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-122.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 122.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-123.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 123.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-124.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 124.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-125.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 125.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-126.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 126.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-127.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 127.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-128.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 128.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-129.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 129.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-130.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 130.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-131.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 131.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-132.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 132.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b15/fnmadd.d_b15-133.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b15/fnm 133.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b16-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b16-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b17-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b17-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b18-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b18-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b6-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b6-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmadd.d_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmadd.d_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b14-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b14-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-001.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-001.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-002.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-002.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-003.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-003.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-004.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-004.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-005.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-005.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-006.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-006.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-007.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-007.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-008.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-008.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-009.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-009.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-010.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-010.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-011.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-011.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-012.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-012.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-013.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-013.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-014.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-014.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-015.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-015.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-016.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-016.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-017.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-017.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-018.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-018.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-019.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-019.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-020.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-020.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-021.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-021.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-022.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-022.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-023.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-023.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-024.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-024.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-025.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-025.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-026.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-026.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-027.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-027.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-028.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-028.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-029.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 029.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-030.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 030.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-031.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 031.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-032.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 032.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-033.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 033.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-034.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 034.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-035.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 035.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-036.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 036.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-037.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 037.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-038.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 038.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-039.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 039.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-040.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 040.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-041.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 041.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-042.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 042.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-043.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 043.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-044.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 044.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-045.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 045.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-046.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 046.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-047.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 047.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-048.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 048.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-049.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 049.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-050.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 050.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-051.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 051.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-052.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 052.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-053.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 053.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-054.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 054.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-055.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 055.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-056.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 056.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-057.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 057.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-058.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 058.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-059.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 059.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-060.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 060.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-061.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 061.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-062.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 062.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-063.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 063.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-064.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 064.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-065.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 065.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-066.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 066.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-067.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 067.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-068.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 068.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-069.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 069.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-070.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 070.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-071.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 071.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-072.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 072.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-073.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 073.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-074.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 074.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-075.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 075.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-076.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 076.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-077.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 077.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-078.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 078.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-079.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 079.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-080.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 080.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-081.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 081.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-082.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 082.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-083.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 083.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-084.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 084.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-085.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 085.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-086.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 086.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-087.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 087.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-088.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 088.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-089.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 089.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-090.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 090.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-091.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 091.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-092.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 092.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-093.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 093.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-094.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 094.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-095.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 095.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-096.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 096.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-097.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 097.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-098.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 098.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-099.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 099.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-100.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 100.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-101.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 101.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-102.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 102.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-103.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 103.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-104.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 104.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-105.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 105.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-106.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 106.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-107.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 107.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-108.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 108.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-109.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 109.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-110.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 110.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-111.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-112.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 112.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-113.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 113.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-114.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 114.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-115.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 115.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-116.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 116.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-117.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 117.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-118.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 118.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-119.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 119.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-120.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 120.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-121.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 121.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-122.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 122.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-123.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 123.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-124.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 124.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-125.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 125.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-126.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 126.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-127.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 127.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-128.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 128.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-130.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 130.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-131.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 131.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-132.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 132.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b15/fnmsub.d_b15-133.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b15/fnm 133.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b16-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b16-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b17-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b17-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b18-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b18-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b4-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b6-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b6-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fnmsub.d_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fnmsub.d_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fsd-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fsd-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fsgnj.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fsgnj.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fsgnjn.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fsgnjn.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fsgnjx.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fsgnjx.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fsqrt.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fsqrt.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fsqrt.d_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fsqrt.d_b2-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fsqrt.d_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fsqrt.d_b3-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fssub.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fssub.d_b1-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fssub.d_b12-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fssub.d_b12-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fssub.d_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fssub.d_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fssub.d_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fssub.d_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fssub.d_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fssub.d_b4-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fssub.d_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fssub.d_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b10-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b10-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b11-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b11-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b12-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b12-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b13-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b13-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b5-01.S

Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fadd_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fadd_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fclass_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fclass_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fcvt.s.w_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fcvt.s.w_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fcvt.s.w_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fcvt.s.w_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fcvt.s.wu_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fcvt.s.wu_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fcvt.s.wu_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fcvt.s.wu_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fcvt.w.s_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fcvt.w.s_b1-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fcvt.wu.s_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fcvt.wu.s_b27-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fcvt.wu.s_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fcvt.wu.s_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fdiv_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fdiv_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fdiv_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fdiv_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fdiv_b20-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fdiv_b20-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fdiv_b21-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fdiv_b21-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fdiv_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fdiv_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fdiv_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fdiv_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fdiv_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fdiv_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fdiv_b6-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fdiv_b6-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fle_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fle_b1-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/flt_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/flt_b1-01.S

Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/flw-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/flw-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmadd_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmadd_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmadd_b14-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmadd_b14-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmadd_b15/fmadd_b15-001.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmadd_b15/fmadd_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmadd_b15/fmadd_b15-002.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmadd_b15/fmadd_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmadd_b15/fmadd_b15-003.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmadd_b15/fmadd_
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmadd_b15/fmadd_b15-005.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmadd_b15/fmadd_
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmadd_b15/fmadd_b15-033.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmadd_b15/fmadd_

Test	Result	Path
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Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-017.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-018.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-019.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-020.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-021.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-022.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-023.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-024.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-025.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-026.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-027.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-028.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-029.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-030.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-031.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-032.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-033.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-034.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-035.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-036.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-037.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-038.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-039.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-040.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-041.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-042.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-043.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-044.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-045.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-046.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-047.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-048.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-049.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b15/fmsub_b15-050.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b15/fmsub_
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b16-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b16-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b17-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b17-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b18-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b18-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b6-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b6-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmsub_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmsub_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b6-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b6-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmul_b9-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmul_b9-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.w.x_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.w.x_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.w.x_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.w.x_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.x.w_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.x.w_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.x.w_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.x.w_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.x.w_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.x.w_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.x.w_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.x.w_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.x.w_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.x.w_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.x.w_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.x.w_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fmv.x.w_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fmv.x.w_b29-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b14-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b14-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-001.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-002.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-003.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-004.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-005.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-006.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-007.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-008.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-009.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-010.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-011.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-012.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-013.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-014.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-015.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-016.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-017.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-018.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-019.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-020.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-021.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-022.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-023.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-024.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-025.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-026.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-027.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-029.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-031.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-032.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-033.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-034.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-035.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac

Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-037.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-038.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-039.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-040.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-041.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-042.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-043.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-044.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-045.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-046.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-047.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-048.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-049.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b15/fnmadd_b15-050.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b15/fnmac
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b16-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b16-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b17-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b17-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b2-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b5-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmadd_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmadd_b7-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-002.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-003.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-004.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-005.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-006.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-008.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-009.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-010.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu

Test	Result	Path
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-012.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-013.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-014.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-015.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-020.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-021.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-022.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-023.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-024.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-025.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-026.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-027.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-028.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-029.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-030.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-031.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-032.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-033.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-034.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-035.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-036.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-037.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-038.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-039.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-040.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-041.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-042.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-043.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-044.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-045.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-046.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-047.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-048.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-049.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b15/fnmsub_b15-050.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b15/fnmsu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b16-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b16-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b17-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b17-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b18-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b18-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b6-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b6-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fnmsub_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fnmsub_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsgnj_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsgnj_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsgnjn_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsgnjn_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsgnjx_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsgnjx_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b20-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b20-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsqrt_b9-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsqrt_b9-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b10-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b10-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b11-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b11-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b12-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b12-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b13-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b13-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b2-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b3-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b4-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b5-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b7-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsub_b8-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsub_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/F/src/fsw-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/F/src/fsw-align-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amoadd.d-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amoadd.d-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amoadd.w-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amoadd.w-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amoand.d-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amoand.d-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amoand.w-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amoand.w-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amomax.d-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amomax.d-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amomax.w-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amomax.w-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amomaxu.d-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amomaxu.d-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amomaxu.w-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amomaxu.w-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amomin.d-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amomin.d-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amomin.w-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amomin.w-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amominu.d-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amominu.d-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amoswap.w-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amoswap.w-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amoxor.d-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amoxor.d-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/A/src/amoxor.w-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/A/src/amoxor.w-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cadd-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cadd-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/caddi-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/caddi-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/caddi16sp-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/caddi16sp-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/caddi4spn-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/caddi4spn-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/caddiw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/caddiw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/caddw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/caddw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cand-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cand-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/candi-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/candi-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cbeqz-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cbeqz-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cbnez-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cbnez-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cebreak-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cebreak-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cj-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cj-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cjalr-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cjalr-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cjr-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cjr-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cld-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cld-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cldsp-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cldsp-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cli-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cli-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/clui-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/clui-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/clw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/clw-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/clwsp-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/clwsp-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cmv-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cmv-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cnop-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cnop-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cor-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cor-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/csd-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/csd-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/csdsp-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/csdsp-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cslli-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cslli-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/csrai-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/csrai-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/csrli-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/csrli-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/csub-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/csub-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/csubw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/csubw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/csw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/csw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cswsp-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cswsp-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/cxor-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/cxor-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/misalign1-cjalr-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/misalign1-cjalr-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/C/src/misalign1-cjr-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/C/src/misalign1-cjr-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.d.l_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.d.l_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.d.l_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.d.l_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.d.lu_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.d.lu_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.d.lu_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.d.lu_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.l.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.l.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.l.d_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.l.d_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.l.d_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.l.d_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.l.d_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.l.d_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.l.d_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.l.d_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.l.d_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.l.d_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.l.d_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.l.d_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.lu.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.lu.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.lu.d_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.lu.d_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.lu.d_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.lu.d_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.lu.d_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.lu.d_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.lu.d_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.lu.d_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.lu.d_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.lu.d_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fcvt.lu.d_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fcvt.lu.d_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.d.x_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.d.x_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.d.x_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.d.x_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.x.d_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.x.d_b1-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.x.d_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.x.d_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.x.d_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.x.d_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.x.d_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.x.d_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.x.d_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.x.d_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.x.d_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.x.d_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/D/src/fmv.x.d_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/D/src/fmv.x.d_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.l.s_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.l.s_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.l.s_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.l.s_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.l.s_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.l.s_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.l.s_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.l.s_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.l.s_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.l.s_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.l.s_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.l.s_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.l.s_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.l.s_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.lu.s_b1-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.lu.s_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.lu.s_b22-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.lu.s_b22-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.lu.s_b23-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.lu.s_b23-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.lu.s_b24-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.lu.s_b24-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.lu.s_b27-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.lu.s_b27-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.lu.s_b28-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.lu.s_b28-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.lu.s_b29-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.lu.s_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.s.l_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.s.l_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.s.l_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.s.l_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.s.lu_b25-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.s.lu_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/F/src/fcvt.s.lu_b26-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/F/src/fcvt.s.lu_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/add-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/add-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/addi-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/addi-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/addiw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/addiw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/addw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/addw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/and-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/and-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/andi-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/andi-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/auipc-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/auipc-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/beq-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/beq-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/bge-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/bge-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/bgeu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/bgeu-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/blt-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/blt-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/bltu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/bltu-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/bne-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/bne-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/fence-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/fence-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/jal-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/jal-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/jalr-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/jalr-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/lb-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/lb-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/lbu-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/lbu-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/ld-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/ld-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/lh-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/lh-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/lhu-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/lhu-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/lui-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/lui-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/lw-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/lw-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/lwu-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/lwu-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/misalign1-jalr-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/misalign1-jalr-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/or-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/or-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/ori-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/ori-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sb-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sb-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sd-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sd-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sh-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sh-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sll-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sll-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/slli-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/slli-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/slliw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/slliw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sllw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sllw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/slt-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/slt-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/slti-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/slti-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sltiu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sltiu-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sltu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sltu-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sra-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sra-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/srai-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/srai-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sraiw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sraiw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sraw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sraw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/srl-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/srl-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/srli-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/srli-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/srliw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/srliw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/srlw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/srlw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sub-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sub-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/subw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/subw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/sw-align-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/sw-align-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/xor-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/xor-01.S

Test	Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/I/src/xori-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/I/src/xori-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/div-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/div-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/divu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/divu-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/divuw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/divuw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/divw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/divw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/mul-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/mul-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/mulh-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/mulh-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/mulhsu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/mulhsu-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/mulhu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/mulhu-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/mulw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/mulw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/rem-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/rem-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/remu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/remu-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/remuw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/remuw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/M/src/remw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/M/src/remw-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/Zifencei/src/Fencei.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/Zifencei/src/Fencei.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/ebreak.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/ebreak.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/ecall.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/ecall.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-beq-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-be
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-bge-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-bg
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-bgeu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-bg
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-blt-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-blt
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-bltu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-blt
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-bne-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-bn
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-jal-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-jal
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-ld-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-ld
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-lh-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-lh
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-lhu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-lhu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-lw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-lw-
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-lwu-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-lwu
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-sd-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-sd
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-sh-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-sh
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign-sw-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign-sw
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv64i_m/privilege/src/misalign2-jalr-01.S	Passed *(show details)*	/home/sn/workspace/uemu/verif/riscof_work/rv64i_m/privilege/src/misalign2-ja