

Environment

Riscof Version	1.25.3
Riscv-arch-test Version/Commit Id	-
DUT	uemu
Reference	sail c simulator
ISA	RV64IMAFDSUZicsr_Zifencei
User Spec Version	2.3
Privilege Spec Version	1.10

Yaml

[Show all details](#) / [Hide all details](#)

Name
/home/sn/workspace/uemu/verif/riscof_work/uemu_isa_checked.yaml <i>(show details)</i>
/home/sn/workspace/uemu/verif/riscof_work/uemu_platform_checked.yaml <i>(show details)</i>

Please visit [YAML specifications](#) for more information.

Summary

 1167Passed,  0Failed

Results

[Show all details](#) / [Hide all details](#)

▼ Test	▲ Result	Path
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b1-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b10-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b10-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b11-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b11-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b12-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b12-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b13-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b13-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b2-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b2-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b3-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b3-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b4-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b4-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b5-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b5-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b7-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b7-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fadd.d_b8-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fadd.d_b8-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fclass.d_b1-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fclass.d_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b1-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b1-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b22-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b22-01.S
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/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.s_b29-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.s_b29-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.w_b25-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.w_b25-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.w_b26-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.w_b26-01.S
/home/sn/workspace/uemu/riscv-arch-test/riscv-test-suite/rv32i_m/D/src/fcvt.d.wu_b25-01.S	Passed <i>(show details)</i>	/home/sn/workspace/uemu/verif/riscof_work/rv32i_m/D/src/fcvt.d.wu_b25-01.S

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