STANDARD HCMOS LS TTL

[16, 15, A, B, 12, 11, 10, 9,	VCC Wr1 WRITE ENWENR Rd1 Rd2
	74LS670 4×4RAM
V4HC6/U6≓ 4X4RAM Wr2Wr3 Wr4 READ Rd4 Rd3 GND	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
1 2 3 B A 6 7 8	INIZWISWI4 READ RO4 ROS UND
16 15 Å B 12 11 10 9	16 15 A B 12 11 10 9
VCC Wr1 WRITE ENW ENR Rd1 Rd2	VCC WIT WRITE ENWENR Rd1 Rd2
74HC670 :: 4×4RAM	\74I S670«≟≟≟ 4x4RΔM
	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
1 2 3 B A 6 7 8	1 2 3 B A 6 7 8
16 15 A B 12 11 10 9	16 15 A B 12 11 10 9
VCC Wr1 WRITE ENW ENR Rd1 Rd2	VCC Wr1 WRITE ENW ENR Rd1 Rd2
74HC670 :: 4×4RAM	74LS670 ::
Wr2 Wr3 Wr4 READ Rd4 Rd3 GND	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
16 15 Å B 12 11 10 9	16 15 A B 12 11 10 9
VCC W/1 WRITE ENW ENR Rd1 Rd2	VCC W/1 WRITE ENWEND Rd1 Rd2
74HC670 - 4x4RAM	VCC WT1 WRITE ENW ENR Rd1 Rd2 74LS670
	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
1 2 3 B A 6 7 8	1 2 3 B A 6 7 8
16 15 A B 12 11 10 9	16 15 A B 12 11 10 9
VCC W/1 WRITE ENW ENR Rd1 Rd2	VCC WIT WRITE ENWENR Rd1 Rd2
74HC670:::	\74LS670 ::: 4×4RAM
Wr2 Wr3 Wr4 READ Rd4 Rd3 GND	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
1 2 3 B A 6 / 8	16 15 A B 12 11 10 9
16 15 A B 12 11 10 9	16 15 A B 12 11 10 9
74HC670 === 4×4RAM	74LS670
Wr2 Wr3 Wr4 READ Rd4 Rd3 GND	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
1 2 3 B A 6 7 8	11 2 3 B A 6 7 8
16 15 A B 12 11 10 9	16 15 A B 12 11 10 9
VCC Wr1 WRITE ENWENR Rd1 Rd2	VCC WIT WRITE ENWEND ROT ROZ
74HC670 :: +	174LS670 ₽=≥ 4×4RAM
Wr2 Wr3 Wr4 READ Rd4 Rd3 GND	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
1 2 3 B A 6 7 8	1 2 3 B A 6 7 8
16 15 A B 12 11 10 9	16 15 A B 12 11 10 9
74HC670 4×4RAM	74LS670 === 4x4RAM
Wr2 Wr3 Wr4 READ Rd4 Rd3 GND	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
1 2 3 B A 6 7 8	11 2 3 WI 4 READ ROARDS OND
16 15 A B 12 11 10 9	16 15 A B 12 11 10 9
VCC WIT WRITE ENWENR Rd1 Rd2	VCC WIT WRITE ENWENR Rd1 Rd2
74HC670 :: 4×4RAM	\74LS670 :°≐≟≟ 4×4RAM
Wr2 Wr3 Wr4 READ Rd4 Rd3 GND	Wr2Wr3 Wr4 READ Rd4 Rd3 GND
1 2 3 B A 6 7 8	11 2 3 B A 6 7 8
16 15 A B 12 11 10 9	16 15 A B 12 11 10 9
	VCC WE1 WRITE ENWENE Rd1 Rd2
74HC670 4×4RAM	
Wr2Wr3Wr4 READ Rd4 Rd3 GND	Wr2 Wr3 Wr4 READ Rd4 Rd3 GND
1	11 4 3 B A 6 / 8