

HCMOS	LS TTL
-------	--------

Figure 10 displays 20 circuit diagrams arranged in a 10x2 grid. Each diagram shows a 4-bit data bus (16, 15, 14, 13) and a 4-bit address bus (12, 11, 10, 9). The diagrams illustrate various combinations of 74HC75 and 74ALS75 flip-flops, LATCH inputs, and clock signals (CLK, CH, CH2). The diagrams are organized into two columns, with the left column labeled '74HC75' and the right column labeled '74ALS75'. Each diagram shows a different configuration for setting and clearing the flip-flops using the LATCH and clock inputs.

ALTERNATE

[illegible]