

HCMOS LS TTL

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Figure 1 displays a 10x3 grid of circuit diagrams. Each row contains three diagrams: a 74HC14, a NOT gate, and a 74LS14. The diagrams show the internal components and pin connections of these logic devices. The 74HC14 and 74LS14 diagrams include pin numbers (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16) and labels for various pins (VCC, GND, A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z). The NOT gate diagram shows the input and output pins. The diagrams are arranged in three columns: 74HC14, NOT, and 74LS14. The rows are numbered 1 to 10. The diagrams show the circuit components and their connections, with the NOT gate symbol in the middle column.