

HCMOS	LS TTL
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Figure 10 displays a 10x10 grid of 100 circuit diagrams. Each diagram is a small schematic showing a combination of 74HC75 and 74ALS75 flip-flops, LATCH inputs, and clock signals (CLK, GND, VCC, 3D, 4D, 6D, 8D). The diagrams are arranged in a grid where each row and column represents a different combination of these components. The labels for each diagram are as follows:

Row	Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10
1	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
2	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
3	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
4	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
5	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
6	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
7	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
8	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
9	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75
10	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75	74HC75	74ALS75

ALTERNATE

[illegible]