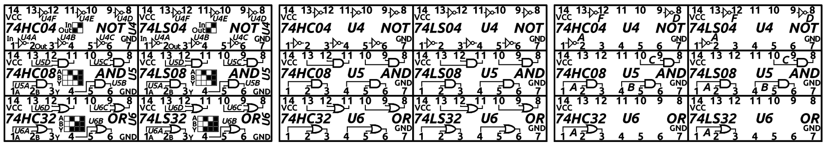
CLOCK MODULE

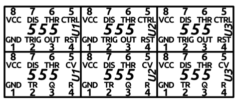
PRINT, CUT, AND PASTE CHIP PIN LABELS

HIGH RESOLUTION PRINTER — *HC* — *LS*

KEEP IT SIMPLE — *HC* — *LS*

...SUPER SIMPLE — *HC* — *LS*



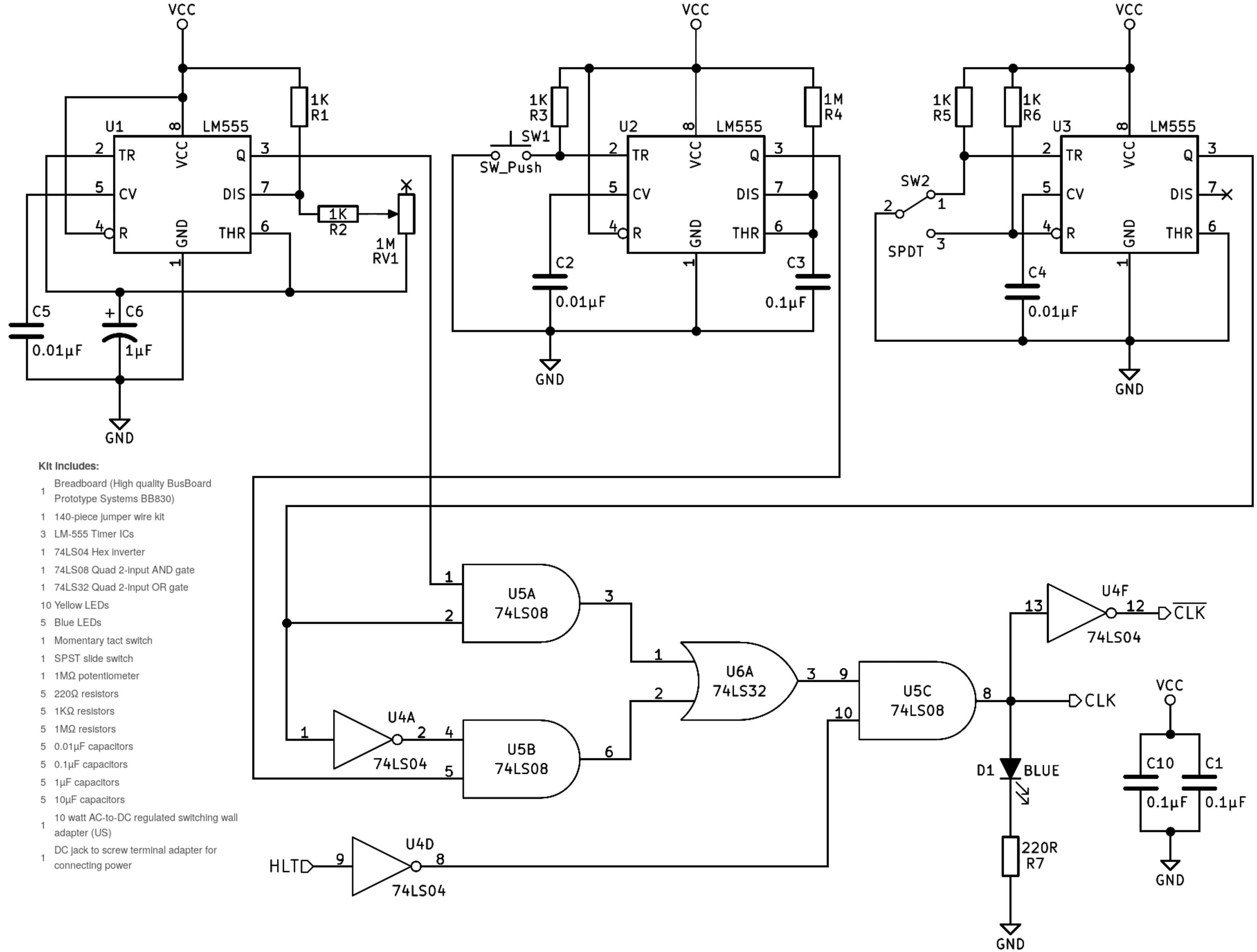


-SLIGHTLY LONGER PIN NAMES

-MATCHES SCHEMATIC PIN NAMES

This file contains chip labels, a black and white schematic sized for standard A4 printer paper, and the 555, 7404, 7408, and 7432 datasheets. The datasheets have had their chip package size and ordering information pages removed as these are useless for most people and more than halves the total number of pages. There is also a second copy of the schematic in a landscape orientation on the last page for easier digital viewing

ORIGINAL LABELS AND UNOFFICIAL DOCUMENTATION BY JAKE L.



Kit Includes:

1	Breadboard (High quality BusBoard Prototype Systems BB830)
1	140-piece jumper wire kit
3	LM-555 Timer ICs
1	74LS04 Hex inverter
1	74LS08 Quad 2-input AND gate
1	74LS32 Quad 2-input OR gate
10	Yellow LEDs
5	Blue LEDs
1	Momentary tact switch
1	SPST slide switch
1	1MΩ potentiometer
5	220Ω resistors
5	1KΩ resistors
5	1MΩ resistors
5	0.01µF capacitors
5	0.1µF capacitors
5	1µF capacitors
5	10µF capacitors
1	10 watt AC-to-DC regulated switching wall adapter (US)
1	DC jack to screw terminal adapter for connecting power

LM555/NE555/SA555

Single Timer

Features

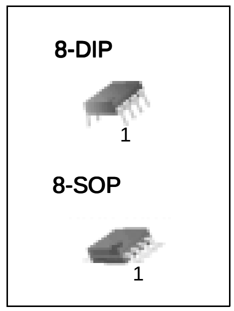
- High Current Drive Capability (200mA)
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- Timing From µSec to Hours
- Turn off Time Less Than 2µSec

Applications

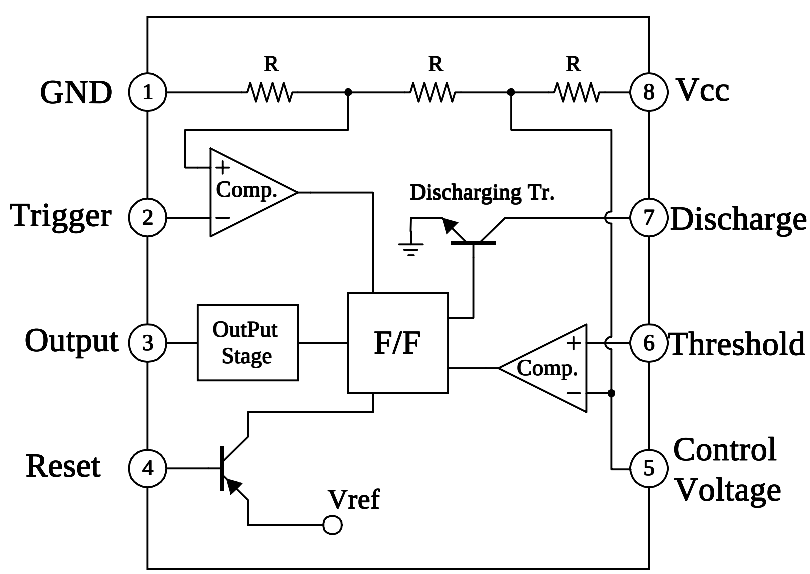
- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing

Description

The LM555/NE555/SA555 is a highly stable controller capable of producing accurate timing pulses. With a monostable operation, the time delay is controlled by one external resistor and one capacitor. With an astable operation, the frequency and duty cycle are accurately controlled by two external resistors and one capacitor.



Internal Block Diagram



Rev. 1.0.3

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (Soldering 10sec)	T_{LEAD}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range LM555/NE555 SA555	T_{OPR}	 0 ~ +70 -40 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics

(T_A = 25°C, V_{CC} = 5 ~ 15V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-	4.5	-	16	V
Supply Current (Low Stable) (Note1)	I_{CC}	V_{CC} = 5V, $R_L = \infty$	-	3	6	mA
		V_{CC} = 15V, $R_L = \infty$	-	7.5	15	mA
Timing Error (Monostable) Initial Accuracy (Note2) Drift with Temperature (Note4) Drift with Supply Voltage (Note4)	ACCUR $\Delta t/\Delta T$ $\Delta t/\Delta V_{CC}$	R_A = 1kΩ to100kΩ C = 0.1μF	-	1.0 50 0.1	3.0 0.5	% ppm/°C %/V
Timing Error (Astable) Intial Accuracy (Note2) Drift with Temperature (Note4) Drift with Supply Voltage (Note4)	ACCUR $\Delta t/\Delta T$ $\Delta t/\Delta V_{CC}$	R_A = 1kΩ to 100kΩ C = 0.1μF	-	2.25 150 0.3	-	% ppm/°C %/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15V	-	10.0	-	V
		V_{CC} = 5V	-	3.33	-	V
Threshold Current (Note3)	I_{TH}	-	-	0.1	0.25	μA
Trigger Voltage	V_{TR}	V_{CC} = 5V	1.1	1.67	2.2	V
		V_{CC} = 15V	4.5	5	5.6	V
Trigger Current	I_{TR}	V_{TR} = 0V		0.01	2.0	μA
Reset Voltage	V_{RST}	-	0.4	0.7	1.0	V
Reset Current	I_{RST}	-		0.1	0.4	mA
Low Output Voltage	V_{OL}	V_{CC} = 15V I_{SINK} = 10mA I_{SINK} = 50mA	-	0.06 0.3	0.25 0.75	V V
		V_{CC} = 5V I_{SINK} = 5mA	-	0.05	0.35	V
High Output Voltage	V_{OH}	V_{CC} = 15V I_{SOURCE} = 200mA I_{SOURCE} = 100mA	12.75	12.5 13.3	-	V V
		V_{CC} = 5V I_{SOURCE} = 100mA	2.75	3.3	-	V
Rise Time of Output (Note4)	t_R	-	-	100	-	ns
Fall Time of Output (Note4)	t_F	-	-	100	-	ns
Discharge Leakage Current	I_{LKG}	-	-	20	100	nA

Notes:

1. When the output is high, the supply current is typically 1mA less than at V_{CC} = 5V.
2. Tested at V_{CC} = 5.0V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$ for 15V operation, the max. total R = 20MΩ, and for 5V operation, the max. total R = 6.7MΩ.
4. These parameters, although guaranteed, are not 100% tested in production.

Application Information

Table 1 below is the basic operating table of 555 timer:

Table 1. Basic Operating Table

Threshold Voltage (V_{th})(PIN 6)	Trigger Voltage (V_{tr})(PIN 2)	Reset(PIN 4)	Output(PIN 3)	Discharging Tr. (PIN 7)
Don't care	Don't care	Low	Low	ON
V_{th} > 2Vcc / 3	V_{th} > 2Vcc / 3	High	Low	ON
Vcc / 3 < V_{th} < 2 Vcc / 3	Vcc / 3 < V_{th} < 2 Vcc / 3	High	-	-
V_{th} < Vcc / 3	V_{th} < Vcc / 3	High	High	OFF

When the low signal input is applied to the reset terminal, the timer output remains low regardless of the threshold voltage or the trigger voltage. Only when the high signal is applied to the reset terminal, the timer's output changes according to threshold voltage and trigger voltage.

When the threshold voltage exceeds 2/3 of the supply voltage while the timer output is high, the timer's internal discharge Tr. turns on, lowering the threshold voltage to below 1/3 of the supply voltage. During this time, the timer output is maintained low. Later, if a low signal is applied to the trigger voltage so that it becomes 1/3 of the supply voltage, the timer's internal discharge Tr. turns off, increasing the threshold voltage and driving the timer output again at high.

1. Monostable Operation

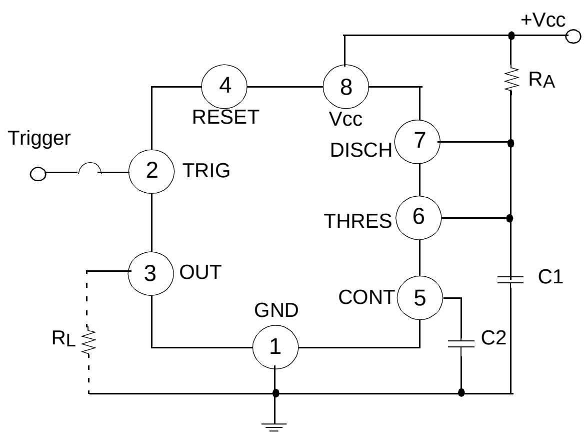


Figure 1. Monoatable Circuit

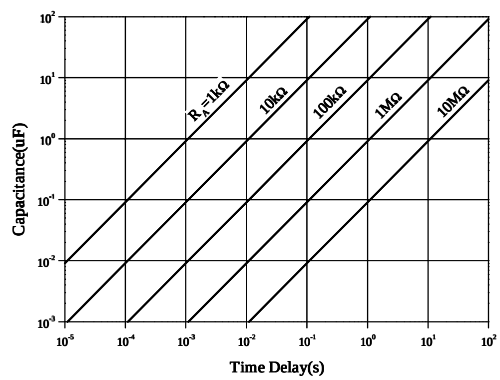


Figure 2. Resistance and Capacitance vs. Time delay(t_d)

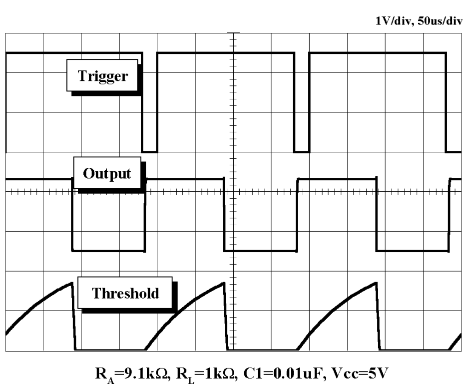


Figure 3. Waveforms of Monostable Operation

Figure 1 illustrates a monostable circuit. In this mode, the timer generates a fixed pulse whenever the trigger voltage falls below Vcc/3. When the trigger pulse voltage applied to the #2 pin falls below Vcc/3 while the timer output is low, the timer's internal flip-flop turns the discharging Tr. off and causes the timer output to become high by charging the external capacitor C1 and setting the flip-flop output at the same time.
The voltage across the external capacitor C1, V_{C1} increases exponentially with the time constant t=R_A*C and reaches 2Vcc/3 at td=1.1R_A*C. Hence, capacitor C1 is charged through resistor R_A. The greater the time constant R_AC, the longer it takes for the V_{C1} to reach 2Vcc/3. In other words, the time constant R_AC controls the output pulse width.
When the applied voltage to the capacitor C1 reaches 2Vcc/3, the comparator on the trigger terminal resets the flip-flop, turning the discharging Tr. on. At this time, C1 begins to discharge and the timer output converts to low.
In this way, the timer operating in the monostable repeats the above process. Figure 2 shows the time constant relationship based on R_A and C. Figure 3 shows the general waveforms during the monostable operation.
It must be noted that, for a normal operation, the trigger pulse voltage needs to maintain a minimum of Vcc/3 before the timer output turns low. That is, although the output remains unaffected even if a different trigger pulse is applied while the output is high, it may be affected and the waveform does not operate properly if the trigger pulse voltage at the end of the output pulse remains at below Vcc/3. Figure 4 shows such a timer output abnormality.

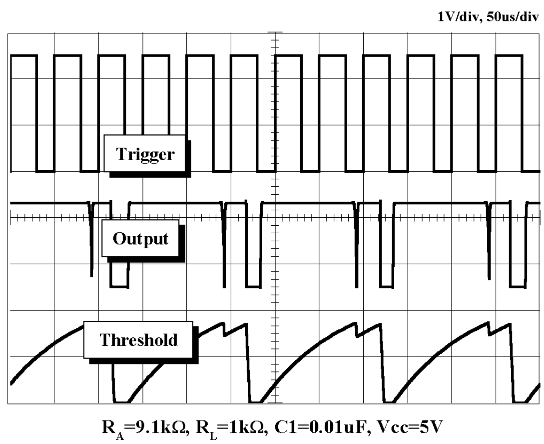


Figure 4. Waveforms of Monostable Operation (abnormal)

2. Astable Operation

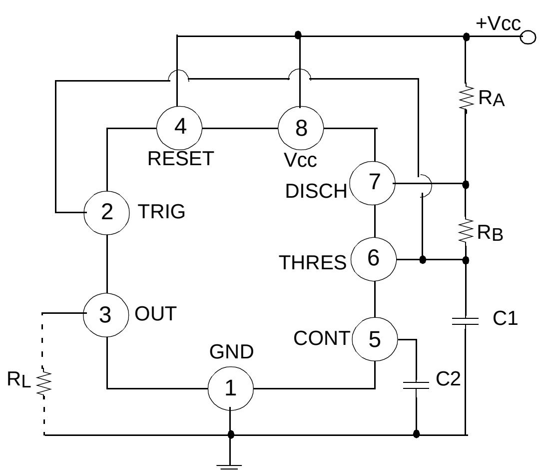


Figure 5. Astable Circuit

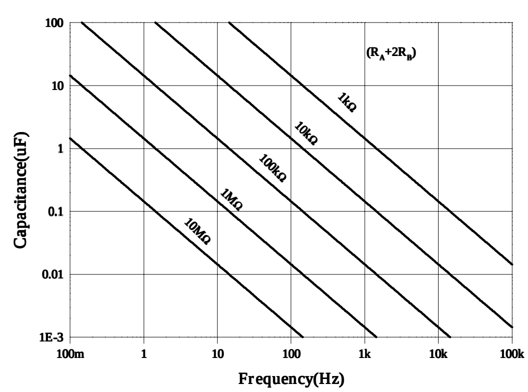


Figure 6. Capacitance and Resistance vs. Frequency

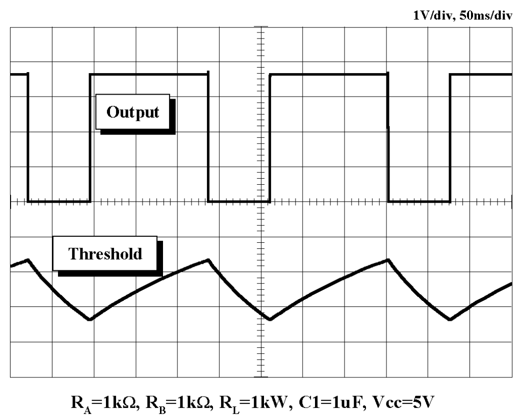
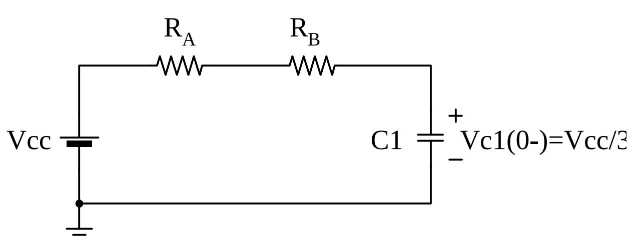


Figure 7. Waveforms of Astable Operation

An astable timer operation is achieved by adding resistor R_B to Figure 1 and configuring as shown on Figure 5. In the astable operation, the trigger terminal and the threshold terminal are connected so that a self-trigger is formed, operating as a multi vibrator. When the timer output is high, its internal discharging Tr. turns off and the V_{C1} increases by exponential function with the time constant (R_A+R_B)*C.
When the V_{C1}, or the threshold voltage, reaches 2Vcc/3, the comparator output on the trigger terminal becomes high, resetting the F/F and causing the timer output to become low. This in turn turns on the discharging Tr. and the C1 discharges through the discharging channel formed by R_B and the discharging Tr. When the V_{C1} falls below Vcc/3, the comparator output on the trigger terminal becomes high and the timer output becomes high again. The discharging Tr. turns off and the V_{C1} rises again.
In the above process, the section where the timer output is high is the time it takes for the V_{C1} to rise from Vcc/3 to 2Vcc/3, and the section where the timer output is low is the time it takes for the V_{C1} to drop from 2Vcc/3 to Vcc/3. When timer output is high, the equivalent circuit for charging capacitor C1 is as follows:



$$C_1 \frac{dv_{c1}}{dt} = \frac{V_{cc} - V(0\text{-})}{R_A + R_B} \qquad (1)$$

$$V_{C1}(0+) = V_{CC}/3 \qquad (2)$$

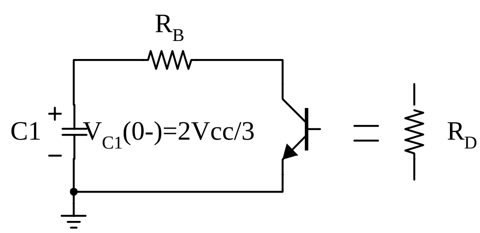
$$V_{C1}(t) = V_{CC}\left(1 - \frac{2}{3}e^{-\left(-\frac{t}{(R_A + R_B)C1}\right)}\right) \qquad (3)$$

Since the duration of the timer output high state(t_H) is the amount of time it takes for the $V_{C1}(t)$ to reach 2Vcc/3,

$$V_{C1}(t) = \frac{2}{3}V_{CC} = V_{CC}\left(1 - \frac{2}{3}e^{-\left(-\frac{t_H}{(R_A + R_B)C1}\right)}\right) \qquad (4)$$

$$t_H = C_1(R_A + R_B)\ln 2 = 0.693(R_A + R_B)C_1 \qquad (5)$$

The equivalent circuit for discharging capacitor C1, when timer output is low is, as follows:



$$C_1\frac{dv_{C1}}{dt} + \frac{1}{R_A + R_B}V_{C1} = 0 \qquad (6)$$

$$V_{C1}(t) = \frac{2}{3}V_{CC}e^{-\frac{t}{(R_A + R_D)C1}} \qquad (7)$$

Since the duration of the timer output low state(t_L) is the amount of time it takes for the V_{C1}(t) to reach Vcc/3,

$$\frac{1}{3}V_{CC} = \frac{2}{3}V_{CC}e^{-\frac{t_L}{(R_A + R_D)C1}} \qquad (8)$$

$$t_L = C_1(R_B + R_D)\ln 2 = 0.693(R_B + R_D)C_1 \qquad (9)$$

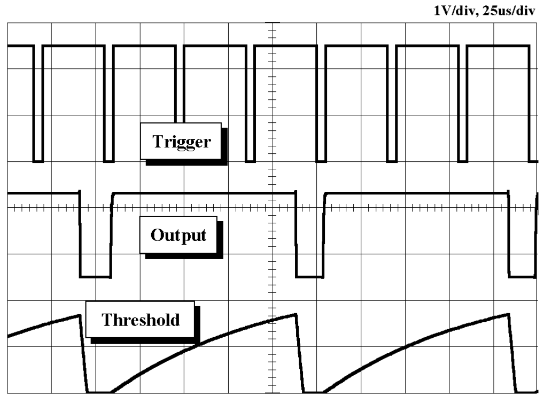
Since R_D is normally $R_B \gg R_D$ although related to the size of discharging Tr.,
$t_L = 0.693 R_B C_1$ (10)

Consequently, if the timer operates in astable, the period is the same with
'$T = t_H + t_L = 0.693(RA+R_B)C_1 + 0.693R_BC_1 = 0.693(R_A+2R_B)C_1$' because the period is the sum of the charge time and discharge time. And since frequency is the reciprocal of the period, the following applies.

$$\text{frequency,} \qquad f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_1} \qquad (11)$$

3. Frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 1 can be made to operate as a frequency divider. Figure 8. illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.



R_A=9.1kΩ, R_L=1kΩ, C1=0.01uF, Vcc=5V

Figure 8. Waveforms of Frequency Divider Operation

4. Pulse Width Modulation

The timer output waveform may be changed by modulating the control voltage applied to the timer's pin 5 and changing the reference of the timer's internal comparators. Figure 9 illustrates the pulse width modulation circuit.
When the continuous trigger pulse train is applied in the monostable mode, the timer output width is modulated according to the signal applied to the control terminal. Sine wave as well as other waveforms may be applied as a signal to the control terminal. Figure 10 shows the example of pulse width modulation waveform.

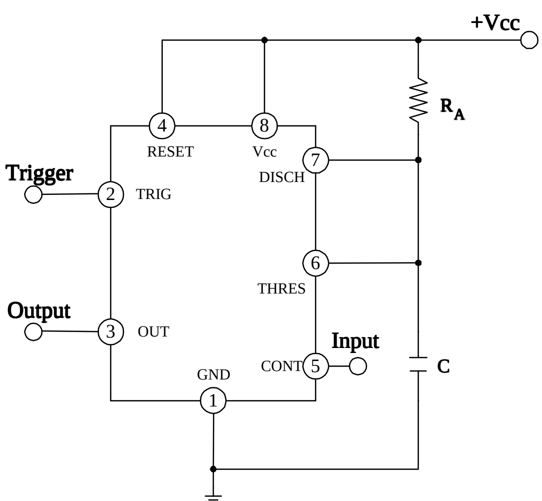
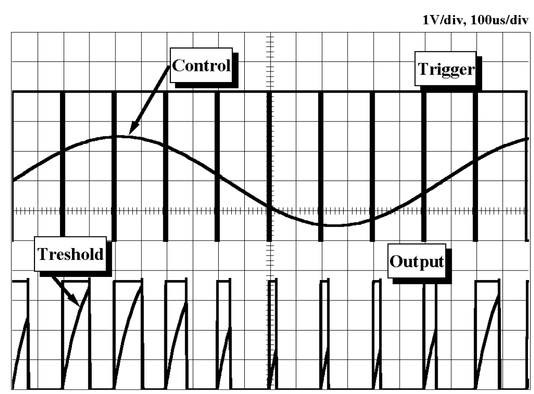


Figure 9. Circuit for Pulse Width Modulation



R_A=9.1kΩ, R_L=1kΩ, C1=0.01uF, Vcc=5V

Figure 10. Waveforms of Pulse Width Modulation

5. Pulse Position Modulation

If the modulating signal is applied to the control terminal while the timer is connected for the astable operation as in Figure 11, the timer becomes a pulse position modulator.
In the pulse position modulator, the reference of the timer's internal comparators is modulated which in turn modulates the timer output according to the modulation signal applied to the control terminal.
Figure 12 illustrates a sine wave for modulation signal and the resulting output pulse position modulation : however, any wave shape could be used.

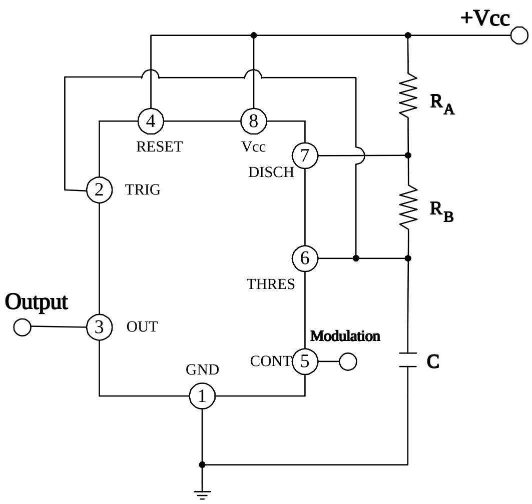


Figure 11. Circuit for Pulse Position Modulation

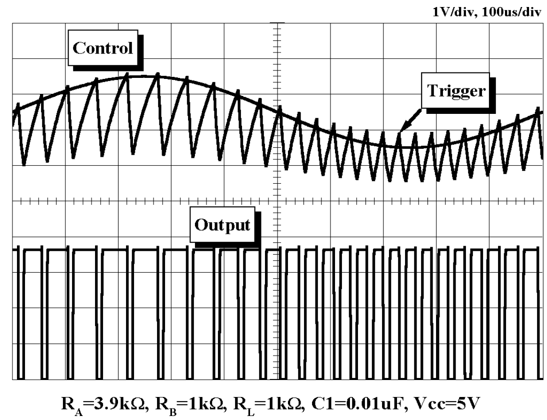


Figure 12. Waveforms of pulse position modulation

6. Linear Ramp

When the pull-up resistor RA in the monostable circuit shown in Figure 1 is replaced with constant current source, the V_{C1} increases linearly, generating a linear ramp. Figure 13 shows the linear ramp generating circuit and Figure 14 illustrates the generated linear ramp waveforms.

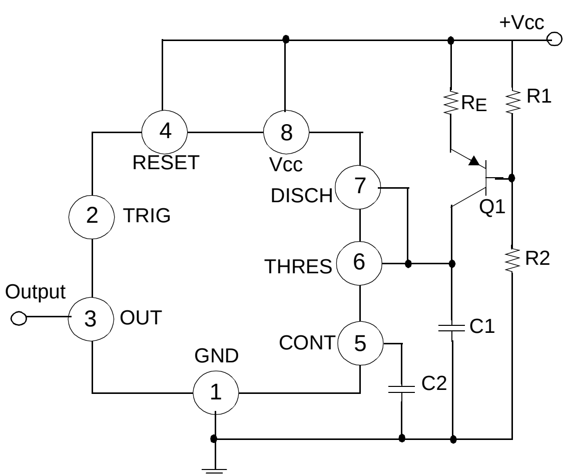


Figure 13. Circuit for Linear Ramp

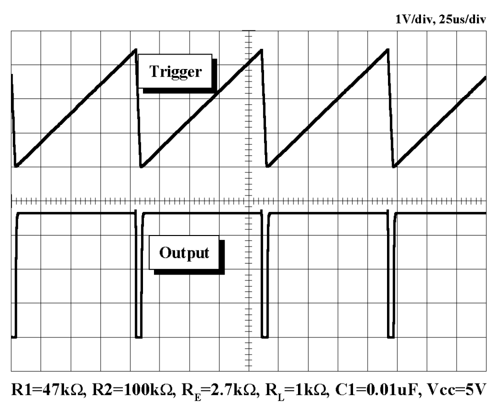


Figure 14. Waveforms of Linear Ramp

In Figure 13, current source is created by PNP transistor Q1 and resistor R1, R2, and R_E.

$$I_C = \frac{V_{CC} - V_E}{R_E} \qquad (12)$$

Here, V_E is

$$V_E = V_{BE} + \frac{R_2}{R_1 + R_2} V_{CC} \qquad (13)$$

For example, if Vcc=15V, R_E=20kΩ, R1=5kW, R2=10kΩ, and V_{BE}=0.7V,
V_E=0.7V+10V=10.7V
Ic=(15-10.7)/20k=0.215mA

When the trigger starts in a timer configured as shown in Figure 13, the current flowing through capacitor C1 becomes a constant current generated by PNP transistor and resistors.
Hence, the V_C is a linear ramp function as shown in Figure 14. The gradient S of the linear ramp function is defined as follows:

$$S = \frac{V_{p-p}}{T} \qquad (14)$$

Here the Vp-p is the peak-to-peak voltage.
If the electric charge amount accumulated in the capacitor is divided by the capacitance, the V_C comes out as follows:

$$V=Q/C \qquad (15)$$

The above equation divided on both sides by T gives us

$$\frac{V}{T} = \frac{Q/T}{C} \qquad (16)$$

and may be simplified into the following equation.

$$S=I/C \qquad (17)$$

In other words, the gradient of the linear ramp function appearing across the capacitor can be obtained by using the constant current flowing through the capacitor.
If the constant current flow through the capacitor is 0.215mA and the capacitance is 0.02µF, the gradient of the ramp function at both ends of the capacitor is S = 0.215m/0.022µ = 9.77V/ms.

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised July 2001

DM7404
Hex Inverting Gates

General Description

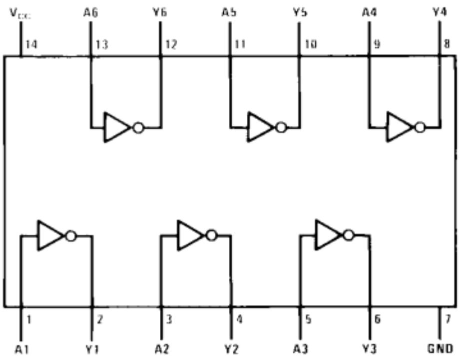
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram



Function Table

$Y = \overline{A}$

Inputs	Output
A	**Y**
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−18		−55	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		6	12	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		18	33	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			15	ns

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS08
Quad 2-Input AND Gates

General Description

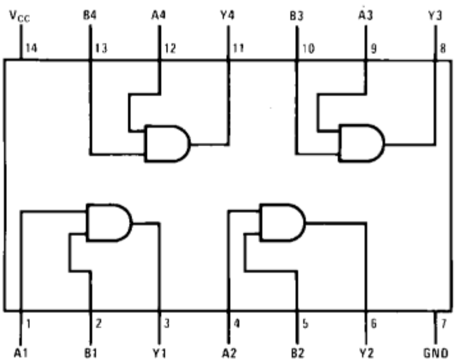
This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram



Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		2.4	4.8	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		4.4	8.8	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

FAIRCHILD
SEMICONDUCTOR™

June 1986
Revised March 2000

DM74LS32
Quad 2-Input OR Gate

General Description

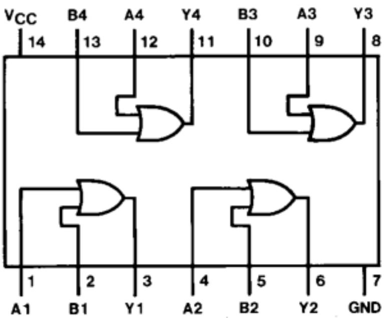
This device contains four independent gates each of which performs the logic OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS32N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Y = A + B

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		3.1	6.2	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		4.9	9.8	mA

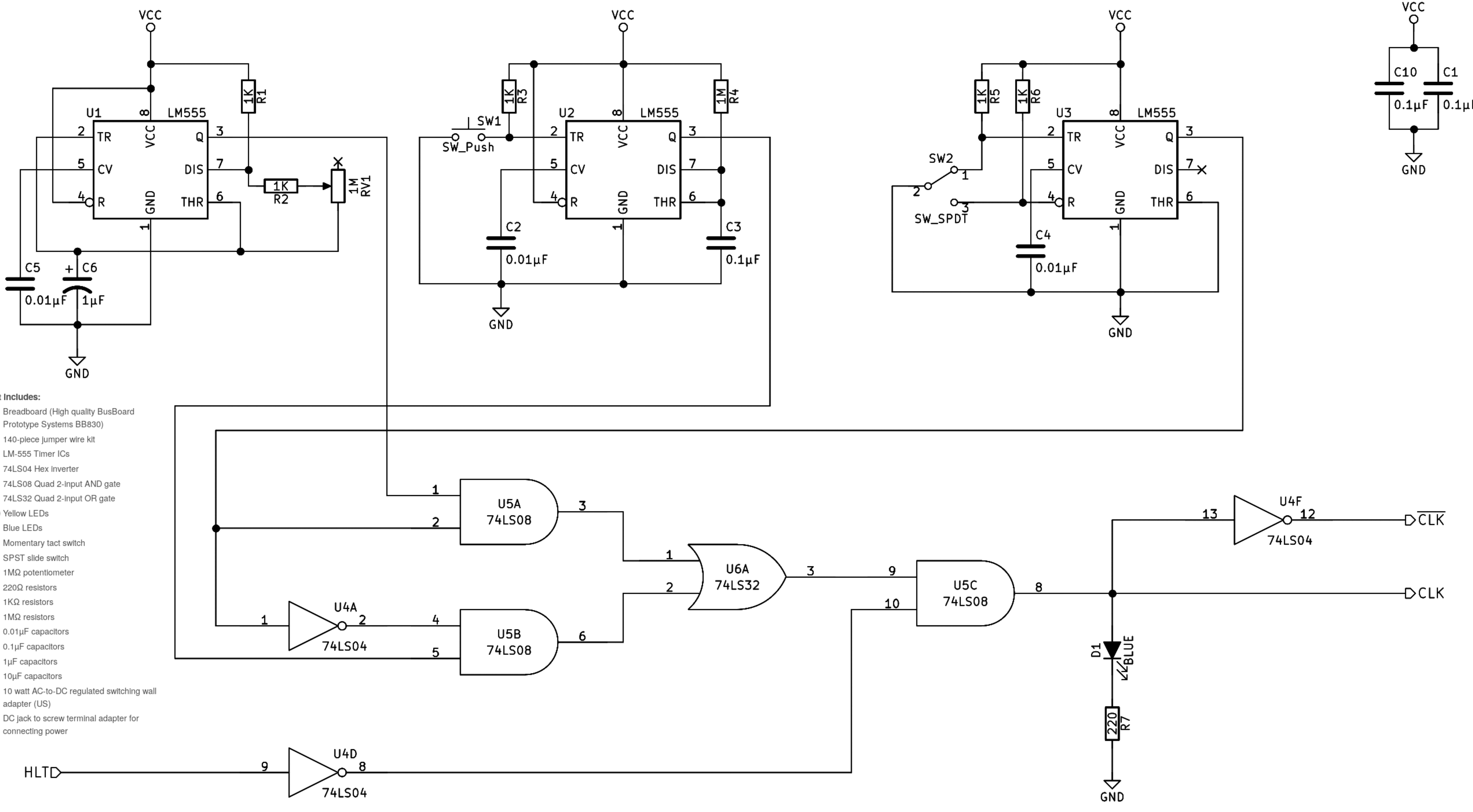
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns



Kit Includes:

1	Breadboard (High quality BusBoard Prototype Systems BB830)
1	140-piece jumper wire kit
3	LM-555 Timer ICs
1	74LS04 Hex inverter
1	74LS08 Quad 2-input AND gate
1	74LS32 Quad 2-input OR gate
10	Yellow LEDs
5	Blue LEDs
1	Momentary tact switch
1	SPST slide switch
1	1MΩ potentiometer
5	220Ω resistors
5	1KΩ resistors
5	1MΩ resistors
5	0.01µF capacitors
5	0.1µF capacitors
5	1µF capacitors
5	10µF capacitors
1	10 watt AC-to-DC regulated switching wall adapter (US)
1	DC jack to screw terminal adapter for connecting power