

HCMOS LS TTL

Figure 1 displays a 10x10 grid of 100 small circuit diagrams, each representing a 74HC337 and 74ALS337 decoder configuration. Each diagram shows the internal logic of the decoder, including inputs (EN, D0-D3, CLK), outputs (Q0-Q3), and the internal flip-flop (Flop) and NAND gates. The diagrams are arranged in a grid, with the first row labeled 74HC337 and 74ALS337, and the last row labeled 74HC337 and 74ALS337. The diagrams are numbered 1 through 100.

*ALTERNATE*

Figure 1 displays 30 histograms arranged in a 10x3 grid, showing the distribution of the number of nodes in the largest component of a network. The columns are labeled '74HC377', 'FLIP-FLOP', and '74LS377'. Each histogram has 'Nodes' on the x-axis (0 to 20) and 'Frequency' on the y-axis (0 to 15). The distributions are generally unimodal and centered around 10-12 nodes, with some variation in peak frequency and spread across the different components and iterations.