PIC16(L)F15313/23

PIC16(L)F15313/23 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F15313/23 family devices that you have received conform functionally to the current Device Data Sheet (DS40001897**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F15313/23 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F15313/23 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A2	A3	A4
PIC16F15313	30BEh	2002h	2003h	2004h
PIC16LF15313	30BFh	2002h	2003h	2004h
PIC16F15323	30C0h	2002h	2003h	2004h
PIC16LF15323	30C1h	2002h	2003h	2004h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F153XX Memory Programming Specification"* (DS40001838) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				A2	A3	A4
Electrical Specifications	SMBus 2.0	1.1	The maximum V_{IL} level changes when V_{DD} is below 4.0V at 125°C.	X	—	—
	Fixed Voltage Reference (FVR) Accuracy	1.2	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below –20°C.	X	X	X
	Nonvolatile Memory (NVM)	1.3	NVM Self-Writes on LF devices may not work properly at specified voltage levels and temperatures.	X	X	—
	Nonvolatile Memory (NVM) for LF Devices	1.4	NVM on LF devices may not work properly at specified voltage levels and temperatures.	X	X	X
Comparator	Input Pin	2.1	Negative Input Pin on RA4 is not functional.	X	—	—
I/O Port	SMBus 2.0	3.1	SMBus 2.0 levels are not functional on the default I^2C function pins for SCL and SDA.	X	—	—
	I^2C Driver	3.2	I^2C levels are not functional on the default I^2C function pins for SCL and SDA.	X	—	—
Nonvolatile Memory (NVM)	WRERR Bit Operation	4.1	WRERR Bit Operation	X	X	—
Windowed Watchdog Timer (WWDT)	Window Operation	5.1	The Window feature of the WWDT does not operate correctly in DOZE mode.	X	X	—
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	6.1	SSPBUF may become corrupted.	X	X	—
Digital-to-Analog (DAC)	Debug Mode	7.1	FVR as the Positive Voltage Source is not functional in Debug mode.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Electrical Specifications

1.1 SMBus 2.0 V_{IL} Level

At 125°C when the V_{DD} voltage level supplied to the device is 4.0V and above, the maximum SMBus 2.0 voltage level for the V_{IL} parameter is 0.8V. When V_{DD} drops below 4.0V, the maximum SMBus voltage level for V_{IL} drops to 0.7V. This issue applies to extended temperature devices only.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X							

1.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

1.3 Nonvolatile Memory (NVM)

Performing self-writes through NVMREG access, on LF version devices, and the following conditions listed below, may not work.

- V_{DD}<2.3V at temperatures between -40°C and <0°C.
- V_{DD}<2.1V at temperatures between ≥0°C and 25°C.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X						

1.4 Nonvolatile Memory (NVM) for LF Devices

Nonvolatile memory (NVM) access on LF devices may not work when operating at temperatures between -40°C and +25°C and V_{DD} levels below 2.0V. VDD_MIN for parameter (D002) is 2.0V for temperatures between -40°C and 25°C.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: Comparator

2.1 Input Pin

The negative input pin for the C1 Comparator, on RA4, is not functional on the PIC16(L)F15313 devices.

Work around

Use another negative input pin for the C1 comparator.

Affected Silicon Revisions

A2	A3	A4					
X							

3. Module: I/O Port

3.1 SMBus 2.0

The SMBus 2.0 signal levels are not available on the default I^2C function pins on PORTA for SCL and SDA on the PIC16(L)F15313. Standard ST and TTL levels are still available for these pins, which are configurable through the INLVLA register settings.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X							

3.2 I²C Drivers

The I²C signal levels are not available on the default I²C function pins on PORTA for SCL and SDA on the PIC16(L)F15313. Standard ST and TTL levels are still available for these pins, which are configurable through the INLVLA register settings.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X							

4. Module: Nonvolatile Memory (NVM)

4.1 WRERR Bit Operation

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again, regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X						

5. Module: Windowed Watchdog Timer (WWDT)

5.1 Window feature of the WWDT does not operate correctly in DOZE mode

When the Windowed mode of operation is enabled in DOZE mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

Method 1

Use the Windowed mode of operation in any other mode than DOZE. If disabling the DOZE mode is not an option, use the WWDT module without the window being enabled.

Method 2

If the device is in DOZE mode, perform the arming process for the window in NORMAL mode, and return to the DOZE mode.

Method 3

If there is an ISR in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A2	A3	A4					
X	X						

6. Module: Master Synchronous Serial Port (MSSP)

6.1 SSPBUF may become corrupted

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit shift register may become corrupted. The transmitted slave byte cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

Work around

Method 1 (Interrupt based using $\overline{SS}$): Connect the SS line to both the SS input and either an INT or IOC input pin.

1. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS}$ == 0 when the interrupt occurs).

2. Load SSPBUF with the data to be transmitted.

3. Continue program execution.

4. When the Interrupt Service Routine (ISR) is invoked, do either of the following:

a. Add a delay that ensures the first SCK clock will be complete, or

b. Poll SSPSTAT.BF (while (BF == 0)) and wait for the transmission/reception to complete.

Once either of these are complete, it is safe to return to program execution.

Method 2 (Bit polling based using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.

2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active ($\overline{SS}$(!PORTx.$\overline{SS}$ == 0)).

3. When $\overline{SS}$ is active ($\overline{SS}$ == 0), do either of the following:

a. Add a delay that ensures the first SCK clock will be complete, or

b. Poll SSPSTAT.BF (while (BF == 0)), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ not available):

1. Load SSPBUF with the data to be transmitted.

2. Poll SSPSTAT.BF (while (BF == 0)), and wait for the transmission/reception to complete**.**

Affected Silicon Revisions

A2	A3	A4					
X	X						

7. Module: Digital-to-Analog (DAC)

7.1 FVR as the positive voltage source in Debug mode

When using the DAC module while in Debug mode, and selecting the FVR as the positive voltage source, DAC1PSS = 10, the DAC is not functional and unexpected results can be seen on the output.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001897**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

1.1 Table 37-14: Comparator Specifications

The max. for Parameter CM01 is incorrect. The correct spec. number is ±60 as shown below.

TABLE 37-14: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)
V_{DD} = 3.0V, T_A = 25°C

Param. No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
CM01	V_{IOFF}	Input Offset Voltage	—	—	**±60**	mV	$V_{ICM} = V_{DD}/2$
CM02	V_{ICM}	Input Common Mode Range	GND	—	V_{DD}	V	
CM03	CMRR	Common Mode Input Rejection Ratio	—	50	—	dB	
CM04	V_{HYST}	Comparator Hysteresis	15	25	35	mV	
CM05	T_{RESP}(1)	Response Time, Rising Edge	—	300	600	ns	
		Response Time, Falling Edge	—	220	500	ns	
CMOS6	T_{MCV2VO}(2)	Mode Change to Valid Output	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at $V_{DD}/2$, while the other input transitions from V_{SS} to V_{DD}.

2: A mode change includes changing any of the control register values, including module enable.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev C Document (01/2019)

Added Affected Silicon Revision A4. Added Modules 1.4, 4, 5, 6, and 7. Other minor corrections.

Data Sheet Clarifications:

Added Module 1: Electrical Specifications; Correction to Table 37-14.

Rev B Document (8/2017)

Added Affected Silicon Revision A3. Other minor corrections.

Rev A Document (4/2017)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

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ISBN: 978-1-5224-4078-9

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