

1. Description

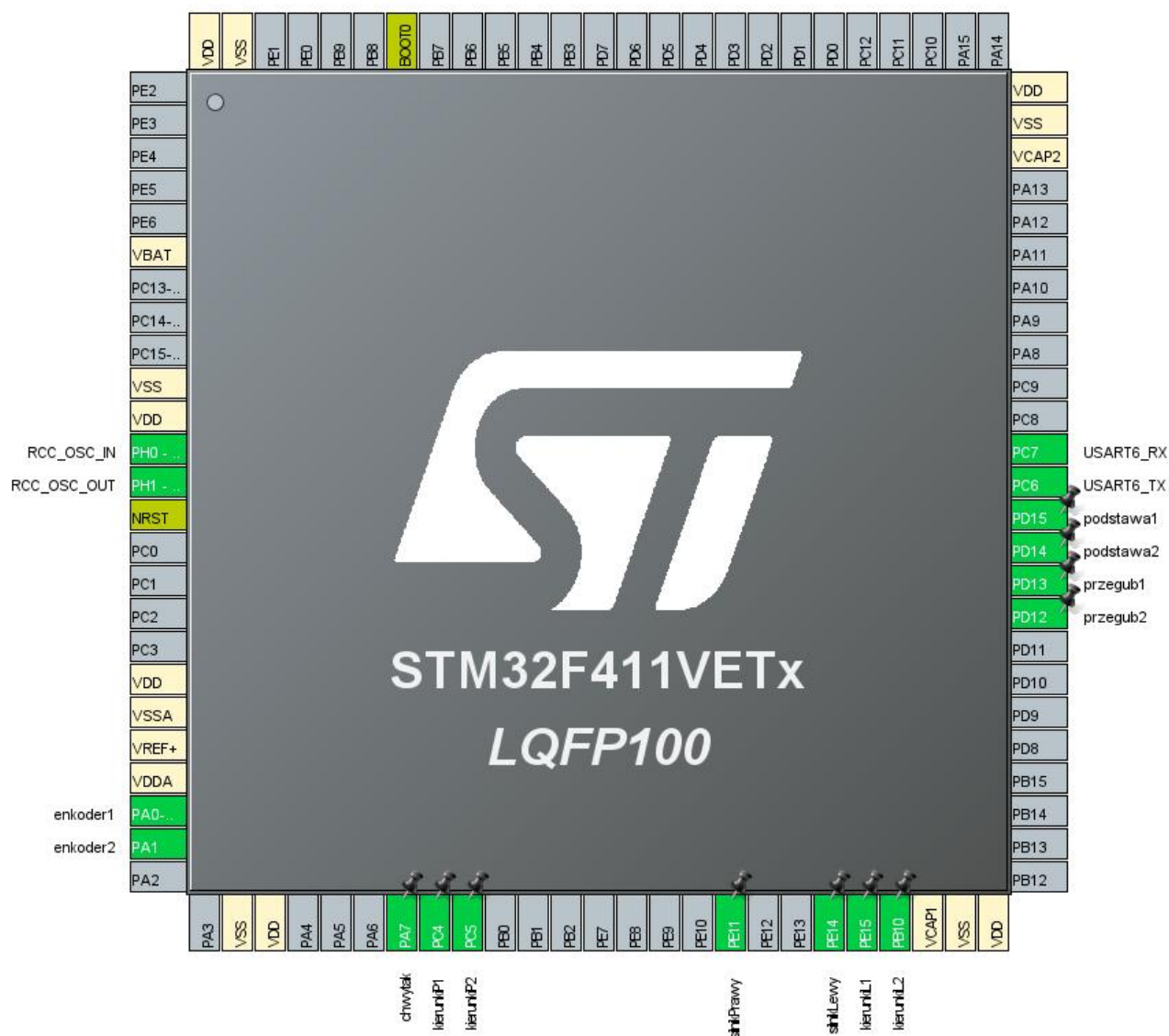
1.1. Project

Project Name	testserwa
Board Name	custom
Generated with:	STM32CubeMX 5.6.0
Date	05/07/2020

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411VETx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration

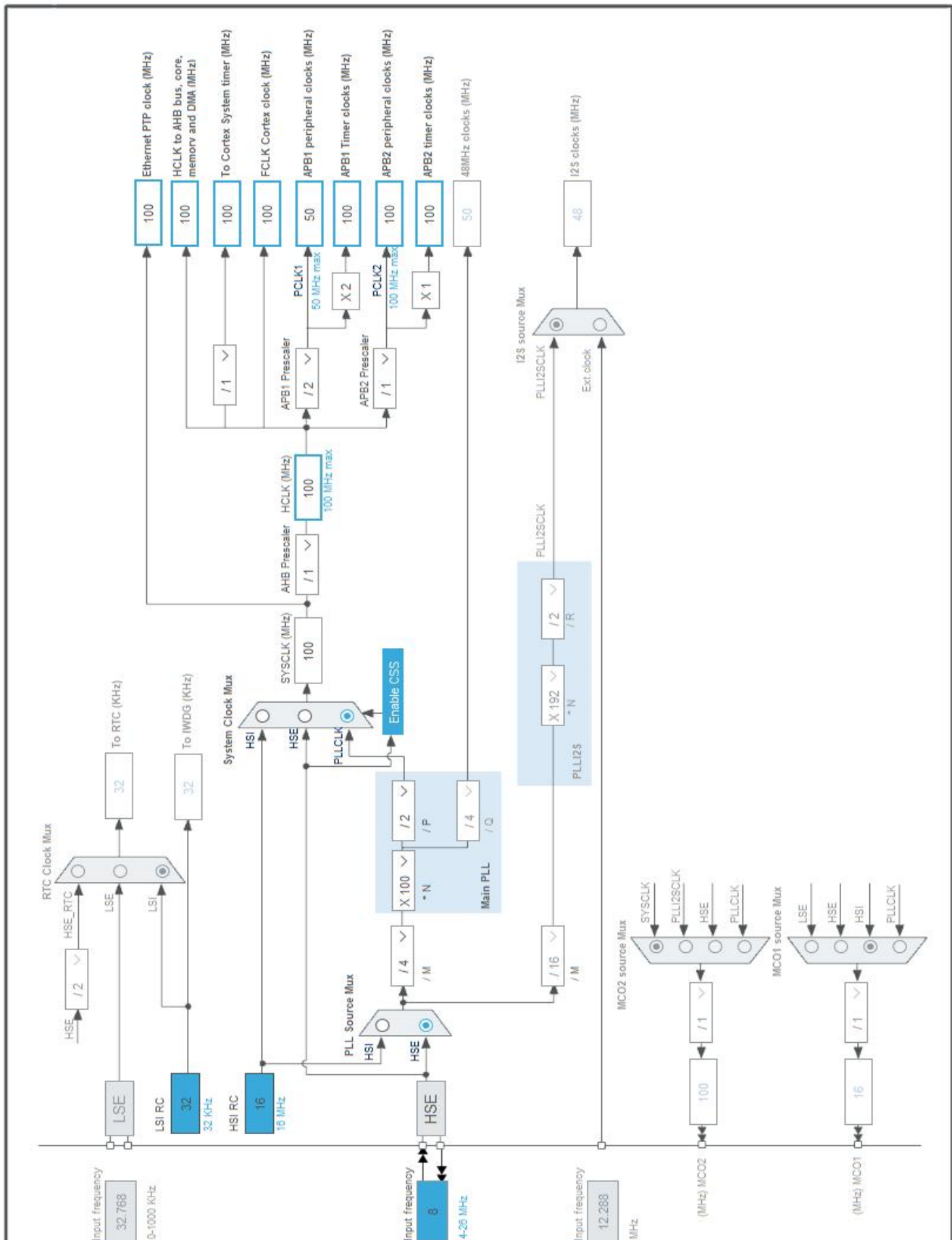


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0 - OSC_IN	I/O	RCC_OSC_IN	
13	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	enkoder1
24	PA1	I/O	TIM5_CH2	enkoder2
27	VSS	Power		
28	VDD	Power		
32	PA7	I/O	TIM3_CH2	chwytak
33	PC4 *	I/O	GPIO_Output	kierunkiP1
34	PC5 *	I/O	GPIO_Output	kierunkiP2
42	PE11	I/O	TIM1_CH2	silnikPrawy
45	PE14	I/O	TIM1_CH4	silnikLewy
46	PE15 *	I/O	GPIO_Output	kierunkiL1
47	PB10 *	I/O	GPIO_Output	kierunkiL2
48	VCAP1	Power		
49	VSS	Power		
50	VDD	Power		
59	PD12	I/O	TIM4_CH1	przegub2
60	PD13	I/O	TIM4_CH2	przegub1
61	PD14	I/O	TIM4_CH3	podstawa2
62	PD15	I/O	TIM4_CH4	podstawa1
63	PC6	I/O	USART6_TX	
64	PC7	I/O	USART6_RX	
73	VCAP2	Power		
74	VSS	Power		
75	VDD	Power		
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	testserwa
Project Folder	F:\STM\workspace_1.3.0\testserwa
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411VETx
Datasheet	026289_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

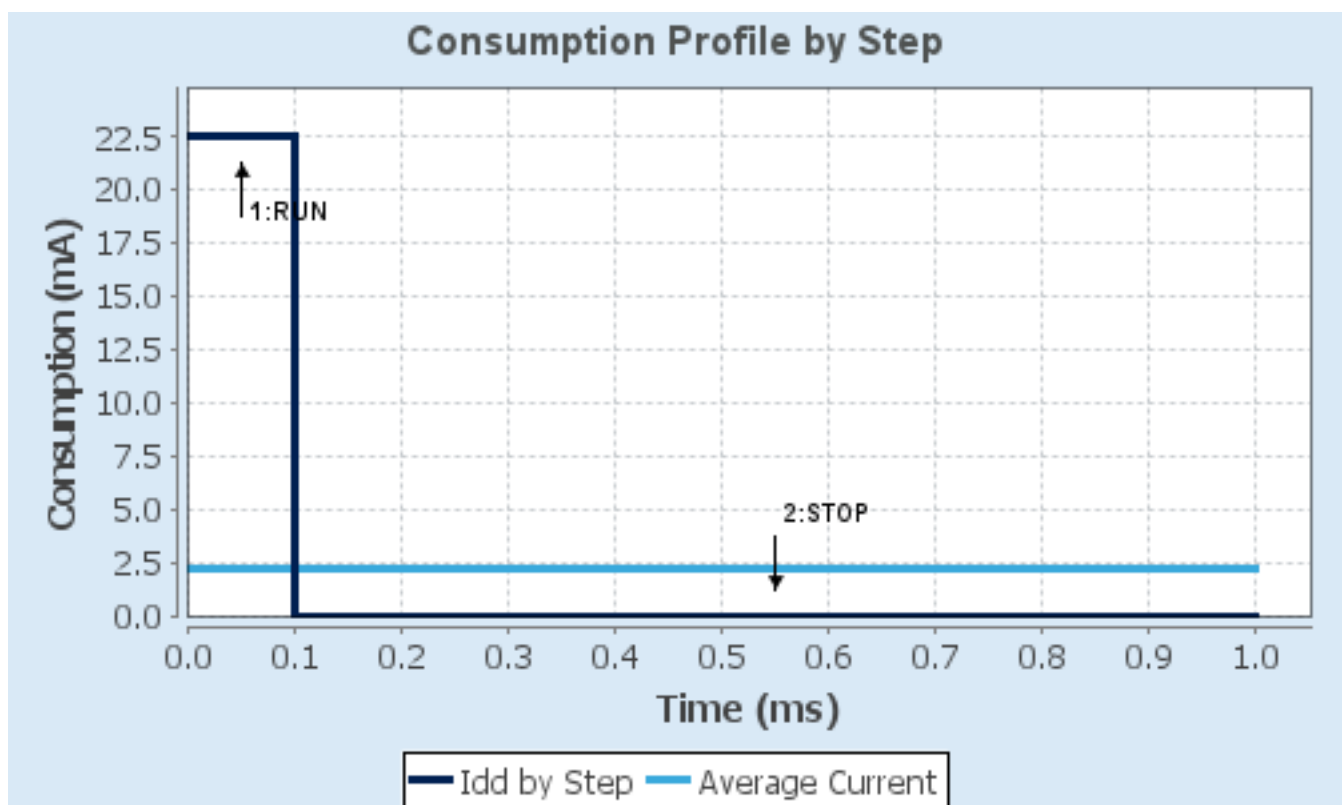
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH/ART/PREFETCH	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	22.5 mA	10 μ A
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	101.52	105
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	2.26 mA
Battery Life	2 months, 1 day, 18 hours	Average DMIPS	125.0 DMIPS

6.6. Chart



7. IPs and Middleware Configuration

7.1. GPIO

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.3. SYS

Timebase Source: SysTick

7.4. TIM1

Channel2: PWM Generation CH2

Channel4: PWM Generation CH4

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	9999 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	99 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.5. TIM2

Clock Source : Internal Clock

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	3999 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.6. TIM3

Channel2: PWM Generation CH2

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1999 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.7. TIM4

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1999 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
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Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM5

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	14000 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode

____ Parameters for Channel 1 ____

Polarity

IC Selection

Prescaler Division Ratio

Input Filter

____ Parameters for Channel 2 ____

Polarity

IC Selection

Prescaler Division Ratio

Input Filter

Encoder Mode TI1 and TI2 *

Rising Edge

Direct

No division

15 *

Rising Edge

Direct

No division

15 *

7.9. TIM9

mode: Clock Source

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

500 *

Counter Mode

Up

Counter Period (AutoReload Register - 16 bits value)

99 *

Internal Clock Division (CKD)

No Division

auto-reload preload

Disable

7.10. USART6

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate

115200

Word Length

8 Bits (including Parity)

Parity

None

Stop Bits

1

Advanced Parameters:

Data Direction

Receive and Transmit

Over Sampling

16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
TIM1	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	silnikPrawy
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	silnikLewy
TIM3	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	chwytak
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	przegub2
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	przegub1
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	podstawa2
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	podstawa1
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	enkoder1
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	enkoder2
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	kierunkiP1
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	kierunkiP2
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	kierunkiL1
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	kierunkiL2

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 break interrupt and TIM9 global interrupt	true	0	0
TIM2 global interrupt	true	0	0
USART6 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		

* User modified value

9. Predefined Views - Category view : Current

Middleware

System Core

Analog


Timers

Connectivity

Multimedia


Computing

DMA

GPIO 


NVIC 

RCC 

SYS 

TIM1 

TIM2 

TIM3 

TIM4 

TIM5 

TIM9 

USART6 

10. Software Pack Report