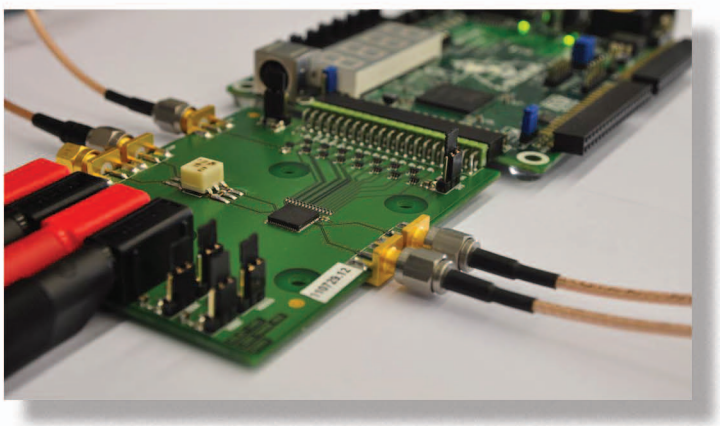
Pieter Harpe

Successive-approximation register analog-to-digital converters (SAR ADCs) have been around for a long time, but they have recently received a lot of attention due to the advantages of process scaling and recent architectural innovations, leading to improvements in power efficiency and conversion speed. For illustration, Figure 1 shows a collection of data converters in terms of energy per conversion (which is the power consumption P divided by the sampling rate f_s) and accuracy, expressed as signal-to-noise-and-distortion ratio (SNDR), based on data from [1]. As one can see, SAR ADCs are very power efficient compared to other

Successive Approximation Analog-to-Digital Converters

Improving power efficiency and conversion speed



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architectures for medium accuracies between 40 and 70 dB of SNDR. In terms of speed, SAR ADCs have managed to reach sampling rates of up to 90 GS/s when time interleaved [2]. One of the reasons SAR ADCs are doing so well is because they use simple analog and digital circuits that tend to scale well and benefit from newer process technologies. Moreover, the simple structure often allows operation at reduced supply levels, which can save additional power. In this article, we will discuss the basic design aspects of SAR ADCs and give a short overview of state-of-the-art designs and future trends.

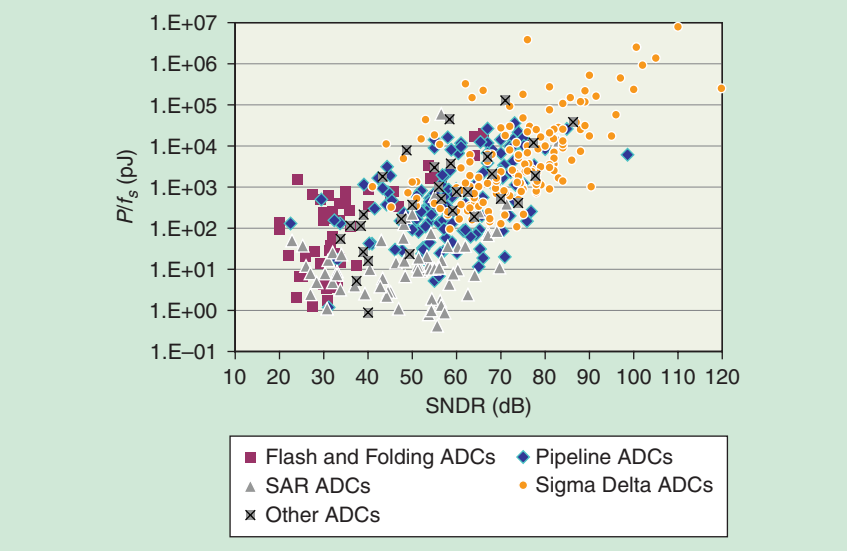

FIGURE 1: An ADC performance benchmark, energy per conversion versus SNDR.

Basic Operation

An SAR ADC implements a binary search algorithm to find the digital code that bests represents the analog input. This algorithm requires exactly N steps to find an N-b digital code. An example for a 3-b ADC is shown in Figure 2, where a given analog input voltage (V_{in}) is translated to an output code given a full-scale signal range between −1 and +1 V. In the first step, the unknown V_{in} is compared to a reference V_{ref} that is initially set to the middle of the range (i.e., 0 V in this example). As shown in the figure, $V_{in} < V_{ref}$, so the first bit is resolved as 0, and the reference is now shifted to the middle of the remaining search range. Since we know that V_{in} must be between −1 and 0 V, the new reference is thus set to −0.5 V. In the next cycle, $V_{in} > V_{ref}$, so the second resolved bit becomes 1; and, therefore, the reference voltage is now updated to −0.25 V. A last comparison resolves the third bit, which is 0, thus resulting in the final digital code 010.

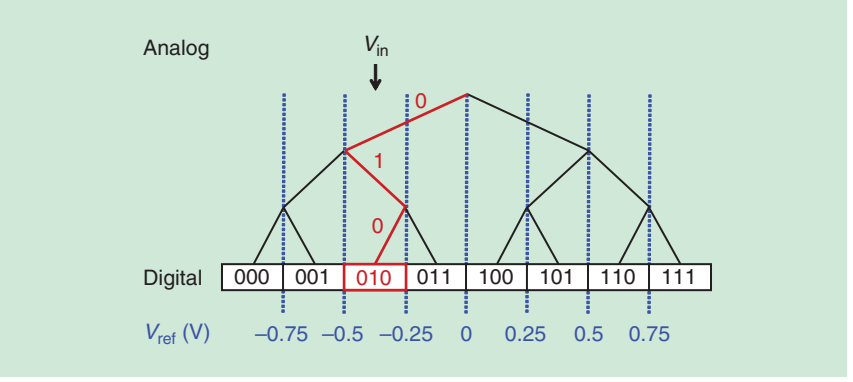

FIGURE 2: A binary search tree of a 3-b SAR ADC.

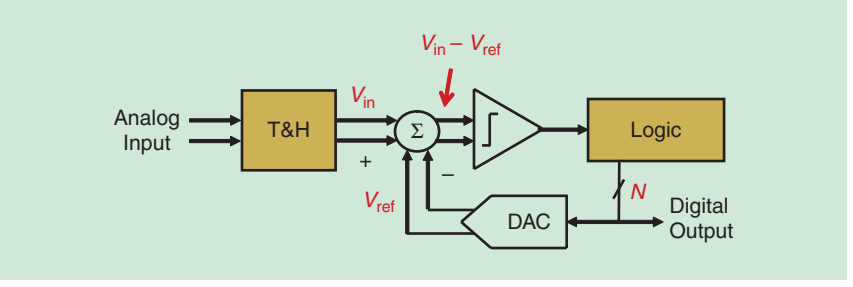

FIGURE 3: A block diagram of a differential SAR ADC.

As one can see, the algorithm requires three components. First, a digital-to-analog converter (DAC) is required to generate a reference voltage V_{ref} that is updated depending on the bit decisions. Second, a comparator is required to compare V_{in} to V_{ref}. Finally, logic is required to time the various operations and to store the actually obtained digital code. In addition, a track and hold (T&H) is also required to sample and hold the analog input voltage prior to performing the binary search method.

Figure 3 shows a block diagram of an N-b SAR ADC. In this case, rather than comparing V_{in} against V_{ref}, V_{ref} is subtracted from V_{in} first, and the comparator simply determines the sign of $V_{in} - V_{ref}$, which is identical to comparing V_{in} against V_{ref}. As we will see later, the T&H is nothing more than a set of switches, and the DAC is usually composed of a switched-capacitor network, leading to a simple hardware implementation.

A simplified timing diagram of an SAR ADC is shown in Figure 4. After sampling the input, the digital bits 1–N are decided one by one. A clock at the sample rate (f_s) controls the T&H

SAR ADCs are very power efficient compared to other architectures for medium accuracies between 40 and 70 dB of SNDR.

switches. A higher clock frequency (f_{clk}) is usually required such that for each of the N cycles of the SAR algorithm, distinctive clock phases are available to time the DAC, comparator, and logic activities. Hence, f_{clk} is usually at least N+1 times higher than the sample rate f_s.

T&H

Essentially, the function of a T&H circuit is to sample and hold the analog input signal onto a capacitor such that it can be quantized by the SAR ADC afterward. Figure 5 shows a single-ended T&H composed of a sampling switch and a sampling capacitance C_s. In reality, a differential circuit can be made by making two copies of this design. Further, capacitance C_s is often composed of the DAC capacitors rather than an explicit additional sampling capacitance. As shown in the figure, as long as the clock signal (CLK) is high (Vdd), V_{out} tracks the input V_{in}. As soon as CLK becomes low, the input is sampled and V_{out} is held on C_s. The major limitation of an n-channel metal–oxide–semiconductor (NMOS)-only switch is that it can only conduct when V_{in} is well below Vdd – V_{tn} (i.e., where V_{tn} is the NMOS threshold voltage), which does not allow a rail-to-rail input signal.

A potential, simple solution is the use of a complimentary metal–oxide–semiconductor (CMOS) switch (Figure 6). In this case, an NMOS and a p-channel MOS (PMOS) device are used in parallel. As shown in Figure 6, this could theoretically lead to a switch with a rail-to-rail conductivity. However, this is only feasible when Vdd $\gg V_{tp} + V_{tn}$. If this condition is not met, the switch will not conduct for signals in the middle of the range. For advanced CMOS nodes, this requirement can become difficult to satisfy as the supply levels tend to scale more rapidly than the threshold voltages.

To overcome these limitations, a common solution is to use an NMOS-only switch (as in Figure 5), where the gate voltage is increased beyond Vdd during tracking to allow better conduction of the switch. With clock boosting [3], the gate is elevated to a fixed higher value, e.g., 2×Vdd, allowing a rail-to-rail input range and a far better overdrive voltage that gives more bandwidth and linearity. However, the elevated voltage could result in violating the safe voltage levels of the NMOS. An alternative is bootstrapping [4], where the gate is elevated to an input-dependent voltage Vdd + V_{in}, which ensures that the V_{gs} of the NMOS is constant and equal to Vdd. This assures safe operation of the NMOS within its voltage limits and, moreover, enhances

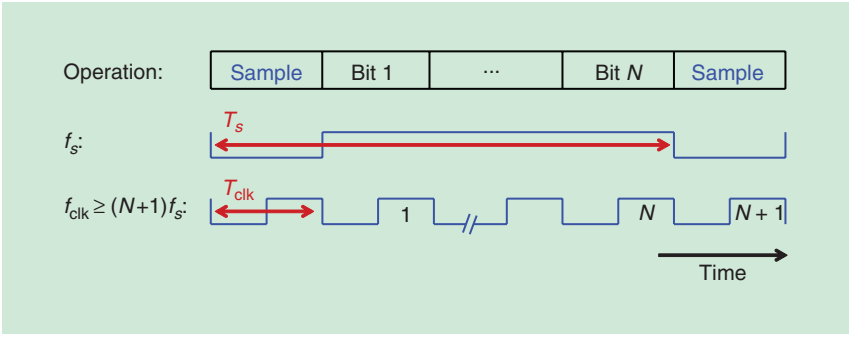

FIGURE 4: A timing diagram of an SAR ADC.

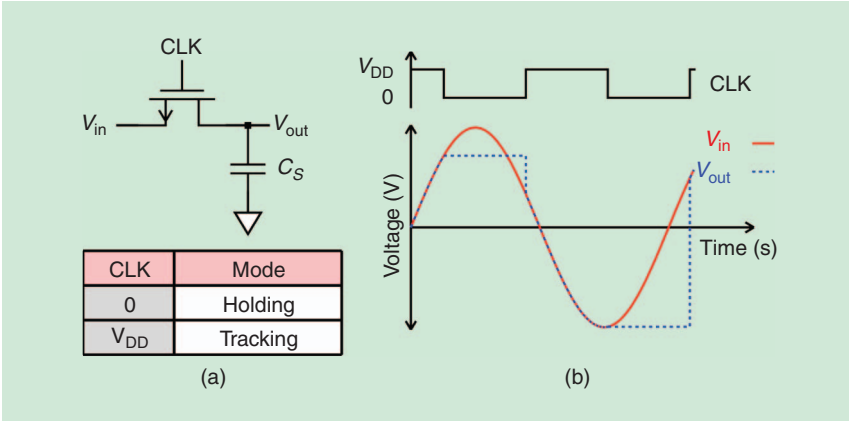

FIGURE 5: A T&H circuit with an NMOS sampling switch.

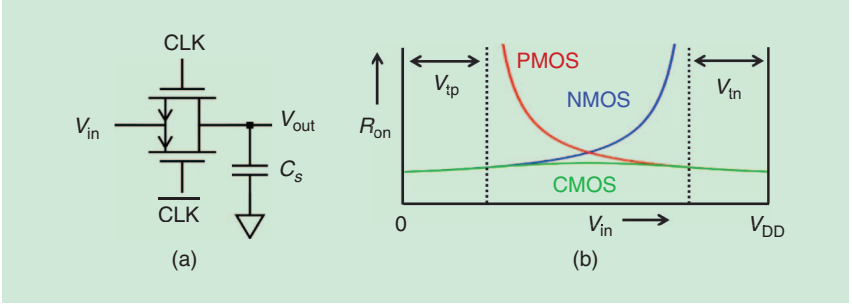

FIGURE 6: A T&H circuit with a CMOS sampling switch.

linearity by making the overdrive voltage signal independent.

Having described the basic switch implementations, we now discuss the most important imperfections of the T&H. In the tracking phase, the on-resistance is a critical imperfection. At the sampling instant (i.e., when CLK goes from high to low), the charge injection, sampling noise, and jitter/time-skew are introduced. Finally, during the hold mode, leakage and capacitive coupling can deteriorate the sampled value.

As an example, the on-resistance of an NMOS switch is given by (1), and the on-resistance of an NMOS, PMOS, and CMOS switch is shown in Figure 6. As can be seen from (1), the on-resistance can be reduced by increasing W/L, by increasing the CLK voltage (e.g., using boosting or bootstrapping), or by using low-threshold voltage transistors. In practice, the on-resistance results in two T&H limitations. First of all, R_{on} in combination with C_s results in a low-pass filter, thus limiting the bandwidth of the system. Secondly, since R_{on} is dependent on the input signal V_{in} (unless bootstrapping is used), the resistance results in the distortion of the signal. However, this distortion only becomes significant when the input signal is nearing the bandwidth of the $R_{on}C_s$ filter, which implies that the distortion is frequency dependent.

$$R_{on} = \frac{1}{\mu_n c_{ox} \frac{W}{L}(V_{CLK} - V_{in} - V_{tn})}. \quad (1)$$

At the sampling moment, a second form of distortion can occur due to charge injection, i.e., as soon as the switch is turned off, the charge Q_{ch} in the channel needs to get out. Assuming the charge is spread equally to input and output nodes, a voltage step at the output is caused that, for an NMOS switch, is equal to

$$\Delta V_{out} = \frac{Q_{ch}}{2c_s} = \frac{c_{ox}WL(V_{CLK} - V_{in} - V_{tn})}{2c_s}. \quad (2)$$

The charge injection causes offset and gain errors, which often can be ignored, and are partially compensated in a differential T&H. However, as this error voltage is signal dependent, it can also cause distortion in reality. Since this contribution does not depend on the frequency of V_{in}, it appears as a frequency independent distortion. Reducing the area WL helps to decrease the impact of charge injection. Another common solution is the use of dummies that compensate charge injection or the use of bottom-plate sampling that removes the signal dependency from (2).

When combining multiple SAR ADCs in a time-interleaved structure, variations of time skew in the various sub-ADCs will lead to distortion for the overall ADC.

As an example, Figure 7 shows the simulated linearity of a differential T&H with NMOS switches. The T&H operates at 10 MS/s and has a sampling capacitance of 1 pF. The linearity, in terms of spurious-free dynamic range (SFDR), is plotted as a function of the input signal frequency. At lower frequencies, the distortion is dominated by the charge injection, which explains why the SFDR remains constant here. For higher frequencies, the distortion due to on-resistance becomes more relevant, causing the SFDR to gradually drop as a function of frequency. We can further observe that a wider switch reduces low-frequency linearity as it increases the charge injection. However, at the same time, this will improve the high-frequency linearity as it reduces the on-resistance. Therefore, the W/L selection is clearly a tradeoff between low- and high-frequency linearity.

A second imperfection occurring at the sampling moment is the introduction of sampling noise. Besides sampling the input signal, the thermal noise originating from the switch is also sampled on C_s, having a total noise power equal to kT/C_s. When a differential topology is used, this term is occurring twice, leading to a total noise contribution of $2kT/C_s$, where C_s is the capacitance of each side of the differential topology. In this case, the only remedy is the proper sizing of C_s. Another solution, since one usually cares about the signal-to-noise ratio (SNR), is to maximize the signal swing by making it rail to rail or by increasing the supply voltage.

The third issue taking place at the sampling instant is the variation in the clock timing. As shown in Figure 8, when the clock signal is an amount of Δt_{clk} from the nominal moment, the sampled output voltage V_{out} will have an error ΔV_{out} that is proportional to both Δt_{clk} and the derivative of the input signal being sampled. Thus, this error is especially critical for ADCs with

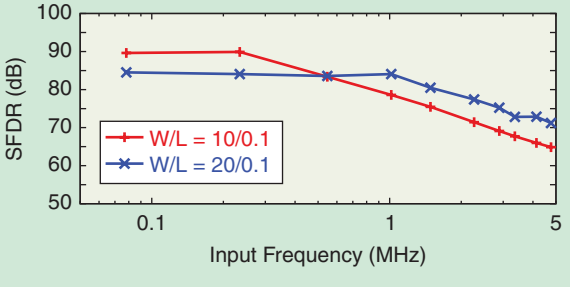

FIGURE 7: A T&H linearity as a function of the input frequency.

Mismatch tends to be one of the biggest concerns in DAC design, and often limits the linearity that can be achieved with an SAR ADC.

high-frequency input signals. When Δt_{clk} shows a random (noise-like) behavior, it is called *jitter* and will introduce noise at the output. When Δt_{clk} is constant, this effect is called *time skew*. When combining multiple SAR ADCs in a time-interleaved structure, variations of time skew in the various sub-ADCs will lead to distortion for the overall ADC.

Finally, the T&H can also have imperfections during the hold mode, in which the output node should ideally be isolated from the input signal. However, in modern CMOS nodes in particular, this is not the case. First of all, transistors can show leakage, which implies that there is a resistive path from the drain to the source of the transistor that connects V_{in} to V_{out}, even when the transistor is supposed to be turned off. A second issue is the capacitive coupling from drain to source due to C_{ds} capacitance, either from the intrinsic transistor or from the metal interconnections. The result of both of these problems is that V_{out} could be disrupted by the input signal, which can lead to faults in the quantization process. Both these problems tend to become more critical in scaled technologies as leakages tend to increase, and capacitive coupling could increase due to reduced dimensions. Minimizing W/L helps to reduce both leakage and capacitive coupling. Otherwise, using a higher threshold voltage device helps to reduce leakage, and layout techniques could be used to reduce or cancel capacitive coupling.

Overall, the T&H can encounter a variety of problems, while the solutions are sometimes in contradiction with each other. As a result, the design in terms of topology and transistor sizing will be a compromise to balance the various issues.

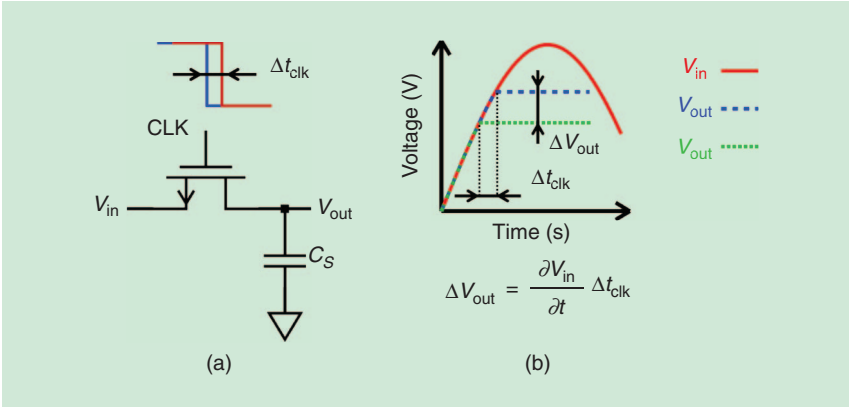

FIGURE 8: The effect of jitter and time skew.

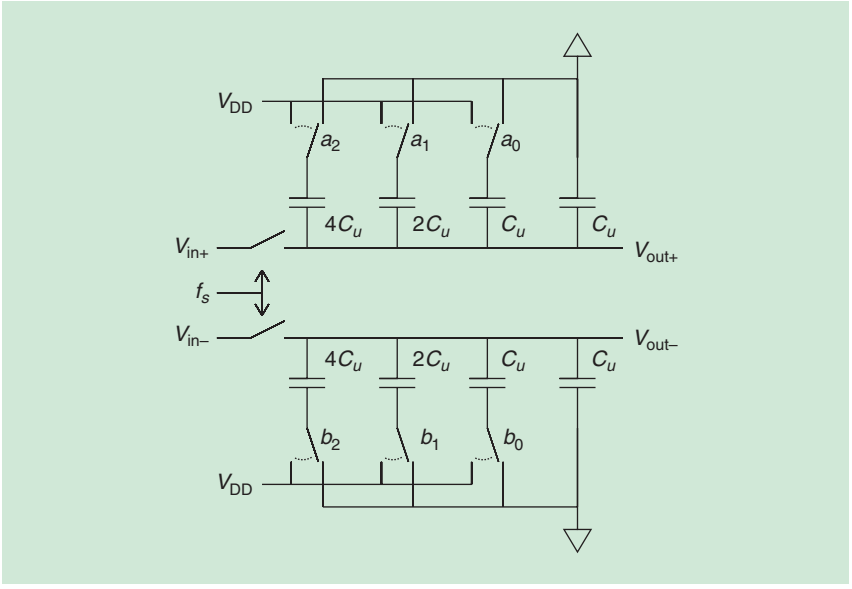

FIGURE 9: A 3-b differential switched-capacitor DAC including T&H.

DAC

The DAC inside an SAR ADC is usually implemented as a switched-capacitor network. While there are many variations, an example using a charge redistribution DAC with monotonic switching will be illustrated in this article [5]. Figure 9 shows an example of such a DAC with 3 b of resolution. The differential topology has a set of binary scaled capacitors with a unit value of C_u. The sampling switches on the left side, controlled by a clock f_s, implement the T&H described previously. First, it will sample the input voltage (V_{in+}, V_{in-}) onto the top plates of all the capacitors. The total capacitance C_s as seen by the sampling switches is $8C_u$ per side. At the moment of sampling, all of the switches controlled by the digital signals $a_{2\text{-}0}$, b_{2-0} are connected to ground. The output (V_{out+}, V_{out-}) is directly connected to the comparator.

As an example, assume Vdd = 1 V, V_{in+} = 0.6 V, and V_{in-} = 0.4 V; thus, the differential input voltage is 0.2 V. After sampling the input voltage at the output nodes, the SAR algorithm initiates. First, a comparison

is performed. Since $V_{out+} > V_{out-}$, the first decision resolves a 1, and bit b_2 will be switched to Vdd to minimize the difference between V_{out+} and V_{out-}. When b_2 is switched from ground to Vdd, the charge redistribution will increase V_{out-} with an amount of $4C_u/C_s \cdot \text{Vdd} = 0.5$ V, giving a new voltage V_{out-} of 0.9 V while V_{out+} remains unchanged. Now $V_{out-} > V_{out+}$, thus the next comparison resolves a 0, and a_1 will be switched to Vdd. This increases V_{out+} by 0.25, giving a new voltage of 0.85 V. Now, it still holds that $V_{out-} > V_{out+}$, so the third comparison again resolves a 0, and a_0 will be switched to Vdd, increasing V_{out+} by 0.125 V, giving a new voltage of 0.975 V. Now, $V_{out+} > V_{out-}$, thus a fourth comparison yields 1, hence the final output code is 1001. Note that, with the monotonic switching scheme, the final ADC resolution can be one bit higher (4 b) than the DAC resolution (3 b).

The monotonic switching scheme is just one example. There are many other ways of implementing the switched-capacitor network. In each case, the ADC can perform the same binary search algorithm but, by smartly switching the capacitors, using multiple reference voltages, or reusing charge, the power consumption of the DAC can be reduced. A few recent examples are the split capacitor switching method [6], merged capacitor switching [7], charge average switching [8], and detect and skip with aligned switching [9]. While these schemes can save significant DAC power, one should also be aware that they may introduce some additional logic overhead, require additional references, and might impact other characteristics such as noise or linearity.

For DAC design, the three main concerns are noise, speed, and mismatch. Noise is introduced at the moment the T&H samples the input on the array of capacitors. Additional noise will also be present due to the on-resistance of the control switches ($a_{2\text{-}0}$, $b_{2\text{-}0}$ in Figure 9). Moreover, the supply Vdd that is used as a reference voltage for the DAC may also couple noise into the system.

For DAC design, the three main concerns are noise, speed, and mismatch.

With respect to speed, each time one of the switches in the DAC is switched, the DAC forms a resistor-capacitor (RC) network causing the output to settle (exponentially) to the new level. Therefore, to have a correct comparison in the next SAR cycle, this RC time limits the maximum speed of operation. To increase the speed, either the capacitors could be reduced or the switches need to be enlarged to reduce their on-resistance.

Mismatch tends to be one of the biggest concerns in DAC design and often limits the linearity that can be achieved with an SAR ADC. Note that the capacitors in the DAC are ideally binary scaled (Figure 9), which ensures that the generated reference levels of the DAC will compose a perfect binary search tree (Figure 2). However, when the capacitors have random or systematic variations, causing the values to be nonbinary scaled, the search tree will not be ideal anymore. An example of this is given in Figure 10. In this case, the capacitor that generates voltage step s has a mismatch. As a result, not only this reference but also the references of the subbranch of this tree will be shifted with an amount equal to the error of this capacitor. Moreover, because of the reuse of hardware in an SAR ADC, the same capacitor will also be used to generate voltage step s'. Therefore, the same error pattern will repeat twice in the transfer curve of this ADC (in this particular example). This type of repetitive patterns is typical for capacitor mismatch errors in SAR ADCs. An example of a chip measurement with severe mismatch errors is shown in Figure 11, where the integral nonlinearity (INL) shows a clear pattern (more or less a square wave) caused by capacitor mismatch [10].

Overall, the selection of the value of the total DAC capacitance

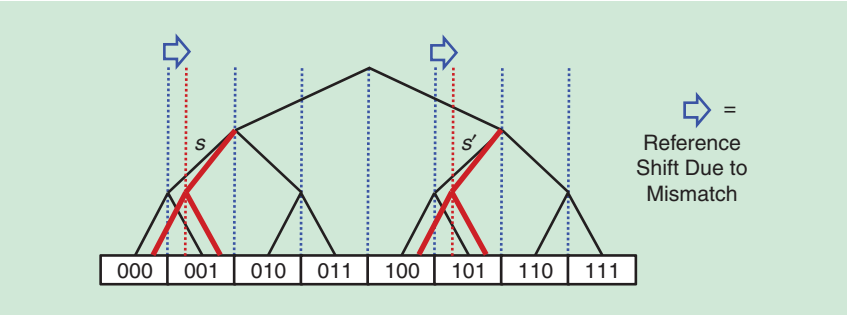

FIGURE 10: The effect of capacitor mismatch on the search tree.

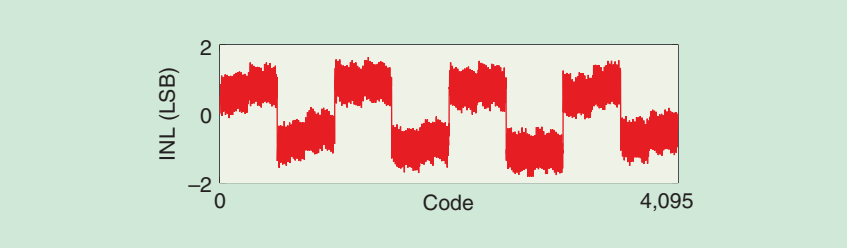

FIGURE 11: A measured INL for a 12-b SAR ADC with substantial capacitor mismatch.

When looking at power consumption, we should realize that the SAR ADC has both analog and digital blocks.

C_s is a tradeoff, i.e., a larger value is beneficial for noise and matching performance, whereas a smaller value is preferred in terms of power consumption, chip area, and operational speed.

Due to the mismatch sensitivity, the layout of the individual capacitors and the layout of the overall array is critical. For the overall array, symmetric common-centroid placement and dummies should be used. For the individual elements, one could either use foundry-default devices or sometimes manually optimized units are proposed to minimize the unit capacitor value or to improve parasitic shielding. An example is shown in Figure 12 where a unit capacitor of 0.5 fF is implemented using the fringing capacitance [11]. The actual capacitor value is validated with an RC extraction tool and chip measurements. The small capacitor value minimizes power consumption while still maintaining sufficient performance in terms of noise and linearity.

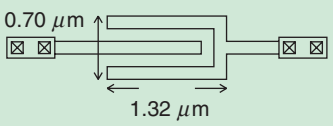

FIGURE 12: A manually designed 0.5-fF capacitor implementation.

A capacitor mismatch usually limits the SAR ADC to moderate linearity performance. To overcome this, a variety of techniques can be applied. A first possibility is the use of calibration, e.g., in [12]. In this example, a background algorithm determines the mismatch of the most important capacitors. Then, with this information, the actual capacitors are trimmed in an analog way by adding or removing very small calibration capacitors in parallel to the mismatched capacitors. The analog correction comes at low power and area overhead, while it can improve the linearity of the ADC substantially.

A second possibility is to apply oversampling and move the mismatch errors (partially) out of band. In [13], a combination of chopping and dithering is used to do so, while [14] implements a mismatch-error shaping technique.

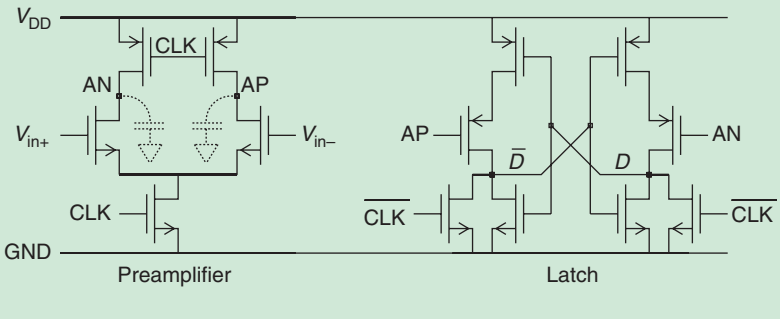

FIGURE 13: A two-stage dynamic comparator.

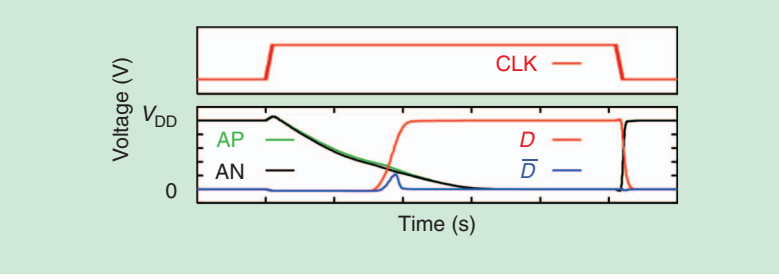

FIGURE 14: The transient simulation of the comparator.

Comparator

The task of the comparator is to determine whether its positive input signal (V_{in+}) is greater or smaller than its negative input signal (V_{in-}) and to produce a digital result (D) of that. An example of a dynamic comparator is shown in Figure 13 [15] that is activated upon a rising CLK edge, and it only consumes power on CLK transitions. Like most comparators, the design has two parts: 1) a preamplifier to provide initial gain and isolation toward the preceding DAC and 2) a latch stage that takes a decision based on positive feedback. The operation of the comparator is illustrated in Figure 14. Before the CLK becomes high, the PMOS devices in the preamplifier precharge the parasitic output capacitances to Vdd such that AP and AN are equal to Vdd. The latch outputs are initialized to ground (GND). When the CLK becomes high, the tail transistor of the preamplifier starts to conduct, and a current in the differential pair will flow that discharges the capacitors such that AP and AN will gradually reduce toward GND.

Assuming that a small input signal difference is applied ($V_{in+} > V_{in-}$), the resulting current imbalance will cause AN to go down a bit faster than AP, which reflects the dynamic preamplification of the input signal. The voltage difference between AP and AN is detected by the latch as soon as one of the input PMOS transistors of the latch starts to conduct. At this point, the latch will take over and a final output (D) is obtained. When CLK becomes low, the comparator will be reset to the initial condition.

The two most relevant imperfections of the comparator are noise and limited speed of operation, eventually resulting in metastability. Since the comparator has an analog input but a digital output, the modeling of noise is slightly different compared to a typical analog block. At the comparator input, the noise can be modeled as an input-referred noise source ($P_{n,\mathrm{cmp}}$ [V^2]). However, since the output is in the digital domain, the output noise should be modeled as a bit error rate (BER). The BER expresses that the decision of the comparator has a certain probability to fail due to the random noise of the circuit. The relation between the output probability and the input noise is given by the error function (ERF) function, where V_{in} is the differential input signal and P_1 is the probability for a 1 as digital output.

$$P_1 = \frac{1}{2}\left[1 + erf\left(\frac{V_{\mathrm{in}}}{\sqrt{2}P_{n,\mathrm{cmp}}}\right)\right]. \quad (3)$$

When V_{in} is positive and large, P_1 will approximate 1, revealing that the noise will not cause any decision error in this case. Similarly, when V_{in} is negative and large, P_1 will approximate 0. Only when V_{in} is close to zero, and in the order of magnitude of the input-referred noise voltage, probability P_1 will be affected by the noise.

For the circuit in Figure 13, the $P_{n,\mathrm{cmp}}$ is inversely proportional to the load capacitance of the preamplifier. At the same time, the power consumption of this stage is proportional to the same capacitance. As a result, there is a direct tradeoff between power and noise performance. A few possibilities have been published to overcome this tradeoff to some extent. For instance, [16] uses a two-mode comparator and redundancy to save power in the majority of SAR cycles while spending more power for better accuracy in the critical last cycles. In addition, [17] implements another technique that can reduce the impact of comparator noise in a power-efficient way by digitally averaging comparator decisions only for those cases that are affected by the BER of (3).

While pure SAR ADCs had a revival a few years ago, the trend in the most recent years is to combine SAR ADCs with other ADC architectures, leading to hybrid designs.

Finally, [18] implements a modified version of the comparator in Figure 13 and takes advantages of both the discharging and the charging phases of AP and AN to perform preamplification, rather than only using the discharging phase, thereby improving the power efficiency.

The second critical aspect in the design of a comparator is the delay. As visible in Figure 14, there is a certain amount of delay (τ_{cmp}) between the rising edge of CLK and the moment the output data D is valid. When the differential input voltage goes to zero, this delay can become extremely long as the comparator approaches metastability. Henceforth, the speed of a comparator should be verified for a small input magnitude to limit the chance of bit errors induced by metastability.

Logic

An example of the core of the SAR logic is given in Figure 15. It is usually composed of two sets of flip-flops. The first set implements a thermometric counter, where each activated flip-flop will initiate an operation of the SAR ADC. For instance, the first flip-flop will let the T&H sample the input signal. The second up to the N+1th flip-flop will perform the N cycles of the SAR algorithm by creating the CLK signal for the comparator, storing the results, and controlling the DAC. The second set of flip-flops implements the data register as it contains the digital code that controls the DAC. At the end of the SAR, this register will contain the final digital output code of the ADC. Other than these flip-flops, there are usually some additional logic gates required, e.g., to implement the DAC switching scheme. While a standard-cell design can be sufficient in many situations, for ADCs that demand very low power consumption or high speed of operation, custom logic design is usually applied, e.g., as explained in [11].

System-Level Tradeoffs

After discussing the detailed design of each block, this section discusses the overall tradeoffs in the design of an SAR ADC in terms of noise, linearity, speed, power consumption, and

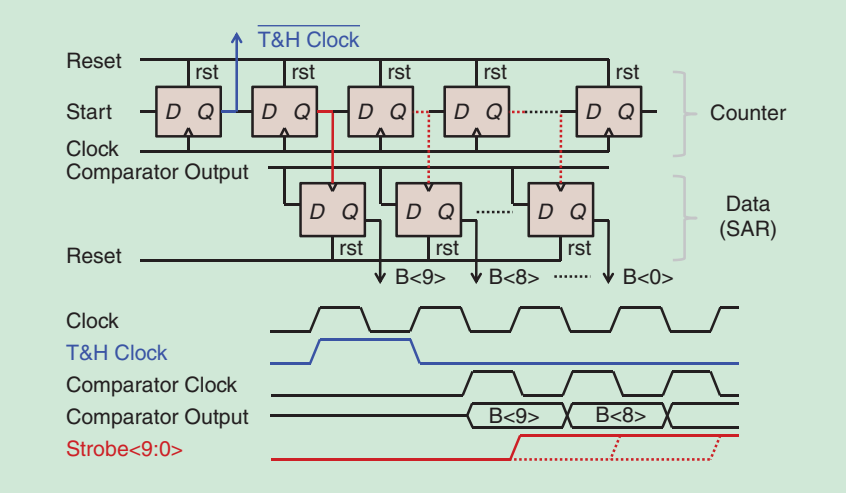

FIGURE 15: A logic and timing diagram of an SAR ADC.

When observing SAR ADC layouts, the largest component is usually the DAC, simply because it has the largest number of elements inside.

chip area. In terms of noise, the most important contributors are sampling noise ($P_{n,\text{th}}$), DAC noise ($P_{n,\text{dac}}$), comparator noise ($P_{n,\text{cmp}}$), and quantization noise ($P_{n,q}$). The first three terms were discussed previously. The quantization noise occurs because of the finite number of bits of the digital output code, resulting in rounding or quantization errors, which can be modeled as a noise source. The overall ADC noise is approximately given by the summation of the above four noise terms. Low-resolution SAR ADCs are typically quantization noise limited, as it is relatively simple and cheap to meet the thermal noise requirements ($P_{n,\text{th}}$, $P_{n,\text{dac}}$, and $P_{n,\text{cmp}}$). On the other hand, high-resolution SAR ADCs are typically limited by thermal noise, as it becomes expensive (in terms of power) to achieve low thermal noise, while quantization noise is now relatively cheaper to minimize.

In terms of the ADC's transfer function, offset and gain errors of the various blocks (e.g., the comparator, DAC, T&H) are usually not very critical, as they simply translate to an ADC input-referred offset or an overall gain error but do not cause distortion. For that reason, these error sources can often be ignored or have relaxed requirements. However, in the case of a time-interleaved ADC, or particular applications that require an ADC with absolute precision, offset and gain errors need to be minimized or compensated by means of calibration. Other than these linear errors, the distortion of the SAR ADC is usually limited by either T&H distortion or by DAC nonlinearity caused by mismatch. Those nonlinearities are immediately visible at the ADC input and thus need to be taken into account.

In terms of speed, we have seen in Figure 4 that in one clock cycle T_{clk}, which has a duration of $T_s/(N + 1)$, the DAC, comparator, and logic need processing time. When these times are denoted by τ_{dac}, τ_{cmp}, and τ_{logic}, the sum should always remain smaller than T_{clk}, thus leading to a speed tradeoff between these blocks. Instead of using a synchronous SAR ADC, where T_{clk} is externally provided and fixed to a fraction of T_s, an alternative is to use an asynchronous implementation. In an asynchronous SAR ADC, only T_s is provided from the outside while T_{clk} is not. T_{clk} is then internally generated, allowing a variable value of T_{clk} for each cycle as long as a total of N T_{clk} cycles can fit into the conversion time. This allows an increase of T_{clk} for cycles where the comparator is close to metastability as long as the other cycles are a bit faster to compensate for the lost time. As a result, the asynchronous architecture offers a better handling of comparator metastability, while it also reduces the frequency of the externally required clock.

When looking at power consumption, we should realize that the SAR ADC has both analog and digital blocks. The digital logic complexity (and, hence, power consumption) scales linear with the resolution *N*. On the other hand, the power consumption of analog blocks is constrained by noise. Fundamentally, the power of analog blocks scales with a factor of four for each 6-dB increase in SNR (which corresponds to 1-b resolution). Hence, the analog power will scale exponentially with *N*. As a result, low-resolution SAR ADCs (or those in older process technologies) tend to have a large power consumption in the digital part. Here, it pays off to explicitly optimize the logic implementation. For high-resolution ADCs, the exponentially growing analog power consumption will quickly start to dominate, in particular, the power from the DAC and the comparator. In these cases, the techniques described previously to minimize DAC and comparator power consumption are useful.

When observing SAR ADC layouts, the largest component is usually the DAC, simply because it has the largest number of elements inside. When area is important, minimizing the number of elements (e.g., by using a split capacitor array) or minimizing the area per element (e.g., by optimizing the layout of each capacitor unit) is advisable.

State-of-the-Art SAR ADCs and Future Trends

As illustrated in the introduction, SAR ADCs can cover a very wide application range. In this section, we mention a few designs that are state of the art in terms of speed, precision, or power consumption. We also discuss emerging trends in the design of SAR ADCs.

In [2], an 8-b SAR ADC operating at an impressive sample rate of 90 GS/s is presented. This speed is achieved by time interleaving 64 SAR ADC channels, each operating at 1.4 GS/s. Using an advanced technology node, 32-nm silicon on insulator CMOS also helps to achieve this speed, which demonstrates the potential of technology scaling for SAR ADCs. In terms of design aspects, a DAC with redundancy and alternate comparators are used to maximize speed while the calibration of offset, gain, and timing mismatches between the channels is employed to increase the precision.

The state of the art in terms of accuracy is [14], achieving an SNDR of 101 dB with a very low power consumption. To achieve this performance, the advantage is taken of an oversampling technique. Next, the DAC mismatch errors and the comparator noise are frequency shaped and moved out of band such that the baseband reaches a very clean spectrum.

When looking at power consumption, a notable work is [19], which

describes a 10-b 1-kS/s SAR ADC that consumes only 1 nW. Such low power is achieved by using small DAC capacitors, an energy efficient comparator design, manually optimized asynchronous logic, and sub-1-V operation. Moreover, the leakage current is carefully reduced by sizing and the selection of transistor types.

While pure SAR ADCs had a revival a few years ago, the trend in the most recent years is to combine SAR ADCs with other ADC architectures, leading to hybrid designs. These hybrids try to take advantage of the power efficiency of SAR ADCs while using concepts from other topologies to overcome the shortcomings of SAR ADCs. For instance, we mentioned [2] previously, which uses time interleaving to increase the speed beyond the capabilities of a single SAR ADC. Other works, e.g., [20], create a pipelined ADC based on SAR substages, which also increases the speed of operation as well as the resolution. A subranging SAR ADC is presented in [9] that achieves a state-of-the-art power efficiency of 0.85-fJ/conversion step at 10-b resolution and at 200 kS/s. Noise-shaping SAR ADCs [21] or sigma-delta modulators with an internal SAR quantizer [22] have been proposed to increase the precision of SAR ADCs toward the domain that is presently dominated by sigma-delta modulators. Altogether, these hybrid designs open a whole new field of opportunities to be explored.

Conclusion

This article has described the basics of the design of an SAR ADC and discussed various circuit implementations, the most critical circuit imperfections, and design tradeoffs. Modern SAR ADCs can use relatively simple hardware, yet a lot of algorithmic and circuit-level innovations can be applied on top of that to improve power efficiency, speed, and accuracy. Besides these basics, the state of the art was briefly described and future trends were identified. Noting the rapid improvement in recent years, we can expect more SAR-based approaches with unprecedented performance in the near future.

References

[1] B. Murmann. (2015). ADC performance survey 1997–2014. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[2] L. Kull, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, "A 90-GS/s 8-b 667-mW 64x interleaved SAR ADC in 32-nm digital SOI CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2014, pp. 378–379.

[3] T. B. Cho and P. R. Gray, "A 10-b, 20 MSample/s, 35-mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[4] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[5] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[6] B. P. Ginsburg and A. Chandrakasan, "A 500-MS/s 5-b ADC in 65-nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, 2006, Honolulu, HI, pp. 140–141.

[7] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon, "Merged capacitor switching based SAR ADC with highest switching energy efficiency," *IET Electron. Lett.*, vol. 46, no. 9, pp. 620–621, Apr. 2010.

[8] C.-Y. Liou and C.-C. Hsieh, "A 2.4-to-5.2fJ/conversion-step 10-b 0.5-to-4MS/s SAR ADC with charge-average switching DAC in 90-nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2013, pp. 280–281.

[9] H.-Y. Tai, Y.-S. Hu, H.-W. Chen, and H.-S. Chen, "A 0.85fJ/conversion-step 10-b 200-kS/s subranging SAR ADC in 40-nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2014, pp. 196–197.

[10] J. Xu, P. Harpe, J. Pettine, C. Van Hoof, and R. F. Yazicioglu, "A low power configurable bio-impedance spectroscopy (BIS) ASIC with simultaneous ECG and respiration recording functionality," in *Proc. Euro. Solid-State Circuits Conf.*, Graz, 2015, pp. 396–399.

[11] P. Harpe, C. Zhou, Y. Bi, N. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, A 26-μW 8-bit 10-MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, July 2011.

[12] M. Ding, P. Harpe, Y.-H. Liu, B. Busze, K. Philips, and H. de Groot, "A 5.5fJ/conv-step 6.4-MS/s 13-b SAR ADC utilizing a redundancy-facilitated background error-detection-and-correction scheme," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2015, pp. 460–461.

[13] P. Harpe, E. Cantatore, and A. van Roermund, "An oversampled 12/14-b SAR ADC with noise reduction and linearity enhancements achieving up to 79.1-dB SNDR," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2014, pp. 194–195.

[14] Y.-S. Shu, L.-T. Kuo, and T.-Y. Lo, "An oversampling SAR ADC with DAC mismatch error shaping achieving 105-dB SFDR and 101-dB SNDR over 1-kHz BW in 55-nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2015, pp. 458–459.

[15] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9-μW 4.4fJ/conversion-step 10-b 1-MS/s charge-redistribution ADC," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2008, pp. 244–245.

[16] P. Harpe, G. Dolmans, K. Philips, and H. de Groot, "A 0.7-V 7-to-10-bit 0-to-2-MS/s flexible SAR ADC for ultra low-power wireless sensor nodes," in *Proc. Euro. Solid-State Circuits Conf.*, Bordeaux, 2012, pp. 373–376.

[17] P. Harpe, E. Cantatore, and A. van Roermund, "A 10-b/12-b 40-kS/s SAR ADC with data-driven noise reduction achieving up to 10.1-b ENOB at 2.2fJ/conversion-step," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3011–3018, Dec. 2013.

[18] M. Liu, P. Harpe, R. van Dommele, and A. van Roermund, "15.4 A 0.8-V 10-b 80-kS/s SAR ADC with duty-cycled reference generation," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2015, pp. 278–279.

[19] P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. van Roermund, "21.2 A 3-nW signal-acquisition IC integrating an amplifier with 2.1 NEF and a 1.5fJ/conv-step ADC," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2015, pp. 382–383.

[20] F. van der Goes, C. Ward, S. Astgimath, H. Yan, J. Riley, J. Mulder, S. Wang, and K. Bult, "11.4 A 1.5-mW 68-dB SNDR 80-MS/s 2x interleaved SAR assisted pipelined ADC in 28nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2014, pp. 200–201.

[21] J. A. Fredenburg, and M. P. Flynn, "A 90-MS/s 11-MHz bandwidth 62-dB SNDR noise-shaping SAR ADC," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2012, pp. 468–469.

[22] S. Porrazzo, V. N. Manyam; A. Morgado, D. San Segundo Bello, C. Van Hoof, A. H. M. van Roermund, R. F. Yazicioglu, and E. Cantatore, "A 1-V 99-to-75-dB SNDR, 256-Hz–16-kHz bandwidth, 8.6-to-39-μW reconfigurable SC ΔΣ modulator for autonomous biomedical applications," in *Proc. Euro. Solid State Circuits Conf.*, Bucharest, 2013, pp. 367–370.

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