Chapter Summaries of Thesis

Berkay IPEK

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Contents

1 Summary of Chapter 1: Introduction

- **Overview of ADCs and Time-Interleaving (TI):**
  Begin by introducing Analog-to-Digital Converters (ADCs) and the concept of Time-Interleaved ADCs (TI-ADCs) and Pipeline ADCs. Explain why TI architectures are commonly used in high-speed applications, emphasizing their advantages—such as increased sampling rate—and the typical challenges they introduce, including offset, gain, and timing mismatches.

- **Need for an Input Buffer in ADCs:**
  Discuss the necessity of using an input buffer at the ADC front-end. Explain how parasitic capacitances from PCB traces, cables, or packaging can degrade signal performance, and how the buffer mitigates these effects by improving impedance matching and driving capability.

- **Buffer Performance and Its Impact on TI-ADCs:**
  Analyze how the input buffer's characteristics influence the overall ADC performance. Highlight that distortion generated by the buffer, especially at high frequencies, can significantly limit the achievable dynamic range and linearity of the entire converter.

- **Performance Metric Selection (THD):**
  Justify the use of Total Harmonic Distortion (THD) as the main performance indicator. Present a representative graph of input and output voltage's THD versus input frequency and discuss its behavior—particularly noting that at higher frequencies, THD degrades (e.g., below –80 dB), which is undesirable.

- **Problem Definition and Solution Approaches:**
  Identify the main issue: the degradation of buffer linearity at high frequencies. Outline two potential solutions:

  1. **Redesigning the buffer**, which could improve linearity but would significantly increase power consumption (e.g., above 30 mW).
  2. **Calibration-based approach**, which allows compensation of nonlinearity without major power penalties.

- **Calibration Strategy:**
  Discuss calibration as a low-power alternative. Introduce the distinction between *foreground* (static) and *background* (dynamic) calibration methods, explaining their respective advantages and disadvantages in terms of complexity, power consumption, and update rate.

- **Foreground Calibration Implementations:**
  Explore possible implementations of foreground calibration, such as lookup tables (LUTs) and piecewise-linear approximations. Compare their characteristics, and conclude by motivating the choice of the LUT-based approach as an energy-efficient and practical solution for this work.

2 Summary of Chapter 2: Theory

- **Linear and Nonlinear Systems:**
  Begin by distinguishing between linear and nonlinear systems. Explain that a nonlinear system can introduce distortion and harmonic components in the output signal, dependent of the input frequencies
- **Mathematical Modeling of Nonlinearity:**
  Introduce mathematical models commonly used to describe nonlinear behavior, including the Taylor series, Volterra series, and memory polynomial models. Note that while the Taylor series approximates static nonlinearities, it cannot represent memory effects present in dynamic systems.
- **Applicability of Polynomial Calibration:**
  Explain that direct polynomial-based (Taylor series) calibration is effective only for systems with static nonlinearities, where frequency-dependent distortion is negligible. In such cases, the system can be accurately modeled using a simple polynomial fit.
- **Need for Memory Representation:**
  For systems exhibiting dynamic or frequency-dependent nonlinearities—such as the input buffer of a high-speed ADC—a memory model becomes necessary. The Volterra series or memory polynomial approaches can capture these memory effects.
- **Limitations of the Volterra Series:**
  Discuss the main drawback of the Volterra series: the number of coefficients increases rapidly with nonlinear order and memory depth. This results in high computational complexity, longer processing times, and increased power consumption, making it unsuitable for low-power applications.
- **Motivation for the Memory Polynomial Approach:**
  Conclude by motivating the use of the memory polynomial model as a practical alternative. It captures dominant nonlinear and memory effects with significantly fewer coefficients, providing an efficient balance between accuracy and power consumption for the proposed calibration scheme.

3 Summary of Chapter 3: Real Application

- **Simulation Setup in Cadence Virtuoso:**
  Describe how the input and output data were obtained from Cadence Virtuoso simulations. Include details about the simulation environment, and relevant configuration parameters. Present a general plot of the input and output waveforms for several input frequencies. Emphasize that, since the target system is a high-speed ADC, more simulation points were concentrated at higher frequencies where performance degradation is most critical.

- **Spectral Analysis:**
  Provide frequency-domain results by plotting the spectra of both input and output signals at low, medium, and high frequencies. Highlight that at higher frequencies, the contribution of higher-order harmonics becomes increasingly dominant.

- **Linearity Assumption and Invertibility Test:**
  Initially assume that the system is linear and can be modeled using a static nonlinearity such as the Taylor series. Define the relationship between input and output as a transfer function $H(s)$, and compute its inverse $H^{-1}(s)$. Apply this inverse function to the output signal to test if the reconstructed signal matches the original input. The resulting mismatch, particularly at high frequencies, demonstrates that the system cannot be accurately represented using only a Taylor series. Therefore, a memory-dependent model is required.

- **Memory and Polynomial Orders:**
  Introduce the concept of *memory order* and *polynomial order* in the calibration model. Explain that only odd-order polynomial terms are considered, as even-order harmonics can be neglible.

  - To determine the suitable polynomial order, fix the memory order and vary the polynomial order (e.g., 3, 5, 7, and 9). Compare the resulting calibrated signal spectra and show that, for high-frequency operation, a 9th-order polynomial is necessary to meet the linearity target (THD $< -80\,\text{dB}$).
  - Next, fix the polynomial order to 9 and vary the memory order. Results indicate that at least a 5th-order memory is required for accurate calibration.

- **Memory Sweep Experiment:**
  To reduce the number of coefficients (and consequently, power consumption), perform a memory sweep experiment. For a given memory order, test every possible combination of input terms $x(t)$, $x(t-1)$, $x(t-2)$, ... up to $x(t-n)$. Run the calibration with memory orders of 3, 5, 7, and 9 at a high frequency. The results confirm that a memory order of 5 provides the best balance between accuracy and efficiency.

- **LUT-Based Calibration and Quantization Effects:**
  Introduce non-idealities associated with implementing calibration using a Lookup Table (LUT). Since LUT-based systems require digital representation, all elements—input signal, coefficients, and output—must be quantized, introducing quantization noise at each stage.

- **Quantization of Input Signal (V_{in}):**
  Explain how quantization noise was added to the input signal. Compare four cases with different quantization resolutions (n = 10, 12, 14, and 16 bits) by plotting their spectra. Show that 14-bit quantization offers

a good compromise between precision and resource usage. Then, present calibration results with a 5th-order memory and 9th-order polynomial, showing that the THD target ($-80\,\mathrm{dB}$) is not met. As a solution, increase the memory order up to 9 (e.g., memory orders [5, 9]) and show the improved THD results.

- **Quantization of Coefficients:**
  Describe the quantization of the calibration coefficients. Normalize the coefficients so that only their fractional part requires fine resolution, while the integer part can be represented by a single bit. Present results for the calibration accuracy using fractional bit resolutions from 1–6 bits (insufficient), 7–12 bits, 13–18 bits, and 19–24 bits. Demonstrate that after 20 fractional bits, the improvement saturates, indicates 21 bits are enough to represent coefficients in the LUT.

- **Quantization of Output Voltage:**
  Explain how quantization noise is added to the output voltage, which represents the final calibrated digital output. Following the same methodology, show that 14 bits are sufficient to represent the output signal without significant distortion.

- **Coefficient Reusability Across Frequencies:**
  To minimize LUT storage requirements, test whether coefficients obtained at one frequency can be reused at other frequencies. Present comparison plots for a few cases with memory order 9 and polynomial order 9. Discuss that the coefficients vary significantly with frequency due to the memory-dependent nature of the system. Confirm this by showing that when the memory order is reduced to zero (memoryless case), the coefficients remain consistent across frequencies, validating the frequency dependence introduced by memory effects.

4 TODO Summary of Chapter 4: Real Implementation

5 TODO Summary of Chapter 5: Conclusion