High-Speed Time Interleaved ADCs

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ABSTRACT

Software-defined multi-gigahertz receivers require high-speed ADCs at the front-end. Time interleaving has emerged as the most common method of achieving ultra-fast quantization at reasonably high resolution. However, this multi-path solution introduces systematic errors due to mismatches in signal paths, whereas in non-interleaved versions these were mixed to DC, where they appeared as a harmless offset. Mitigating all possible time-interleaved errors comes at a heavy cost in complexity, risk, and power. Knowing which errors are most important and which can be neglected in any given application is essential for picking an appropriate architecture and calibration scheme. Guidelines for reducing errors lead to potentially different architecture choices. When the goal is to use the fewest slices, an interleaved pipelined ADC results, whereas when the overriding objective is to use the simplest slice possible, a large array of SAR slices is usually adopted. Both approaches have merit. This article addresses when and where to use each approach by discussing specification requirements and showing that different types of error sources should not be merged into one single metric like ENOB, but should be treated separately to determine their impact on overall system performance. An example of an eight-way interleaved pipelined ADC is presented, which illustrates these principles in the context of a real circuit.

INTRODUCTION

Resolution and speed of analog-to-digital converters (ADCs) continue to improve to the point where digitally-based transceivers are now common in many broadband systems above a few gigasamples. Cable TV, satellite TV, backplanes for network routers, and optical communication links are notable applications. Quantifying the improvement in ADCs can be a subjective matter as multi-dimensional metrics may have one component that is vital for some applications but virtually irrelevant for others. Nevertheless, general trends in circuit quality can be mapped using a few key metrics, such as signal-to-noise-and-distortion ratio (SNDR) and power dissipation. Thankfully, such data has been carefully collected and made publicly available by Boris Murmann for published works at the industry's two premier conferences, the International Solid-State Circuits Conference (ISSCC) and Symposia on VLSI Technology and Circuits (VLSI Symposia), since 1997.

Often this data is graphically represented as two separate plots: resolution vs. speed or power vs. speed. It is difficult to determine the benefits of a given design using only one of these two-dimensional plots: both resolution and power should be considered simultaneously to adequately evaluate quality. Figure 1 provides one means of visualizing four items of data in a two dimensional plot. Resolution vs. speed is represented by the position on the x and y axes. The power dissipation of the ADC is visualized by the size of the circle, which is proportional to the log of the power dissipation. Finally, the color of the marker is used to show the year of publication. Designers aim to move toward the upper right corner, achieving the highest resolution at the highest speeds while having the smallest dot possible (meaning low power). A few trends stand out in this plot: The speed-resolution frontier is constantly expanding over time toward the upper right corner as most of the "best" performing ADCs have been published in recent years. Also, the power required to obtain better performance at higher speed remains as low or lower than was needed for slower, less precise ADCs in years past.

To aid the reader in becoming better equipped to make optimal architectural and design decisions about time-interleaved ADCs, primary error sources are categorized as *additive* and *multiplicative* and considered for their impact on system performance in both time- and frequency-domain applications. Putting these ideas into practice, an example implementation of a time-interleaved pipelined ADC is presented to illustrate design choices.

ADC ERROR SOURCES

Time-interleaving is a widely used option to push ADC performance boundaries to even higher throughputs by exploiting arrays of reduced speed quantizers operating on subsections of the signal. The technique is not without challenges. The very nature of interleaving forces the signal to traverse multiple paths on its way to the output. Physically distinct circuits process different subsections of the signal, thereby causing any mismatch to result in pattern-dependent errors. Sources of errors and their impact on the combined output of parallel ADCs were analyzed and described as early as the 1980s [1, 2], further into the 1990s [3, 4], and later by several authors [5–7].

Software-defined multi-gigahertz receivers require high-speed ADCs at the front-end. Time interleaving has emerged as the most common method of achieving ultra-fast quantization at reasonably high resolution. However, this multi-path solution introduces systematic errors due to mismatches in signal paths, whereas in non-interleaved versions these were mixed to DC where they appeared as a harmless offset.

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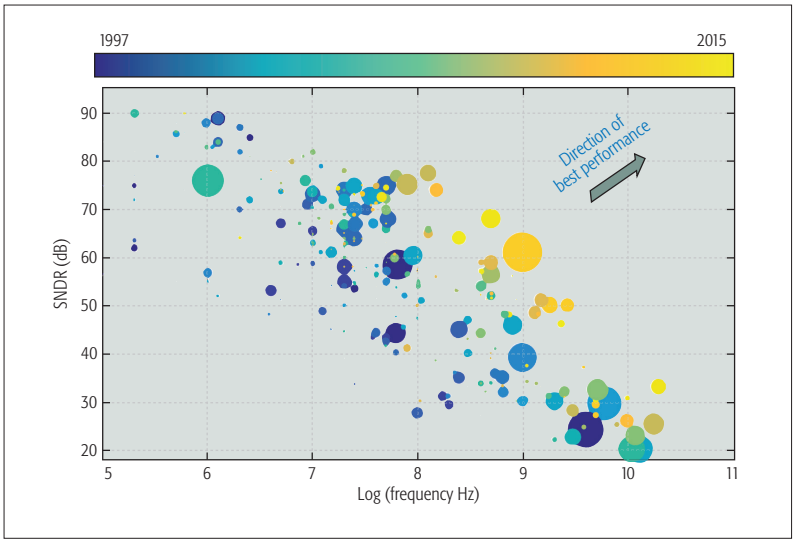

Figure 1. ADC performance survey, 1997–2015 (ISSCC and VLSI Symposia). The size of a marker is proportional to log of power dissipation, and color represents year of publication.

Fundamental Error Sources

Fundamental error sources include additive random noise and quantization. No amount of calibration can reduce these errors, which can only be mitigated by brute force design. Additive noise is dictated by kT/C and $1/g_m$. Reducing thermal noise requires an increase in either area or power, and usually both. Likewise, sufficient digital levels must be included to ensure that quantization noise is not detrimental to overall performance. This simply entails increasing the number of physical bits in the converter, also adding to area and power.

Errors That Can be Eliminated by Calibration

Other errors can be minimized by calibration. These include quasi-linear distortion from front-end buffers and track and hold circuitry, linear and nonlinear radix errors, and element mismatch. Calibration has been used to eliminate these errors within a single ADC slice without increasing area and power.

Time-Interleaved Error Sources

Lastly, time-interleaving introduces another set of errors associated with multi-path mismatches. These include offset errors, which, it is important to note, are not static but can drift due to $1/f$ noise. Offset artifacts will show up in the output spectrum due to $1/f$ noise if the correction bandwidth is not fast enough. Mismatch in gains generate errors that are amplitude modulated with the signal, while timing skews in samplers systematically phase modulate the signal. Additional variations in bandwidth of the slices makes the gain and the timing errors both frequency-dependent and non-orthogonal.

Impact of Additive and Multiplicative Error Sources

All error sources affect the signal in either an additive or multiplicative way. Additive nonidealities include the fundamental sources, thermal noise and quantization, but also include radix errors, element mismatch, and offset mismatch. Additive errors are the most problematic because they do not scale with the signal. As the amplitude is reduced, signal information eventually drops into the fixed noise. Conversely, multiplicative errors are much less important for lower-level signals. Such errors are reduced when the signal energy drops, meaning if the signal-to-noise ratio (SNR) is adequate when the signal is large, it remains adequate when the signal is small as noise and signal scale together.

Sine Wave Input vs. Gaussian Distributed Signals

One of the reasons for relaxation of specifications of the ADC for multiplicative errors is related to how ADCs are usually specified. The traditional technique is to apply a full-scale sine wave to the input. However, performance of the converter with a single tone is not representative of ADC behavior with the actual signal statistics. ADCs for broadband channelizers must back-off the root mean square (rms) level of the signal to avoid hard clipping. Rather than stimulating the ADC with a single narrowband tone, the input is broadband and Gaussian distributed where most of the amplitudes are at low to moderate levels, and compressive distortion at the signal extremes are rarely excited.

Performance in the presence of backed-off signals is much less sensitive to multiplicative errors such as quasi-linear distortion, time skews, and gain errors because they are reduced, relative to full-scale, by the back-off level. As this back-off is often 12 dB relative to a full-scale sine wave, multiplicative errors can be relaxed by as much as two full bits. When designing a time-interleaved ADC for broadband applications, it is these multiplicative errors, that is, smooth, quasi-linear distortion and mismatch of gain and timing, that can be relaxed. This leads to design trade-offs that can simplify the front-end and the calibration scheme significantly [8]. Additionally, the signal statistics for embedded applications are known in advance, so significant simplifications in calibration schemes can be used reliably. Auto-correlation and zero-crossing timing measurements work well in these environments because the richness of the signal spectrum provides more than sufficient randomness.

Smooth vs. Jagged Distortion

One of the difficulties in producing an optimal multi-channel time-interleaved design from a standard specification is that traditional ADC evaluation based on a sine wave input have metrics with contributions from many different types of error sources. For example, total harmonic distortion (THD) results from compressive distortion of the "smooth" quasi-linear front-end transfer function, but it also arises due to "jagged" radix errors and element mismatch. These errors scale differently with amplitude, rendering a lumped specification for THD virtually meaningless for most applications: a circuit could meet a THD specification but fail the system performance when the errors are "jagged," whereas another could fail the THD requirement while comfortably meeting system performance if the errors are due to "smooth" quasi-linear distortion. Therefore, lumped THD is not the right metric to specify. What is needed is information as to how the THD scales with amplitude, and

a separate specification for "smooth" multiplicative distortion and abrupt, additive "jagged" distortion; otherwise, the ADC is likely to be over-designed in one area and under-designed in another.

Architecture Considerations

Before giving advice on architectural choices, the reader should be aware of the author's biases and limited experience in time-interleaved ADCs, which have primarily been restricted to five separate designs ranging from 12 bits at 2.5 GS/s to 8 bits at 64 GS/s. Layouts for all five chips are shown in Fig. 2 and illustrated using the same resolution vs. speed format as Fig. 1.

Time Domain vs. Frequency Domain Modulation

Choosing an appropriate architecture greatly depends on the intended application of an ADC as errors impact various systems quite differently. Often the goals of proposed calibration techniques are ambitious with aims to provide workable solutions for virtually all classes of input signals. This is usually not necessary, as most high-speed ADCs are embedded and therefore only used for one purpose. Calibrating only what is important for this one and only application leads to more efficient and smaller designs. The two most common embedded applications are:

- Multi-channel frequency-division multiplexed signals, such as in cable and satellite TV
- Baseband applications for optical and backplane transceivers

The first is best understood by viewing signals and errors in the frequency domain, while the second is easiest to understand in the time domain.

In time-domain applications such as for radar, backplanes, and optical networks, spectral purity is not as important, so there can be some relaxation of offsets. Most channels with sufficient inter-symbol interference also have a Gaussian distribution of the baseband signal, so the sensitivity to multiplicative errors is also less important than additive errors by the back-off level. As gain and time-skew errors are multiplicative, they often do not need to be calibrated to the same accuracy level of additive errors like thermal noise and offsets. Background calibration of time skews may not be necessary, which further simplifies the overal system.

Rules of Thumb for Time-Interleaved ADCs

After painstaking effort in the laboratory to track down as many sources of errors as possible and determine ultimate limitations of the calibration algorithms, a general consensus emerged about what constitutes good design practice. This experience can be summarized as "rules of thumb" for time-interleaved ADC design. The least controversial rules are listed here.

Never interleave if you do not have to: There are many error sources in multi-path design that are not present in a single-slice ADC. If you can keep the signal path from branching, you save a lot of headaches. If speed or metastability are not at issue the ADC can and should be designed without interleaving.

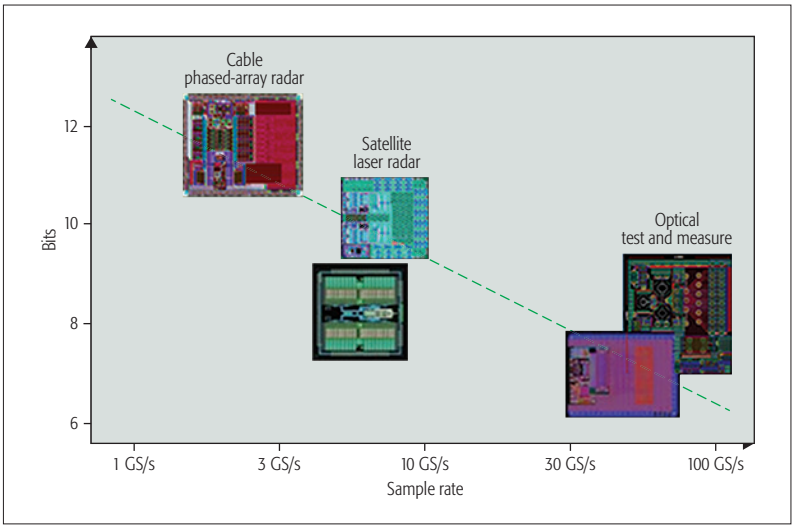

Figure 2. Five time-interleaved ADCs ranging from 12 bits at 2.5 GS/s to 8 bits at 64 GS/s.

Avoid interleaving by two: This might not be obvious at first, but is essentially a corollary to the above rule. If it is possible to design the ADC with only two slices, it should be *nearly* possible, given a little more power, area, time, and risk, to design it with one. Removing all time interleaving is highly advantageous as it eliminates many error sources, most of which require calibration to mitigate. In the special case where there is no signal energy above $f_s/4$ and interleaving is only used as a means to 2× oversample the signal, thereby gaining 3dB in noise performance, this is an exception where interleaving by two might be useful. Otherwise, avoid it. Obviously, if you exhaust all options and still cannot meet the speed requirements, interleaving by two might be the only viable option left. Just make it your last option and not your first.

Use as few slices as possible: Increasing complications arrise as the number of independent slices in an ADC increases. Crosstalk from multiple sources is hard to control as the array gets larger, and as the input signal and clock distribution networks become more complicated. In addition, the difference in the integral nonlinearity (INL) profile of each quantizer generates pattern-dependent errors, which for high-resolution ADCs requires many lookup tables and dither to eliminate, quickly becoming prohibitive in a large array. Keeping the number of quantizers small, but still more than two, is a good idea. Four slices is usually a good place to start.

Pipelined Slices vs. SAR

Adhering to the third rule leads to the strategy of making the ADC slices as fast as possible without compromising power and dynamic settling behavior. This approach was adopted for all ADCs shown in Fig. 2. Each used a pipelined architecture for the slices as itemized in Table 1.

Pipelining allows a high sample rate as throughput is limited only by the speed of a single multiplying digital-to-analog conversion (MDAC) stage. Primary MDAC error sources are highlighted in Fig. 3. These include linear and nonlinear errors in the residue amplifier, and dynamic effects of incomplete settling and

ADC				
Sample rate	Resolution	Slice architecture	Bits per stage	Nominal radix
2.5 GS/s	12 bits	Pipelined	3.5	7.95
6.0 GS/s	10 bits	Pipelined	2.5	3.8
6.0 GS/s	8 bits	Pipelined	0.7	1.6
40.0 GS/s	6 bits	Pipelined	0.7	1.6
64.0 GS/s	8 bits	Pipelined	2.5	3.8

Table 1. Table of ADC architecture details.

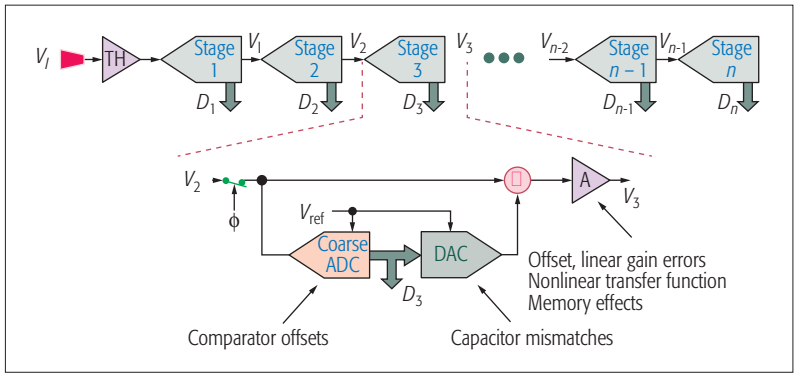

Figure 3. Block diagram of a single 12-bit pipelined ADC slice. Background calibration adjusts the radix and populates a lookup table to remove any errors due to capacitor mismatch.

memory effects due to incomplete reset. All can be corrected digitally as well as mismatched elements in the DAC, which are usually compensated with a lookup table.

Design guidelines, although based on data and experience, are nevertheless subjective. Different designers may arrive at different "rules of thumb" which in turn lead to different design choices. There is a competing school of thought with regard to time-interleaved ADC design to **make each slice as simple as possible.** This guiding principle results in large arrays of interleaved successive approximation register (SAR) ADCs as each SAR slice is simple, compact, and energy-efficient. Since SARs require no resampling of a residue as in a pipelined ADC, there is no gain element needed and therefore no radix error to calibrate. This is indeed an advantage. Calibration of capacitor mismatch is still needed for higher resolution applications, and there are more slices to calibrate, but this can be static and done once at startup or even at factory test and is not required to run in the background.

The drawback with SAR arrays is simply that there are a lot of slices. Assuming roughly the same settling time plus comparator decision delays for both implementations, the number of SARs required in an n-bit ADC is about n times more than for a pipelined implementation as the SAR requires n clock cycles per sample, whereas the pipelined converter requires one. For instance, an ADC constituting a 10-bit, pipelined, four-slice, interleaved approach would require approximately 40 SAR slices for the same resolution and throughput. The complexity of input distribution and clocking networks also increases with the number of slices. Although the quantizer itself is simple, getting the signals and clocks routed to each slice often becomes more complicated than the quantizer itself and can eventually dominate the power dissipation. To counteract this, asynchronous design heavily reduces clock distribution issues to the point where in some cases it is not relevant to the total power budget [9].

To avoid routing a high-speed input to many samplers in a large array, a multi-rank sampling scheme is needed whereby the input is resampled and demultiplexed without gain before quantization. This is an important point to remember when considering a large array. Although some ADCs use a large number of SAR quantizers, they generally adhere to the third rule, which can be amended here to read: **Use as few front-end samplers as possible**. Once the critical first sample is taken, the held signal can be resampled without suffering further errors due to timing skew provided the signal is settled.

Which Architecture Is Best

Although a SAR slice is simpler and more power-efficient than a pipelined ADC, when considering signal and clock distribution as part of the slice design, the SAR slice becomes less efficient, and the two approaches become more comparable. Likewise, a pipelined architecture requires far fewer slices, but a two-rank sampling system makes a large array hierarchically look the same as small arrays from a front-end perspective provided kT/C noise is not compromised by double-sampling.

Both time interleaving of high-count SAR arrays or the use of fewer pipelined slices have merit. Pipelined-based designs are most appropriate for high-resolution signal analysis applications where spectral purity is important such as in spectrum analyzers. Minimizing the number of slices keeps interleaving artifacts to a minimum so that calibration can reduce all residual errors to achieve 80 dB spurious-free dynamic range (SFDR) at 2.5 GS/s [10]. It is difficult to achieve the same level of spectral purity when there are so many SARs that all need to be calibrated to the same level of accuracy. Therefore, SAR arrays are suitable for lower-resolution applications where spectral purity is not as important and kT/C noise requirements are easily met. They have been widely used in high-speed applications, such as in optical networks, backplanes, and real-time oscilloscopes where eight physical bits and about five or six effective bits are common.

8× Time-Interleaved ADC with Slow Reference

As each of the ADCs of Fig. 2 and Table 1 are interleaved pipelined architectures, one design is highlighted here that is representative of all five. This circuit is a 2.5 GS/s 12-bit ADC, implemented as an eight-way time interleaved pipelined architecture and shown in Fig. 4. When presented with the requirements, we primarily considered the first rule, but found it would be nearly impossible to achieve the throughput without interleaving, so the guiding principle in

the design became the third rule: to use as few slices as possible. The initial plan was to use four slices as previously recommended. Each slice would run at approximately 625 MS/s. Initial simulations showed this to be an appropriate choice. As often happens, circuit model and extraction parameters changed during the course of the design to where it became difficult to meet the speed and performance requirements simultaneously. Therefore, eight interleaved slices at 312 MS/s were chosen for the final design.

A slow (1 MS/s) recirculating ADC with dynamic capacitor shuffling is used to provide a reference sample: the error between the actual sample and the reference is used to drive all background calibration. Some drawbacks of the impact of the slow ADC on performance are discussed more fully later.

A single least mean squared (LMS) loop converges all error sources simultaneously [11]. Within each ADC slice the radix is corrected: a lookup table is populated to mitigate errors due to capacitive mismatch in the MDAC. The gain, offset, and time-skew errors of each slice are corrected by forcing them to match the reference ADC. System identification (SI) methods are used for calibration in this design. Since LMS updates are driven by observations from a known reference, this approach, which is common in control systems and adaptive equalizers, is known to be robust and have good convergence properties. Performance is virtually independent of signal statistics, although degenerate cases always exist (e.g., $f_s/8$ tones). Convergence is quick without requiring long decorrelation filters to extract the signal from a randomly applied dither.

To align each of the eight slices to the reference ADC, a full-speed 2.5 GS/s clock is run through a delay line ranging from one- to eight-unit samples. The delay position is randomly selected, multiplexed, and then retimed with the full-speed clock before being divided and then retimed again after the divide-by-eight. Therefore, the reference ADC will align with any of the eight slices with the exact precision of one unit-interval step, but in a user-selectable random order. In this manner calibration of the entire time-interleaved array is accomplished one slice at a time: the reference aligns to each slice, calibrates the errors, then moves to the next randomly selected slice until the complete array is corrected. All calibration is autonomous and operates in the background. Calibration updates can also be frozen by user control depending on the application. No pilot tones or dither are necessary. However, sufficient signal activity at the input is required in order to have something to compare to and correct. In the absence of a signal, a power detector circuit holds the calibration registers frozen until a signal with sufficient amplitude is present.

The layout of the ADC is shown in Fig. 5, which illustrates that all calibration circuitry resides on chip as does an 8 kS memory for use in test. All error correction is performed exclusively in the digital domain, directed only by the magnitude of the sub-sampled error between the main ADC slices and the reference ADC, with the exception of the sample phase. Time-skew correction is similar to clock recovery in that

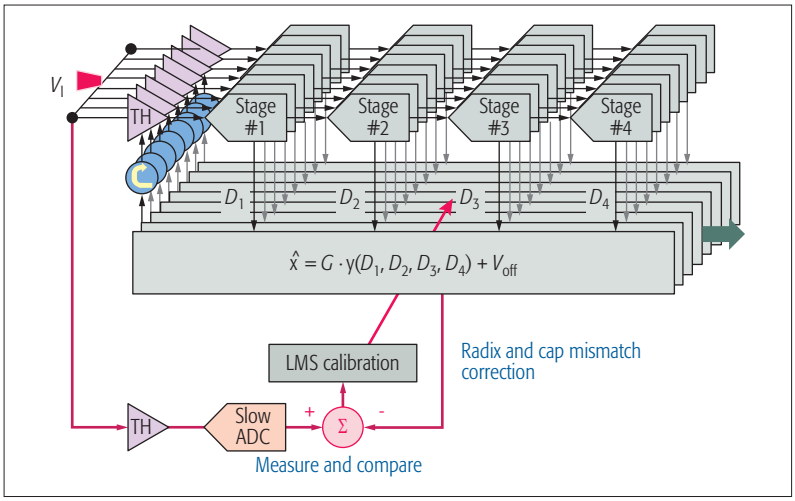

Figure 4. Block diagram of an eight-slice time-interleaved pipelined ADC using a system identification (SI) slow ADC for a reference for full background calibration. The gain, time skew, and offsets are also corrected so that all slices appear identical and uniformly spaced in time.

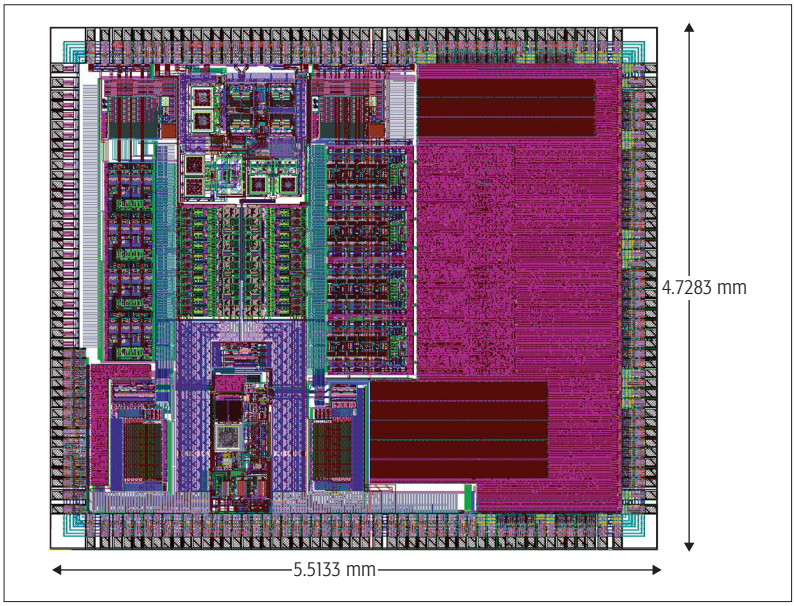

Figure 5. Layout of a 2.5 GS/s 12-bit ADC with 75 dB SFDR through the first Nyquist zone and 62 dB through the third Nyquist zone. All digital circuitry is included to perform background calibration. An 8 kS memory is used to aid in data capture for benchtesting. The chip measures 4.5 mm × 4.7 mm and is fabricated in IBM's 8HP 130 nm BiCMOS process.

information about both magnitude and direction are necessary. Here, a hybrid approach is used to determine direction, which is a combination of a small additional analog block with the digital circuitry [12]. The LMS engine then drives a digital code, which in turn adjusts the edge position of eight capacitive clock-delay DACs, thus closing time-skew correction in the analog domain.

A measured 8 kS spectrum of the ADC with a 2.525 GHz external sample clock and an input near $f_s/5$ is shown in Fig. 6. An SFDR of 75 dBc is achieved, and is limited by the third harmonic of the input buffer and track and hold. The SFDR drops to 62 dBc for a 3.225 GHz input in the third Nyquist zone. The SNR of the ADC is 62 dB at low frequencies. At intermediate frequencies the SNDR is solely a function of the

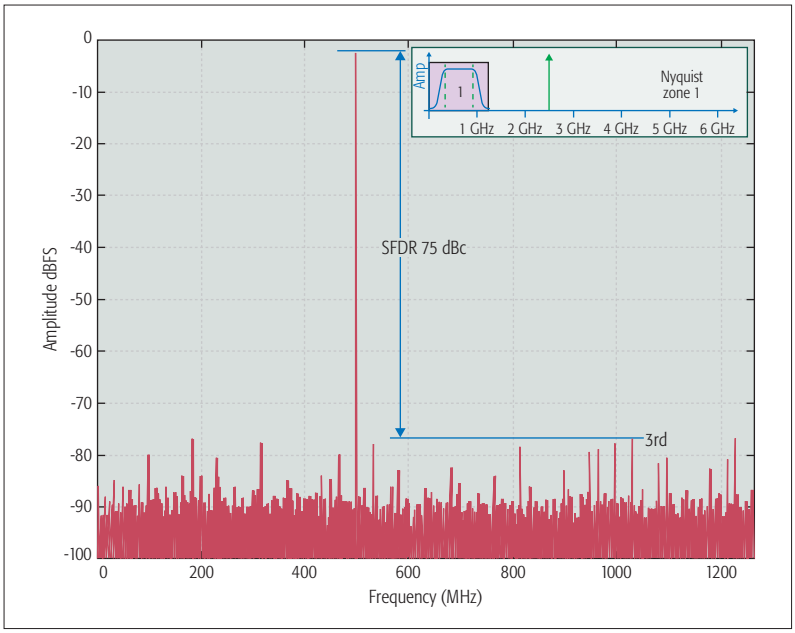

Figure 6. Measured frequency response with an 8 kS fast Fourier transform (FFT) for an input in the first Nyquist zone, f_{in} = 498 MHz, and f_s = 2.525 GS/s.

relative aperture jitter between the clock and the input signal: beyond the second Nyquist zone SNDR is also impacted by the HD_3 of the front-end.

Architecture Considerations and Limitations

When throughput requirements dictate that interleaving be used, the primary observations impacting the design choices involve evaluating how various error sources affect the system and identifying whether those errors are additive or multiplicative. For broadband applications like cable TV, errors due to "smooth" distortion, gain mismatch, and nonuniform sampling can be relaxed significantly (~2 bits) because they are multiplicative errors. Relaxing front-end distortion enables the use of fewer samplers as desensitizing system performance to nonlinearity means that hold time need not be extended to improve accuracy. Using four samplers is a good approach tailored to the application as it allows symmetric layout, balanced loading, and simple clock generation. Reference [13] serves as a good example to illustrate the design principles. The number of samplers is minimized in a two-rank sampling network, and a SAR array is used without mismatch calibration.

The design for both the clock and input network can be laid out in a star configuration, thus matching the paths to all four slices as closely as possible. Offsets and gain errors are easy to remove statistically by setting the mean and variance of each slice to that of a master slice. Since the requirement for time skew is relaxed due to its multiplicative nature, several simplifications in the calibration algorithm can be adopted. A coarse correction of any systematic skew could be made during factory test or at startup. Calibration can remain frozen thereafter. Background adjustments are not always necessary as the differential skew between slices will track temperature and voltage changes after initial calibration to well within the target range for a reduced rms, "backed-off," input signal.

Second-Order Effects

Nonidealities in physical implementation result in error sources being both nonlinear and correlated. Although all the primary errors were described as independent sources earlier, additional problems arrise when these errors interact with each other. This leads to issues with global convergence and the LMS loop settling at non-optimal points. Some of these effects are seen in the measured results of Fig. 6 as residual uncompensated errors due to time interleaving that remain even after calibration.

Another reason for incomplete convergence is that that there is always noise in the estimated error which needs to be averaged out. Environmental variables can change before the "slow" reference ADC has enough time to average the error estimates before they drift. There is also limited resolution of the time skew correction circuit (50 f_s step size for skew adjust). Albeit small, the calibrated spectrum of Fig. 6 still shows artifacts of time interleaving that are also commonly seen in other implementations [13] at various levels unless extensive calibration algorithms and dither are used to eliminate them [10].

Kickback: An explanation identified in the laboratory [14] for incomplete convergence of the calibration algorithm is slice-dependent kickback. The kickback on any one slice will be sampled on the successive slices until it completely settles. Any kickback independent of the signal appears as an offset when it is subsampled by the next slice and mixed to f_s/n_{slice}. Signal-dependent kickback appears as a linear filter causing slice-dependent variation in gain and group delay, thus altering gain and skew errors in a frequency-dependent way. This observation was one of the reasons for adopting the third rule as the fewer slices there are, the easier it is to keep kickback under control.

In the design of Fig. 4, the timing adjustments were made in the analog domain. Whenever the time instant moved, the kickback changed because the dynamics of the front-end changed. Not only did this change the timing instant, but via the kickback also changed offsets and altered the frequency-dependent gains and time skews. Therefore, all error sources interact, causing the LMS loop to wander around in a "whack-a-mole" limit cycle trying to converge all errors simultaneously. Interactions of error sources will always prevent the total system error from converging to its ideal value. Adjusting time skews in the digital domain is one way to break this interaction because the front-end dynamics remain unchanged when the timing skew errors are corrected [15].

Conclusion

The capacity for digital signal processing continues to increase, making it advantageous to implement ADC-based receivers in the gigahertz range. Time interleaving has become widespread to meet the demand for ADCs up to 100 GS/s

and beyond. Multiple error sources exist that can be adressed to varying degrees of success using calibration. However, different applications are sensitive to different error sources, so calibration is not always required. Knowing how sensitive each system requirement is to individual nonidealities is critical for choosing the appropriate architecture and optimizing the design.

Pipelined architectures result in fewer slices, which simplifies many issues but likely requires radix calibration to compensate for incorrect gains in the MDAC stages. SAR arrays do not require gain stages or radix calibration, but make clocking and signal distribution more difficult. They also require two-rank sampling, which can result in a noise penalty that is problematic for higher resolutions. As each sampler needs to meet kT/C requirements, the capacitor area increases as the square of the resolution, and SAR arrays grow exponentially after turning the noise-limited corner at about the 10–11-bit level. Additionally, each slice needs an independent lookup table to mitigate mismatch issues when spectral purity is needed, which makes a large array less attractive for high-resolution applications.

Based on experience and observations, pipelined ADCs with few slices are best for frequency-domain applications and high resolution (7–14 bits). SAR arrays are best for low resolution (5–10 bits). For resolutions of 5 bits and below, simple flash converters are an option. The designer's dilemma is at the level of 7–10 bits, where both SAR and pipelined ADCs have merit and drawbacks without a clear separation between one approach over the other. Designer experience, preference, and available process options, along with other factors such as metastability and crosstalk mitigation, may tip the balance toward one approach over the other.

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The designer's dilemma is at the level of 7–10-bits, where both SAR and Pipelined ADCs have merit and drawbacks without a clear separation between one approach over the other. Designer experience, preference, and available process options, along with other factors such as metastability and crosstalk mitigation, may tip the balance towards one approach over the other.