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Calibration and Dynamic Matching in Data Converters

Part 1: Linearity calibration and dynamic-matching techniques

Data converters include digital-to-analog converters (DACs) and analog-to-digital converters (ADCs). Both have evolved from being implemented as board-level circuits to integrated circuits over about the past 40 years, and calibration has been important at every step along the way.

However, data-converter customers have a love–hate relationship with calibration. On the one hand, customers love the improvements in performance, die area, and power dissipation that calibration gives and sometimes conclude that their data converters need calibration. On the other hand, customers hate the restrictions and costs calibration imposes, and other times conclude that their data converters should not use calibration. This conflict is considered below, pointing out the advantages and disadvantages of calibration in various examples.

This topic is split into two articles. In Part 1, calibration of DACs is considered first. Then dynamic element matching (DEM) is described, followed by calibration of pipelined ADCs. The final section gives a summary. Part 2 of this series will cover calibration of time-interleaved ADCs as well as challenges created by background calibration in all these architectures and draw conclusions based on the examples in both articles.

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Calibration of DACs

Figure 1 shows a block diagram of a successive-approximation-register (SAR) ADC. In the figures in this article, thin lines represent analog circuits

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and signals, and thick lines represent digital circuits and signals. The key points are that many ADCs contain DACs in feedback as shown here, and DAC performance often limits the ADC performance. So DAC calibration improves both DAC and ADC performance. Two detailed examples of DAC calibration through the use of factory trimming are considered next.

Laser Trimming

Figure 2 shows the schematic of the last few bits in an *R*-2*R* ladder DAC. The resistors are implemented in a thin-film layer above all the usual layers in the integrated circuit. Under ideal conditions, each vertical resistance is $2R$, and each horizontal resistance is R. Also, the termination current I_T is ideally equal to the least significant bit current I_N. Ideally, $I_{N-1} = 2I_N$, $I_{N-2} = 2I_{N-1}$, and so on. In practice, variation in the 2/1 resistance ratio changes these currents and causes DAC nonlinearity.

In 1976, laser trimming was used to improve the linearity [1]. At each step in this laser-trimming process, the output current for one of the bits is compared to the sum of all the output currents to its right. For example, I_{N-1} should be equal to $I_N + I_T$. If $I_{N-1} < I_N + I_T$, the laser is applied to resistor R_N, increasing its resistance and voltage drop, which in turn increases I_{N-1}. On the other hand, if $I_{N-1} > I_N + I_T$, the laser is applied to $2R_{N-1}$, increasing its resistance and reducing I_{N-1}. The key point is that this algorithm requires only a single pass, starting on the right and moving to the left to improve the linearity. The drawbacks of laser trimming include the facts that it requires a laser and a thin-film process.

Fuse Trimming

One way to avoid these drawbacks is to use fuse trimming. In 1982, fuse trimming of metal-link fuses blown at wafer sort was used to reduce the offset of a comparator [2]. Blowing fuses at wafer sort uses high-voltage pulses introduced by probe pads [3]. Since the probe pads occupy a large die area, they limit the number of fuses that can be programmed this way. In [3], the authors discovered that fuses made of polysilicon can be blown by low-voltage pulses, less than their junction breakdown, allowing the pulses to be introduced after packaging and sent to the desired fuse by on-chip addressing. So probe pads are not required in this case. However, fuses built and blown this way may not become completely open circuits.

Figure 3 shows the schematic of a fuse amplifier that overcomes this problem [3]. It has two fuses, R_0 and R_1. One of these fuses is blown by turning on M_0 to blow R_0 or by turning on M_1 to blow R_1. The circuit has cascodes connected to V_{BIAS1} and V_{BIAS3}, an *n*-type cascode current mirror, and an output inverter. Because of the cascodes, the impedance at the inverter input is high. When R_0 is blown, small current flows in the left branch and is copied to the right. So R_1 pulls the inverter input high. When R_1 is blown, large current flows in the left branch and is copied to the right, pulling the inverter input low. The key point is that R_0 and R_1 are compared to each other in this way, so the fuse that is blown does not have to become an open circuit for the fuse amplifier to produce a valid logic output level, which can be used to make an analog adjustment in the data converter under calibration.

In practice, an extra fuse can be blown after the trimming is complete to prevent accidentally blowing fuses

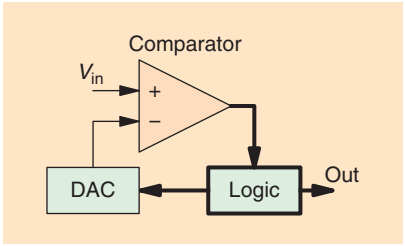

FIGURE 1: A block diagram of a SAR ADC.

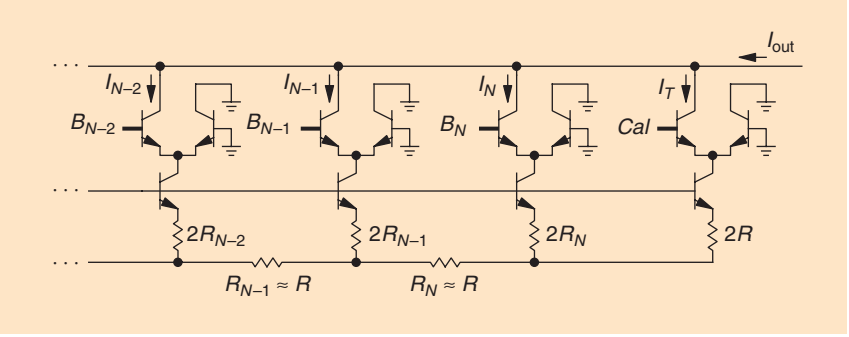

FIGURE 2: A schematic of the last 3 bits in an *R*-2*R* ladder DAC with laser trimming.

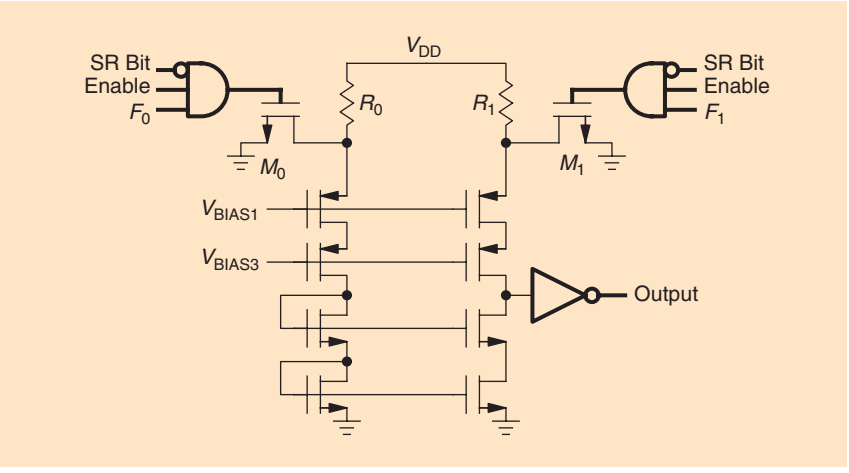

FIGURE 3: A schematic of a fuse amplifier for fuse trimming.

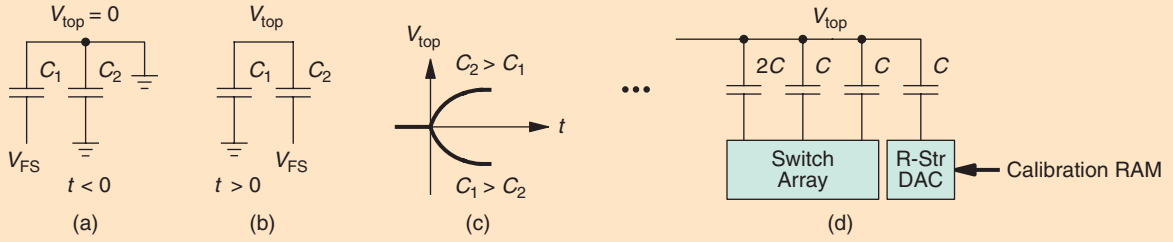

FIGURE 4: (a) Preparing to compare C_1 to C_2 in a SAR ADC, (b) comparing C_1 to C_2, (c) a plot of V_{top} versus time, and (d) using a resistor-string DAC to correct errors from mismatch.

in the field. Instead of fuses, electrically erasable programmable read-only memory (EEPROM) is often used nowadays in processes that support it. Finally, data-converter customers usually like factory trimming because the vendors do the work and guarantee the performance.

Analog Foreground Calibration of Capacitor Mismatch in a SAR ADC

In 1984, a technique that is now called analog foreground calibration was described [4]. A related technique was independently developed [5]. The problem was that the capacitors in a SAR ADC may mismatch. The proposed solution was to compare capacitances that are supposed to match and use analog adjustments to correct the errors. Figure 4 shows that the calibration starts by comparing the most-significant-bit (MSB) capacitance C_1 to the capacitance from the rest of the array C_2. At first, the top plates are grounded, and the bottom plates are connected as shown in Figure 4(a). Then the top plates are floated, and the bottom-plate connections are reversed, as shown in Figure 4(b). Ideally, the top-plate voltage stays at zero, but Figure 4(c) shows that V_{top} becomes positive if $C_2 > C_1$ and negative if $C_1 > C_2$. To correct the error, a resistor-string DAC is introduced in Figure 4(d). Its output is connected to the top plate by another capacitor. The code required to produce the output of the resistor-string DAC that drives V_{top} as close as possible to zero is stored in a calibration random-access memory (RAM), and the process is repeated for the capacitance of the next bit and so on until other errors limit the performance. This calibration must be done at power up because the calibration RAM is erased at power down. Also, this process can be repeated any time the customer is willing to interrupt the conversion to do calibration. As a result, this process can track environmental changes, for example, stemming from changes in temperature, supply voltage, and aging, that are not tracked by factory trimming. This process is called foreground calibration because it brings calibration to the fore, interrupting the usual use of the ADC to digitize its input. Foreground calibration does not require lasers or nonvolatile memory such as fuses. Also, it does not require special fabrication or test equipment. However, customers do not necessarily like foreground calibration because it does require their attention and intervention.

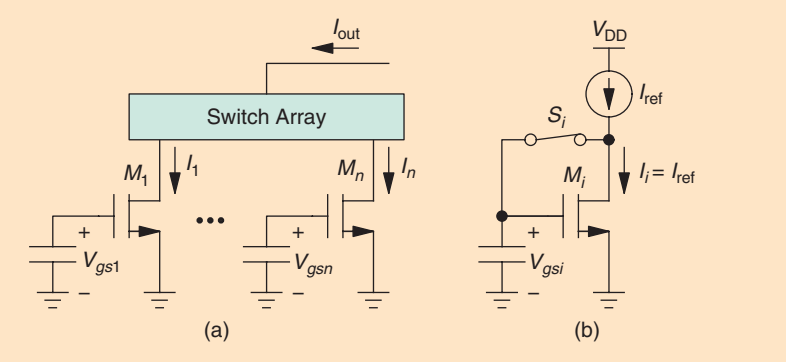

FIGURE 5: Analog background calibration of current mismatch in a unit-element DAC.

Analog Background Calibration of a Unit-Element Current-Source DAC

Figure 5(a) shows a unit-element current-source DAC that uses analog background calibration [6]. Ideally, $I_1 = \ldots = I_n$. If the gates of M_1 through M_n are connected to each other, transistor mismatch can cause errors in the currents and DAC nonlinearity. Therefore, the gates are not all connected together. Instead, Figure 5(b) shows that one transistor at a time (M_i where $1 \le i \le n$) is connected outside the array in a negative feedback loop by turning on switch S_i, forcing it to conduct reference current I_{ref}. Then switch S_i is opened, and the gate voltage of M_i is held almost constant by the gate capacitance, so M_i continues to conduct a current nearly equal to I_{ref} when M_i is put back in the array. For N-bit resolution, $n = 2^N$ current sources are used, which is one more than would be required without calibration. As a result, one transistor can be in calibration while the others are all available to produce the required DAC output. Therefore, this calibration can happen during normal conversion, which means that this work is an early example of what is now called analog background calibration. In this form, customers often like background calibration because it does not require much in the way of

their attention or intervention. However, customers do not necessarily like other forms of background calibration, as described later.

Digital Foreground Calibration of DAC Errors

Figure 6 shows a block diagram of a delta-sigma modulator that uses an erasable programmable read-only memory (EPROM) to digitally calibrate the feedback DAC [7]. The gain around the feedback loop is designed to be high at low frequencies. Because this gain is high and the feedback is negative, the average DAC output is forced to be essentially equal to the average V_{in}. As a result, the inverse of the DAC nonlinearity appears at the analog-to-digital subconverter (ADSC) output for low input frequencies. Therefore, if the EPROM is programmed to have the same nonlinearity as in the DAC, the output of the EPROM is a linear function of the input.

To program the EPROM, the loop is reconfigured as a single-bit delta-sigma modulator, which is inherently linear [8]. The input to that loop comes from the DAC to be calibrated. The calibration operates entirely in the digital domain on the output of the ADSC. Also, the calibration does not change the operation of the loop once the EPROM is programmed until it needs to be programmed again. As a result, this work is an early example of on-chip digital foreground calibration.

A big advantage of digital calibration is that process scaling increases the speed and reduces both the area and power dissipation of digital circuits. Furthermore, process scaling has reduced power-supply voltages, increasing errors in analog circuits by reducing the available headroom. Together, these characteristics have created an opportunity to design data converters that rely less on the raw performance of analog circuits and more on the capability of digital circuits (which carry out calibration algorithms). Other advantages and disadvantages of digital calibration will be described in Part 2 of this series.

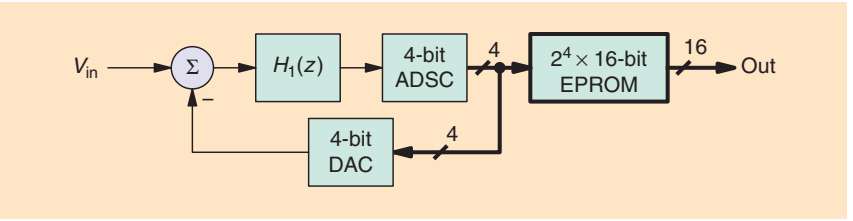

FIGURE 6: Digital foreground calibration of element mismatch errors in the DAC in a delta-sigma modulator.

Dynamic Element Matching

Another way to overcome mismatch is to employ dynamic element matching (DEM) [9]. Figure 7 shows a current source I and a current mirror that produces two outputs, I_1 and I_2, each ideally equal to $I/2$. Switches controlled by a clock connect I_3 and I_4 to I_1 and I_2, respectively, for half the clock period and then reverse the connection for the other half. As a result, $I_3 = I_4$ on average even if $I_1 \neq I_2$, provided that the clock period is divided into two equal halves.

Dynamic element matching has become important in delta-sigma converters because they use oversampling, which gives an opportunity to do the required averaging. Figure 8 shows a block diagram of a 3-bit DAC with DEM [10]. The nth output level is produced by turning on n unit elements. Dynamic element matching is implemented by the randomizer. It selects the elements randomly, decorrelating their selection from the DAC input, and converting the nonlinearity that would otherwise appear from element mismatch into white noise, which can be attenuated by filtering.

Individual level averaging (ILA) is an improvement on this technique [11]. With ILA, the unit elements are not picked randomly but sequentially, starting with the element that was last used longest ago. Also, the

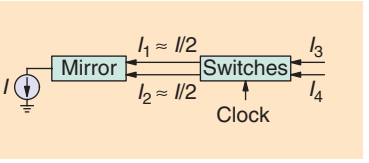

FIGURE 7: Dynamic element matching.

starting point is separately maintained for each output level. Unfortunately, ILA allows short bursts of repeated errors when the input code is changed [12].

Data-weighted averaging (DWA) overcomes this problem [12]–[14]. The concept of DWA is the same as with ILA except that the starting point for using the unit elements is maintained collectively for all the output levels instead of individually for each output level. Figure 9 shows the concept with a 3-bit DAC whose first input is code 6 and whose next input is code 3. To represent code 6, the first six current sources are connected to the output in Figure 9(a). Then to represent code 3, the next three current sources are selected in Figure 9(b), with the selection rolling back to the first element. The key point is that the errors cannot repeat until all the elements have been used. This rotation of the unit elements by DWA shapes the power spectral density, moving the error from mismatch away from baseband to high frequency, as shown in the red plot in Figure 9(c).

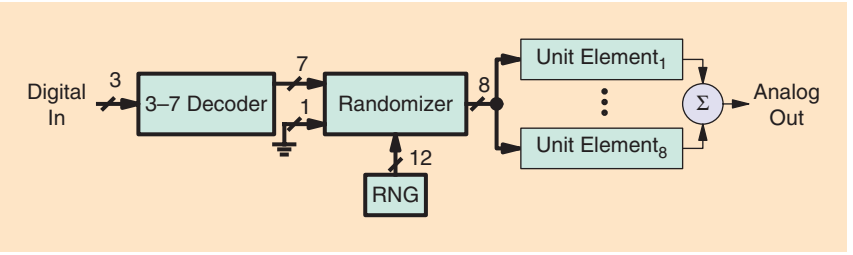

FIGURE 8: Dynamic element matching in a delta-sigma DAC.

A big advantage of digital calibration is that process scaling increases the speed and reduces both the area and power dissipation of digital circuits.

In contrast, the DAC errors generate low-frequency tones with fixed switching as shown in blue, and random switching converts the errors to white noise as shown in green.

Calibration of Pipelined ADCs

Figure 10 shows a block diagram of a pipelined ADC with N stages each operating at the sample rate. Each stage except the last contains a low-resolution ADSC, a DAC, and a subtractor that produces the quantization error or residue, followed by a sample-and-hold amplifier (SHA) with fixed gain. A key point is that the stage input is represented in hybrid form at the output, with a digital component d_1 and an analog component V_{o1}. This arrangement allows pipelined ADCs to be highly tolerant of offset errors provided that they use redundancy and digital correction techniques, which have been around for decades [15]–[20]. In this case, the main performance limitations in pipelined ADCs come from interstage gain errors and DAC nonlinearity.

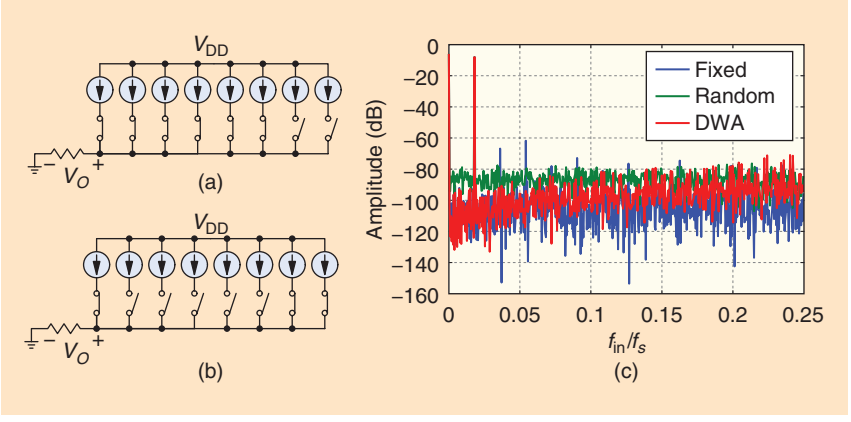

FIGURE 9: (a) A 3-bit DAC with data-weighted averaging (DWA) uses the first six current sources when the first input is code = 6. (b) The same DAC uses the next three current sources when its next input is code = 3. (c) A plot of the magnitude spectra with DWA (red), fixed switching (blue), and random switching (green).

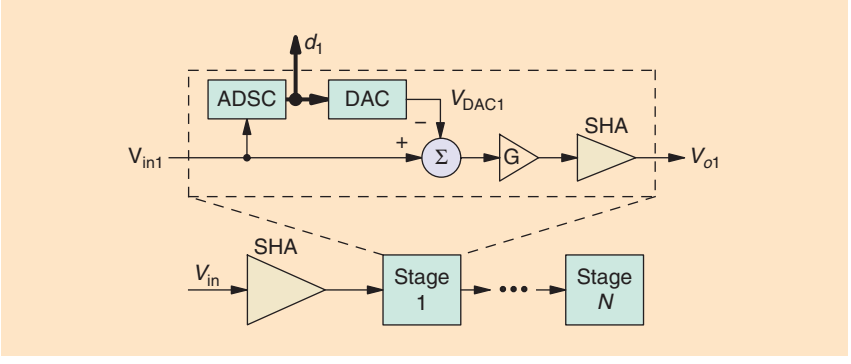

FIGURE 10: A block diagram of a pipelined ADC.

Alternatives to Calibration

Interstage gain errors can be reduced by error averaging [21]. This technique uses a preamplifier, a postamplifier, and three clock phases. Figure 11 shows simplified schematics of the preamplifier during each phase. The postamplifier is ignored for simplicity. Assume that the op amp is ideal. On ϕ_1, the input V_{in} is sampled onto both C_1 and C_2, which are matched capacitors in practice. On ϕ_2, the charge that was sampled on C_2 is transferred to C_1. The resulting op-amp output is $V_{x2} = [1 + (C_2/C_1)]\,V_{in}$. If $C_1 = C_2, V_{x2} = 2V_{in}$, but capacitor mismatch causes a gain error. On ϕ_3, the charge that was on C_1 is transferred to C_2, and the op-amp output is $V_{x3} = [1 + (C_1/C_2)]\,V_{in}$. Capacitor mismatch causes V_{x2} and V_{x3} to move in opposite directions so that $V_{x2} > V_{x3}$ or vice versa. Since these changes are almost equal in magnitude, using a postamplifier to average V_{x2} and V_{x3} greatly reduces the error caused by capacitor mismatch. Note that error

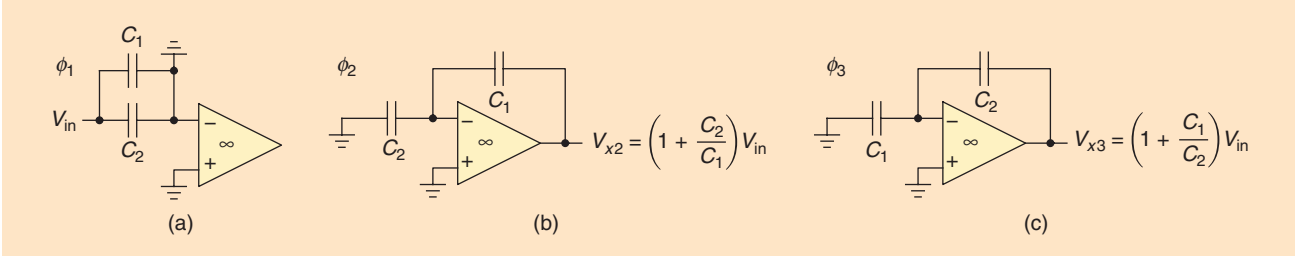

FIGURE 11: The preamplifier in an error-averaged amplifier: (a) during ϕ_1, (b) during ϕ_2, and (c) during ϕ_3.

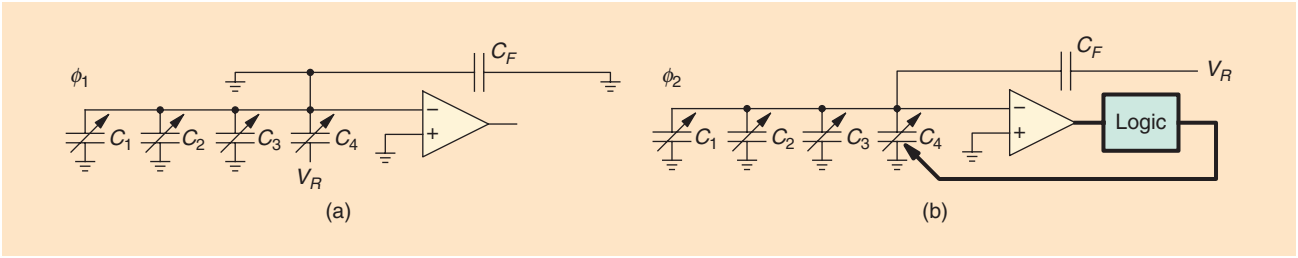

FIGURE 12: Simplified schematics of a pipelined ADC stage with foreground calibration for DAC nonlinearity: (a) during ϕ_1 and (b) during ϕ_2.

averaging is an example of dynamic element matching.

In practice, finite op-amp gain in the preamplifier reduces both V_{x2} and V_{x3}; therefore, this error is not reduced by averaging. As a result, the open-loop op-amp gain in the preamplifier must be large enough by design to make this error negligible in practice.

The main disadvantage of error averaging is that it requires three clock phases instead of only two, so it reduces the maximum conversion rate by a factor of 1.5. Ratio independent gain [22], reference refreshing [23], and correlated double sampling [24] are additional techniques that overcome other important errors, but they all require extra clock phases too. A key point here is that customers like these techniques because they overcome the significance of errors that could otherwise limit the performance and do not require the customer's attention or intervention.

Analog Foreground Calibration in Pipelined ADCs

In 1991, analog foreground calibration was used to overcome DAC errors in a pipeline stage [25]. Figure 12 shows simplified schematics of the analog part of a stage during calibration. The DAC consists of four sampling capacitors $C_1 - C_4$, and mismatch among these capacitors can cause the DAC to be nonlinear. To overcome this problem, a capacitive trim array is added in parallel to each of these capacitors, and the capacitance of each capacitor plus its trim array is forced to be equal to C_F, the capacitance of the feedback capacitor. Figure 12 shows how this equality is forced for C_4, which is compared to C_F using two clock phases. During ϕ_1, the top plates are grounded, the bottom plate of C_4 is connected to V_R, and the bottom plate of C_F is grounded. During ϕ_2, the top plates are floated, and the connections on the bottom plates of C_4 and C_F are reversed. If $C_4 = C_F$, the top-plate voltage stays at zero. However, if $C_4 \neq C_F$, the top-plate voltage changes as in [4], as described above. This change is sensed by the op amp, whose output goes to a logic circuit that controls the trim array in parallel with C_4 so that C_4 plus its trim capacitance is forced to equal C_F. Then the process is repeated for C_1, C_2, and C_3, eliminating DAC nonlinearity. Note that after foreground calibration has been done, it does not require extra clock phases during normal conversion. As a result, foreground calibration can be used to make faster ADCs than the alternatives to calibration described in the previous section. However, unlike these alternatives, foreground calibration interrupts the conversion of the input to recalibrate and track environmental changes. Also, note that the example described in this section uses digitally enabled analog calibration because the logic controls the trim arrays, which operate in the analog domain.

Digital Foreground Calibration in Pipelined ADCs

In 1993, a pipelined ADC with redundancy and digital correction was completely calibrated in the digital domain [26]. Figure 13(a) shows a block diagram of the front end of the ADC. It consists of the input SHA followed by a 1-bit ADSC, a 1-bit DAC, a subtractor, the next SHA, and so on. The 1-bit ADSC is just a comparator whose threshold is ideally zero. The 1-bit DAC is just some switches that ideally connect to either $\pm V_R/2$. Figure 13(b) shows the transfer characteristic of the pipelined ADC when the entire pipeline is

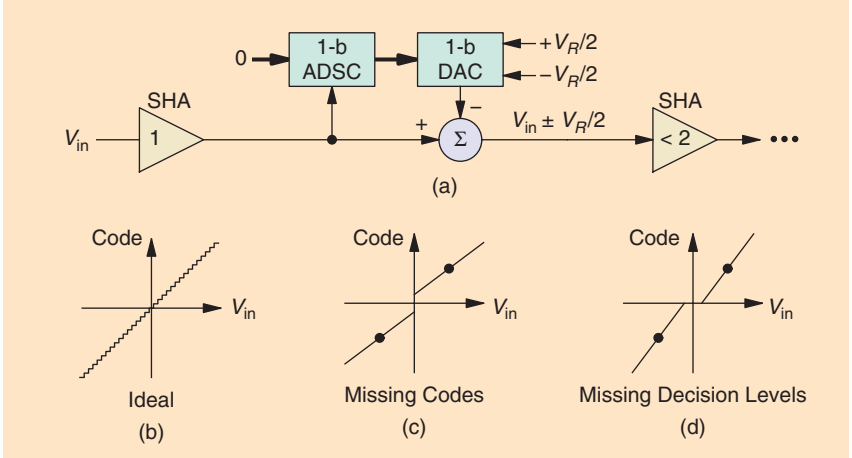

FIGURE 13: (a) A simplified block diagram of the front end of a pipelined ADC with digital foreground calibration, (b) an ideal transfer characteristic, (c) a transfer characteristic with gain < 2 in the second SHA, (d) and a transfer characteristic with gain > 2 in the second SHA.

Dynamic element matching has become important in delta-sigma converters because they use oversampling, which gives an opportunity to do the required averaging.

ideal. Figure 13(c) shows the transfer characteristic when the only error is that the gain of the second SHA is < 2 instead of exactly equal to two. For simplicity, the little steps in the transfer characteristic are ignored here. The two dots are at inputs of $\pm V_R/2$. At these two dots, the codes produced are the same as in the previous case because the input to the SHA with gain error is zero at each of these dots. So the gain error makes no difference to the codes produced at either of these points. However, since the SHA gain is less than ideal, the slope of the transfer characteristic around each dot is less than ideal, causing missing codes at the vertical jump. On the other hand, Figure 13(d) shows the transfer characteristic when the only error is that the gain of the second SHA is > 2. Again, the two dots are in the same locations, but now the slope around each dot is bigger than it should be, causing missing decision levels at the horizontal jump.

With only digital calibration, missing decision levels are an insurmountable problem because digital calibration does not generate or move the decision levels. All it can do is select from the decision levels determined by the analog part of the ADC. To avoid this problem, the interstage gain is set to be < 2, and extra stages are added to introduce redundancy. Then the pipelined ADC can be completely calibrated in the digital domain. This result was a breakthrough because it meant that the calibration circuits could take advantage of scaling predicted by Moore's law [27].

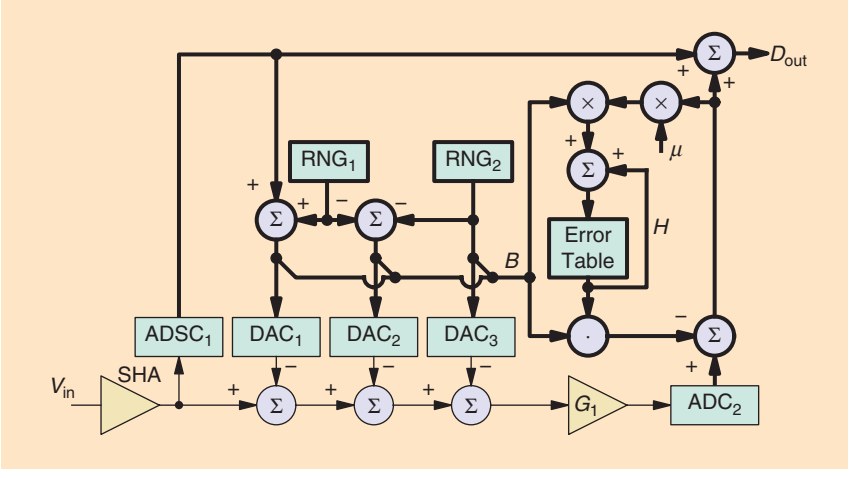

FIGURE 14: A two-step ADC that uses dynamic element matching to calibrate for errors in the first-stage DAC.

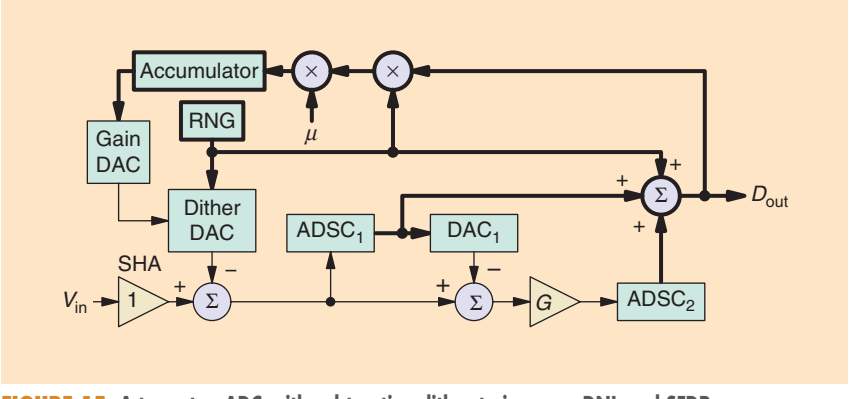

FIGURE 15: A two-step ADC with subtractive dither to improve DNL and SFDR.

Dynamic Element Matching to Enable Background Calibration of DAC Errors in a Pipelined ADC

Figure 14 shows a block diagram of a two-step ADC that uses DEM to background calibrate for DAC errors in the first stage [28]. A related technique was independently developed [29]. The DAC to be calibrated is split into three DACs, whose outputs are summed together. Two independent noise sources are used to make sure that all the DAC input bits except the MSB of DAC_1 are uncorrelated with V_{in} and each other. Each of these noise sources is added and subtracted in the analog domain so neither contributes anything to the residue if the DAC element weightings are ideal. This structure gives DEM, converting mismatch errors in DAC elements into pseudorandom noise. Since this noise is uncorrelated with the ADC input, the errors can be discovered by correlating the DAC input bits B (which does not include the MSB of DAC_1) with the output of the back-end ADC to produce an error table that gives the corrections for the DAC errors. Finally, any uncanceled errors from element mismatch in the DAC appear as noise.

Subtractive Dither with Background Calibration to Improve Differential Nonlinearity and Spurious Free Dynamic Range

Next, consider the use of subtractive dither. Dither is a noise-like signal added to ADC inputs. It was originally used to decorrelate the quantization error from the input, changing fixed

patterns that may have otherwise deteriorated the perceived quality of digitized audio and video communications. Subtractive dither means that a dither signal is added to the input of an ADC and subtracted from its output or vice versa [30]. It can be used not only for its original purpose but also to background calibrate ADCs. Figure 15 shows a block diagram of an early example [31]. It subtracts dither from the input to a two-step ADC and then adds the dither to the ADC output. Subtractive dither smooths out the ADC transfer function, greatly improving the differential nonlinearity and the spurious-free dynamic range. However, if the dither is not completely removed at the output, the dither residue can degrade the signal-to-noise ratio (SNR). For example, nonzero dither residue can result from gain error in the dither DAC and/or the ADC. To avoid this limitation, the digital output can be correlated with the dither and used to adjust the gain of the dither DAC so that the amplitude of the dither injected in the analog domain is chosen to cancel the dither at the output [32], [33]. A disadvantage of this technique is that it reduces the maximum allowed V_{in} because the dither occupies some of the input range of the ADC. To maintain the same SNR as in the case without dither, the input-referred noise of the ADC must be reduced, which significantly increases its power dissipation when the SNR is not limited by quantization noise.

Subtractive Dither to Background Calibrate for Interstage Gain Errors

Also, subtractive dither can be used to background calibrate for interstage gain errors. Figure 16 shows a block diagram of one approach in which the dither is injected at the output of the ADSC [28]. A related technique was independently developed [34]. In this case, the dither is converted to the analog domain by the same DAC that operates on the ADSC output. Then the dither is subtracted from the held input, multiplied by the interstage gain G_1, and converted back to the digital domain by ADC_2. The output of ADC_2 is multiplied by the accumulator output, which weights the bits produced by the second stage relative to those produced by the first stage to compensate for interstage gain error. The weighting factor is $1/\widehat{G_1}$, where $\widehat{G_1}$ is a digital estimate of G_1. Since the dither was subtracted in the analog domain, it is added in the digital domain to the accumulator output. The accumulator operates in a negative feedback loop and adjusts $\widehat{G_1}$, forcing it to converge to G_1. The operation of this loop will be described in detail in Part 2 of this series. The key point here is that when the dither is injected at the output of the ADSC, the required resolution of the DAC increases because each output of the ADSC without dither leads to two inputs to the DAC, assuming the dither is binary valued.

To avoid this problem, Figure 17 shows that the dither can be injected at the ADSC input [35]. The beauty of this technique is that its implementation has low complexity because it does not increase the required DAC resolution. However, a disadvantage of this technique is that it only calibrates for inputs near the comparator thresholds in the ADSC. Another disadvantage is that this technique reduces the redundancy or correction range because introducing the dither at the ADSC input is equivalent to changing the thresholds of the comparators in the ADSC. A similar technique was used to spread out interstage-gain errors in the frequency domain but not to calibrate these errors, improving the spurious-free dynamic range but not the SNR [36].

Also, a redundant residue mode can be used to background calibrate for interstage gain errors [37]. Figure 18 shows two plots of the amplified

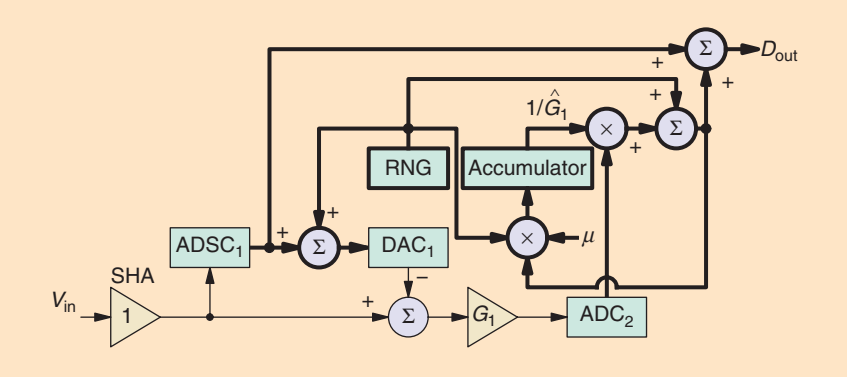

FIGURE 16: A two-step ADC with subtractive dither injected at the output of $ADSC_1$ to background calibrate for error in G_1.

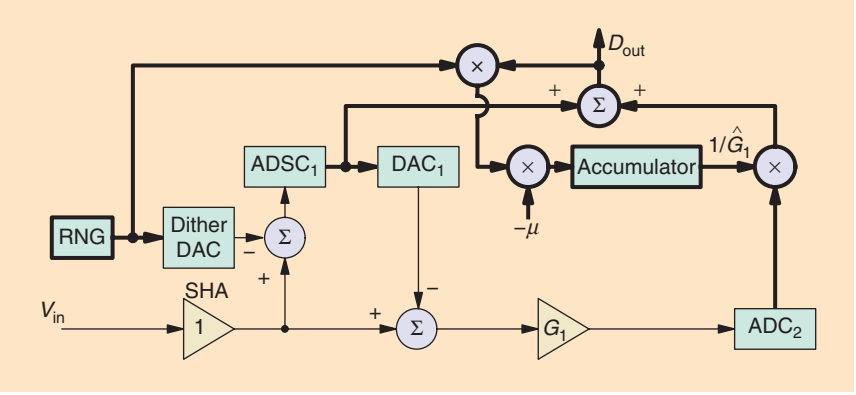

FIGURE 17: A two-step ADC with subtractive dither injected at the input of $ADSC_1$ to background calibrate for error in G_1.

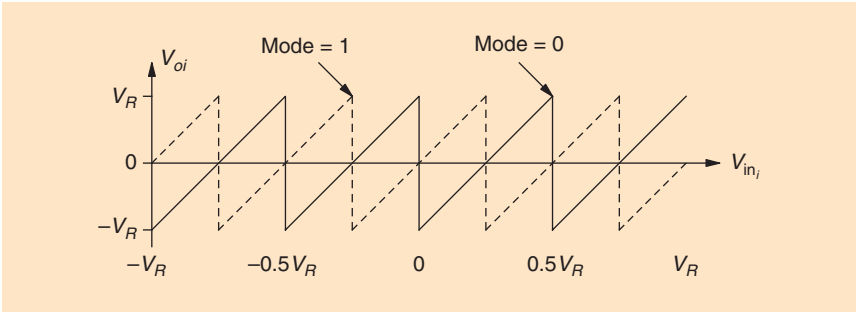

FIGURE 18: Amplified residue versus held input in a stage using two residue modes to do background calibration for interstage gain error.

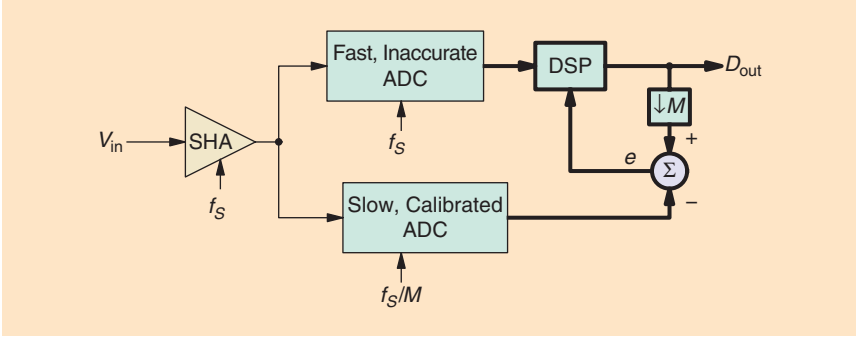

FIGURE 19: A nested calibration architecture.

residue versus the held input in a stage under calibration. The solid plot corresponds to Mode = 0 and has comparator thresholds at the vertical jumps (0 and $\pm V_R/2$) and DAC outputs at the zero crossings in the nonvertical segments ($\pm V_R/4$ and $\pm 3V_R/4$). The dashed plot corresponds to Mode = 1 and requires about one extra bit of resolution to generate because a new set of comparator thresholds and DAC outputs are needed. The introduction of a new residue mode can be viewed as equivalent to adding dither to the ADSC and DAC inputs. Under ideal conditions, the two modes are interchangeable and give identical results. Interstage gain errors are calibrated by measuring the change in the amplified residue that occurs when the mode is changed and the input is constant. To avoid reducing the maximum conversion rate, these changes are measured statistically. When the residue changes from about $-V_R/2$ to about $V_R/2$ (or vice versa), the gain error is measured. Also, when the residue changes from about zero to about $\pm V_R$ (or vice versa), the gain variation is measured. This project background calibrated for both errors. Also, this project started with a commercial product that did not use calibration [38], allowing the results to show that background calibration reduced the required power dissipation. This result is very important because reducing the power dissipation is one of the big goals of using background calibration.

Parallelism to Allow Background Calibration

Figure 19 shows a block diagram of an architecture that uses parallelism to do background calibration [39], [40]. It has an input SHA, a fast but inaccurate ADC in parallel with a slow ADC, followed by a digital-signal processing (DSP) block. Outputs corresponding to the same input are subtracted, producing an error e that is used to calibrate the fast ADC. After calibration, the linearity of the fast ADC is limited by the linearity of the slow ADC. To improve the linearity, the slow ADC can be calibrated also. In this case, the calibration is nested. The input SHA is used to eliminate the effect of timing errors but is not necessary if a layer of timing calibration is added [41]. In practice, the slow ADC is allowed to have high noise and, therefore, can have low power dissipation because its noise can be averaged out in the DSP block as long as the goal is to track variations in the error that only occur slowly, from temperature changes, for example. Also, the slow ADC is allowed to have low resolution as long as its quantization error can be averaged out, which requires using dither for low-enough resolution, where the thermal noise is less than the quantization error.

Summary

In Part 1 of this article series, the calibration of DACs, DEM, and the calibration of pipelined ADCs have been considered. Part 2 will cover calibration in time-interleaved ADCs as well as challenges created by background calibration in all architectures and draws conclusions based on the examples in both parts.

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