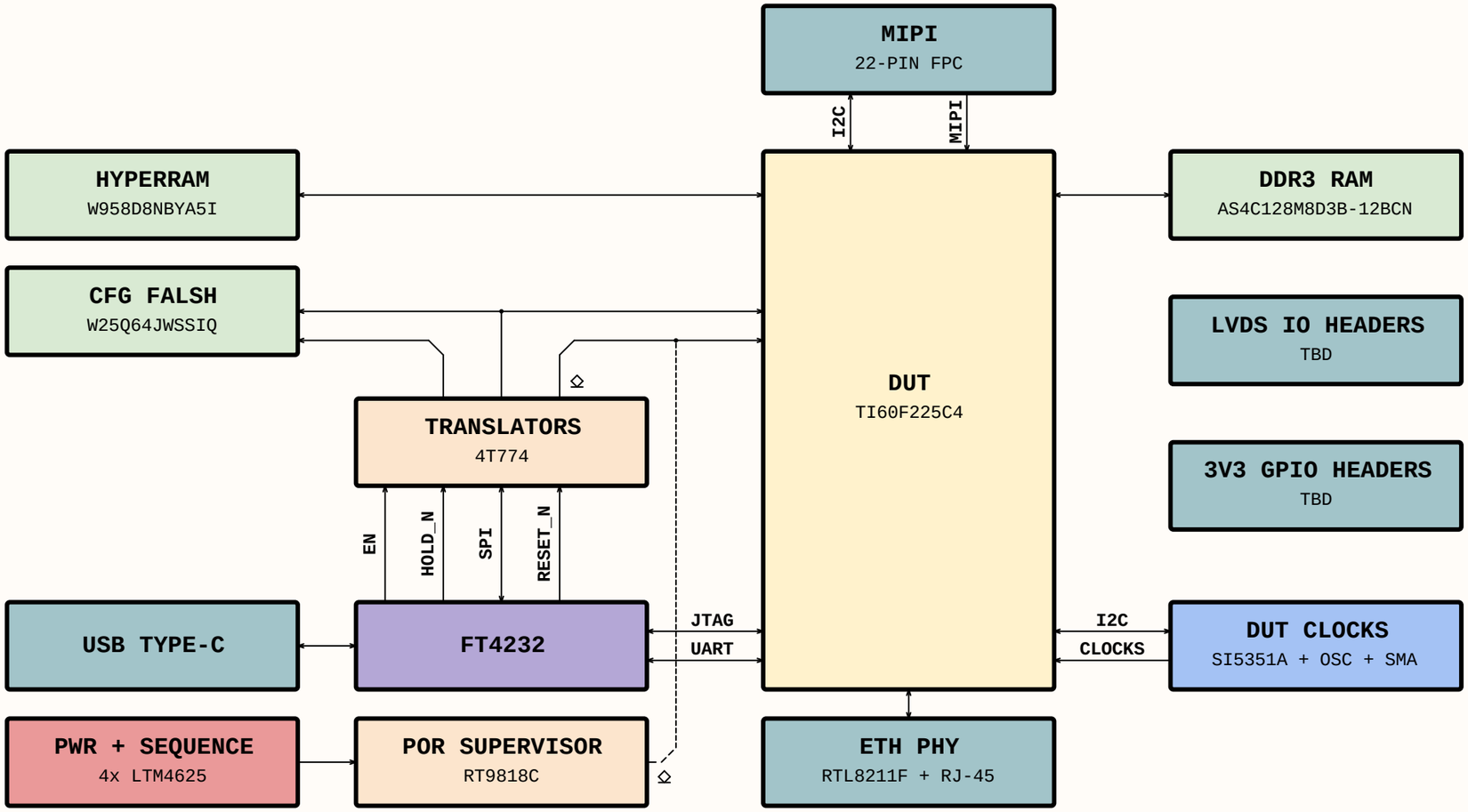
DEVEFX000001A.PrjPcb

01_TOP.SchDoc

LEGEND

- DEBUG
- CLOCKS
- IO
- MEMORY
- DUT
- POWER
- MISC



DEVEFX000001A.PrjPcb

02_RSVD.SchDoc

RESERVED PAGE

DEVEFX000001A.PrjPcb

03_RSVD.SchDoc

RESERVED PAGE

DEVEFX000001A.PrjPcb

04_RSVD.SchDoc

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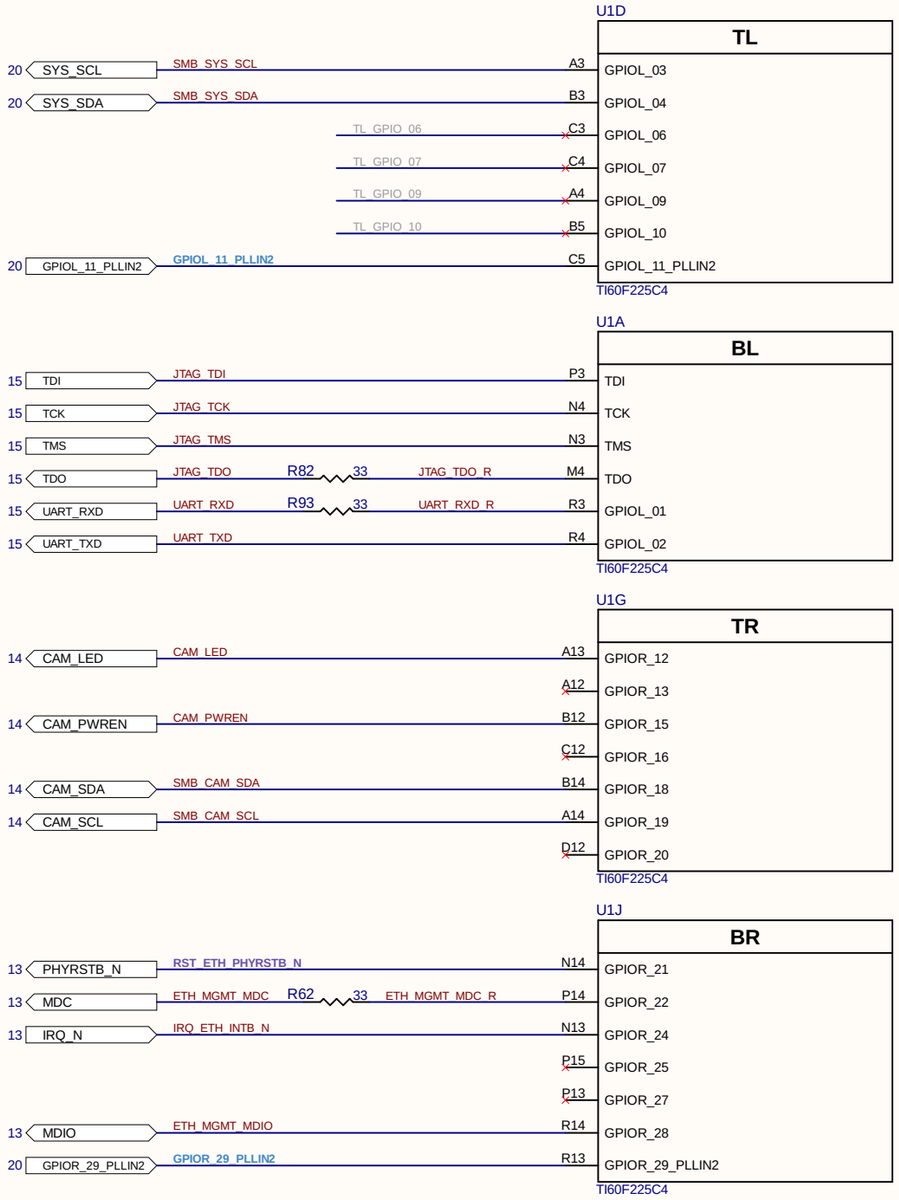
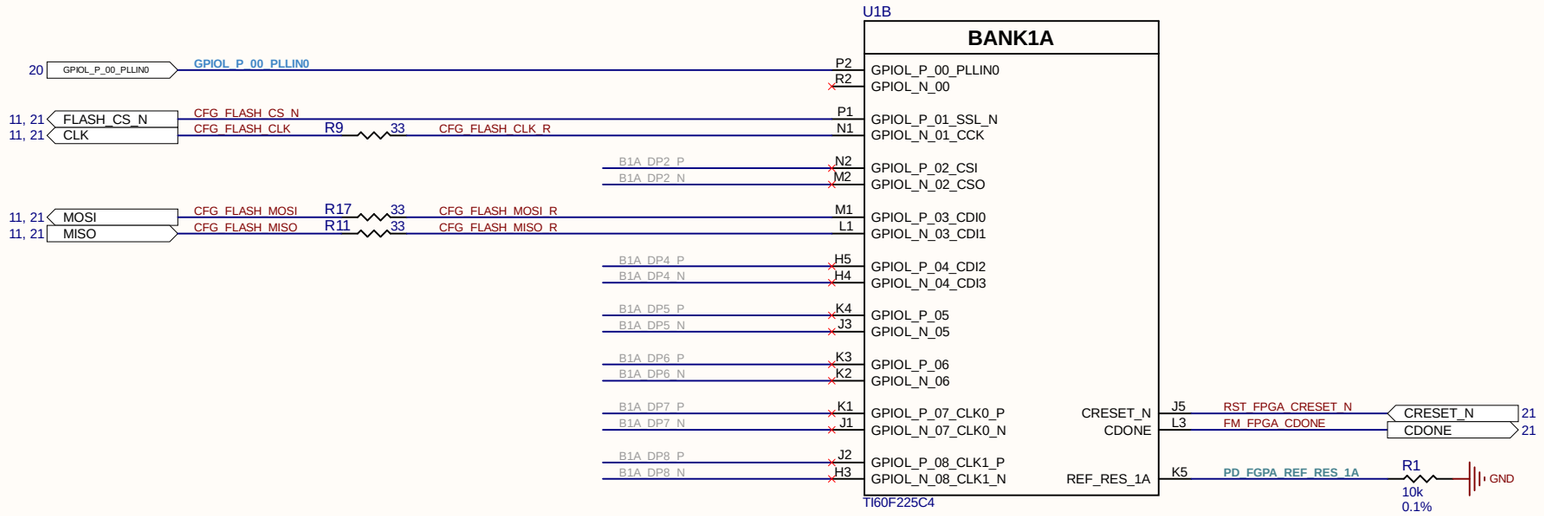
DEVEFX000001A.PrjPcb

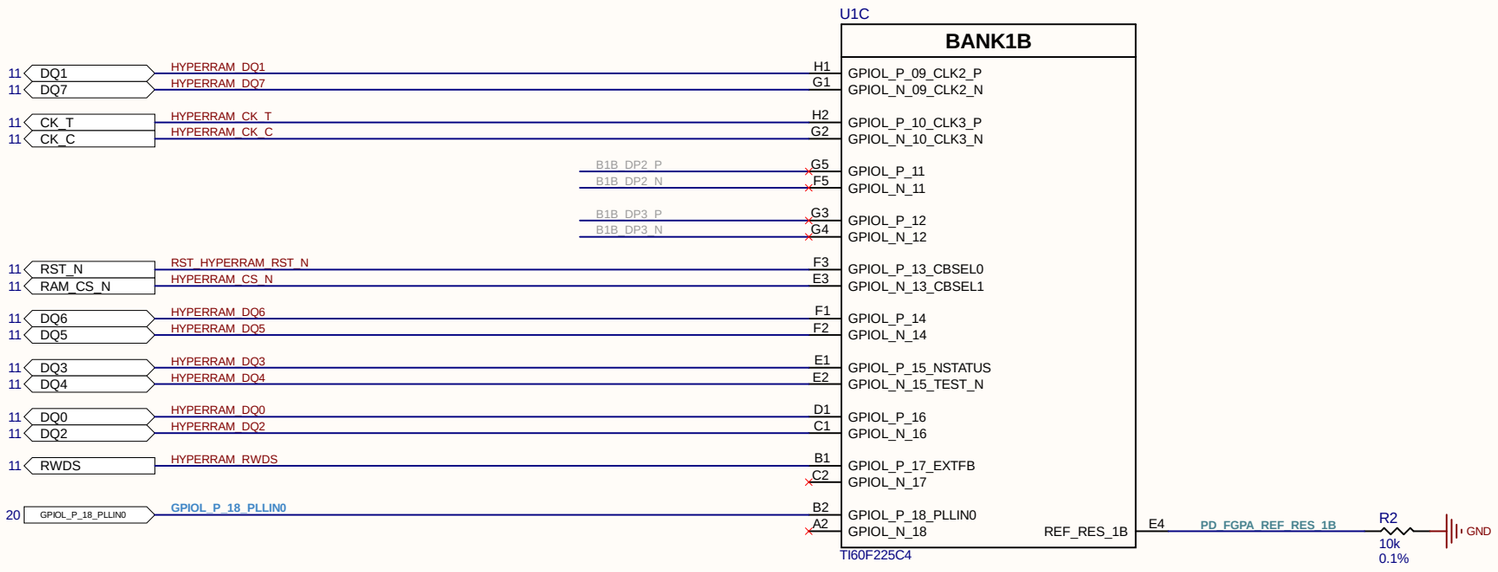
05_FPGA_HVIO.SchDoc



DEVEFX000001A.PrjPcb

06_FPGA_HSIO_B1.SchDoc



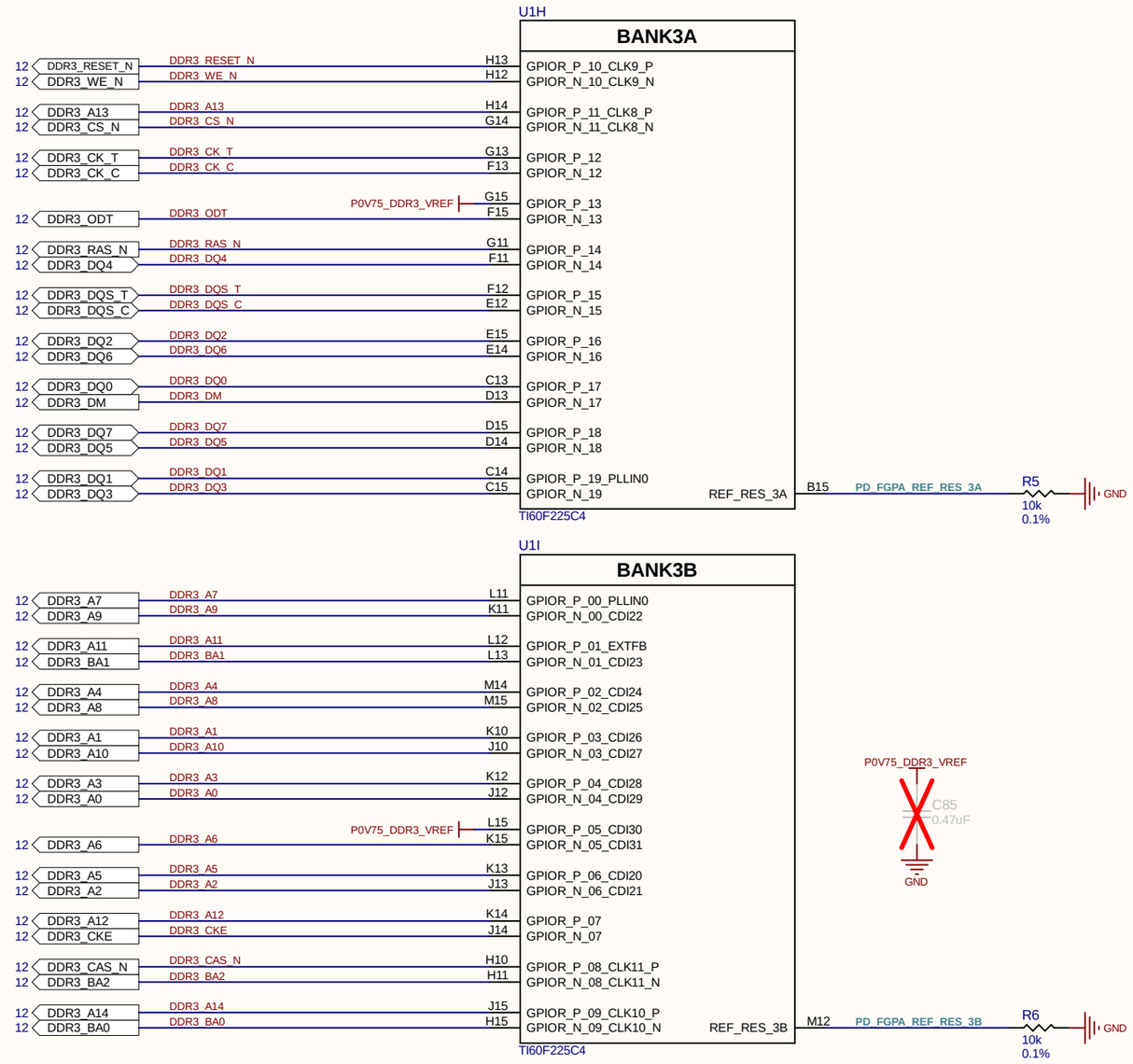


DEVEFX000001A.PrjPcb

07_FPGA_HSIO_B2.SchDoc

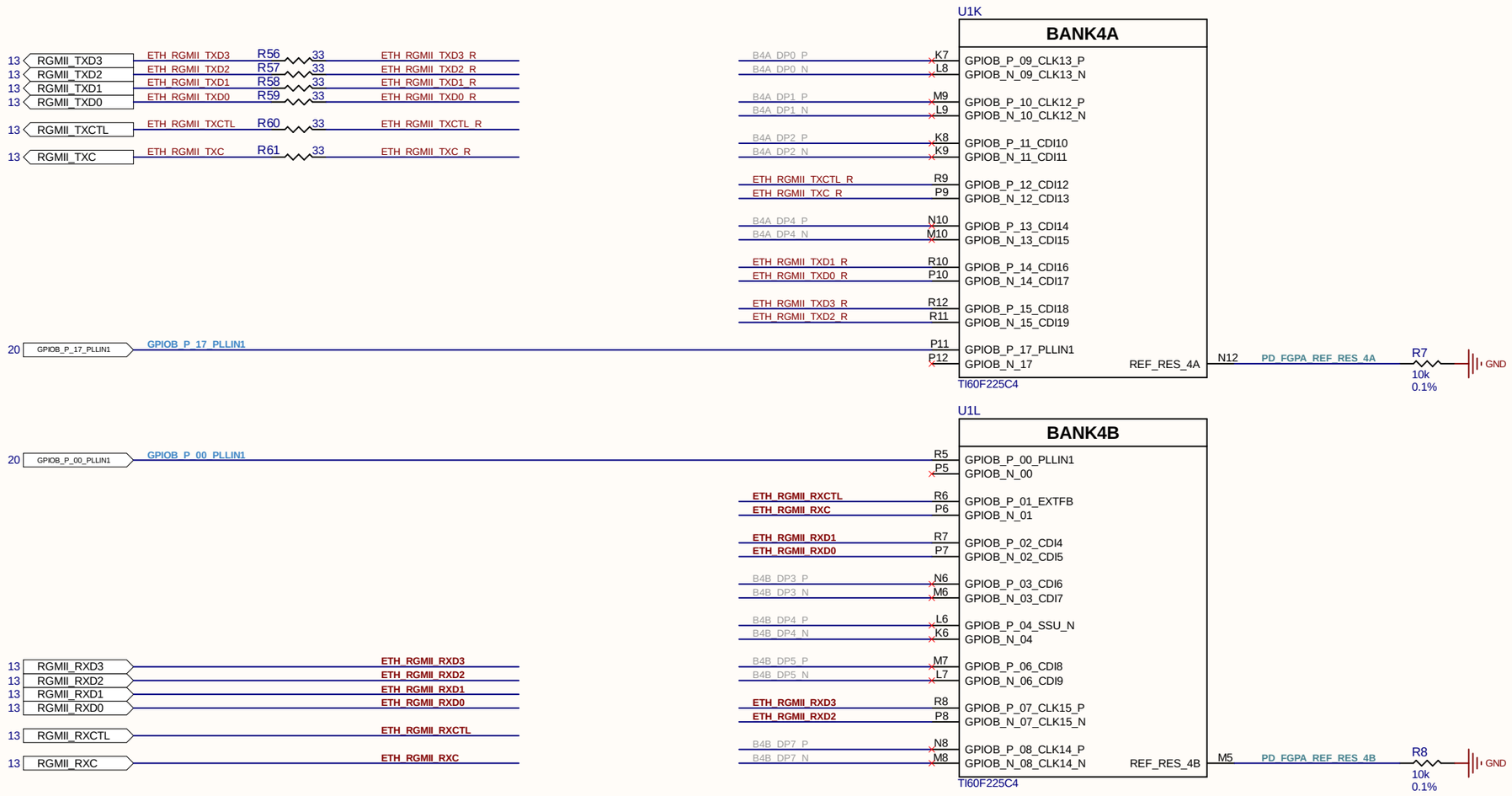
DEVEFX000001A.PrjPcb

08_FPGA_HSIO_B3.SchDoc



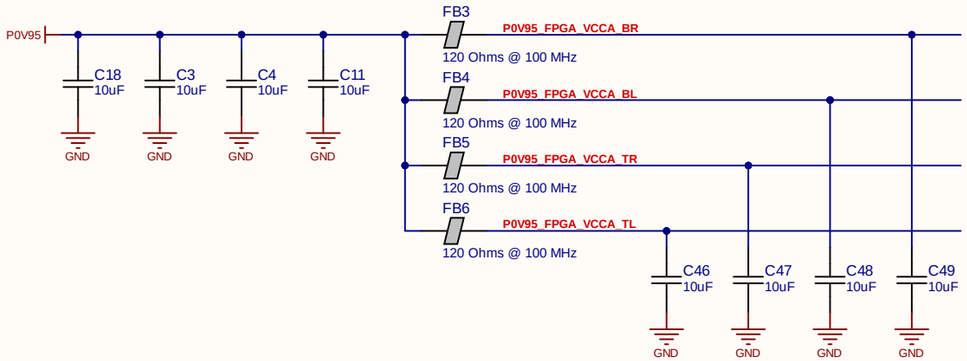
DEVEFX000001A.PrjPcb

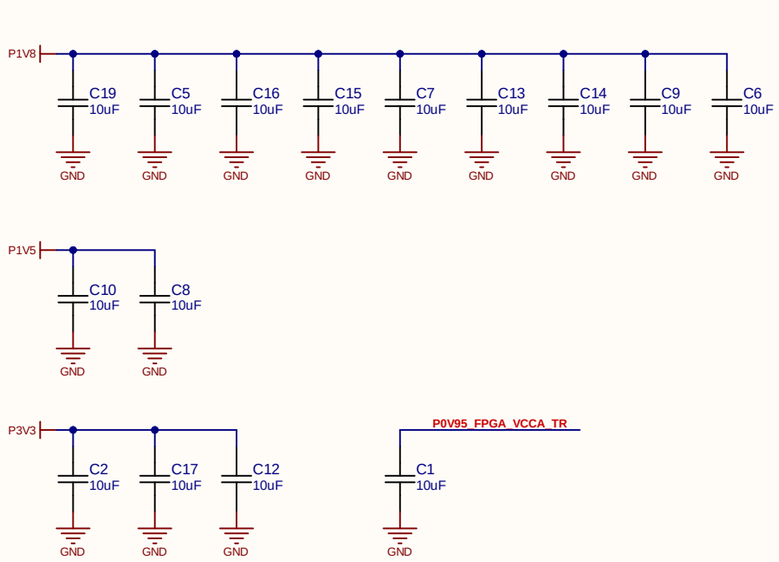
09_FPGA_HSIO_B4.SchDoc

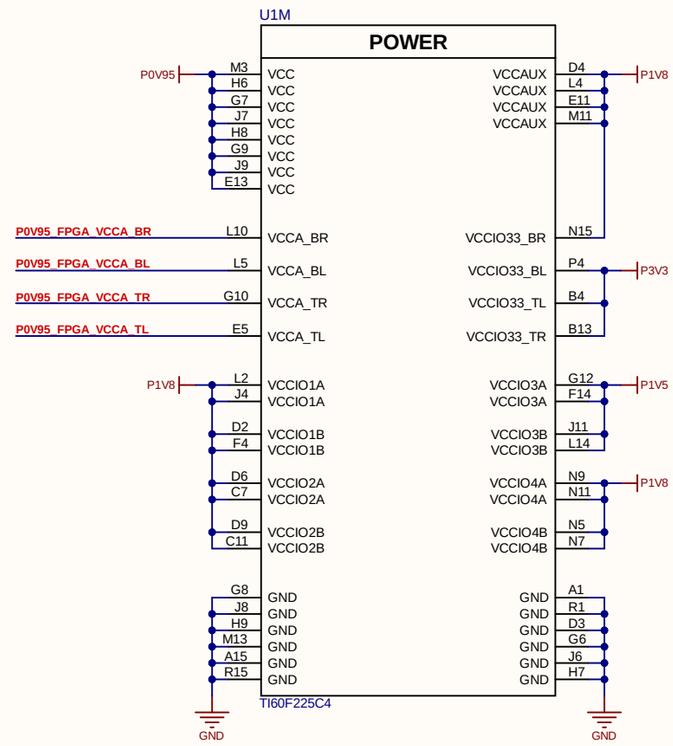


DEVEFX000001A.PrjPcb

10_FPGA_PWR.SchDoc

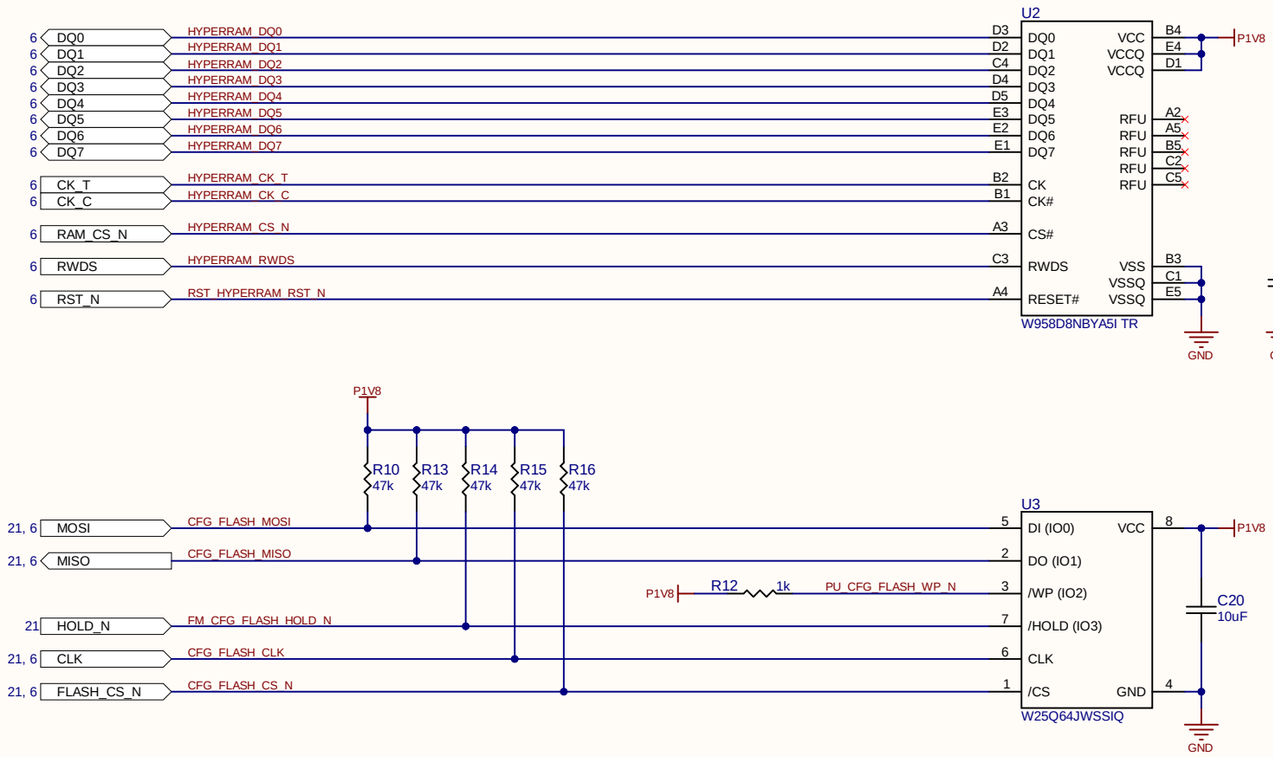






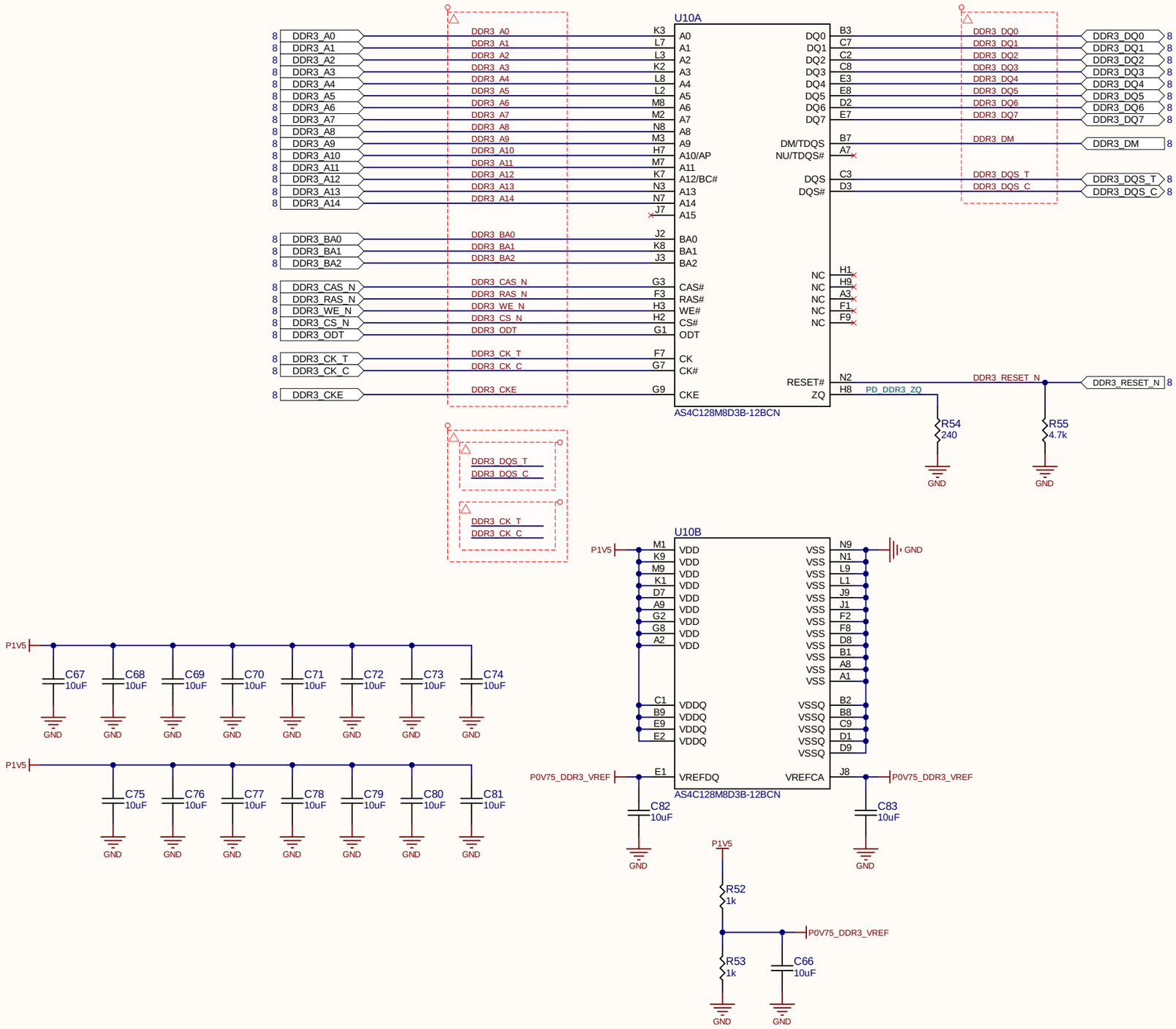
DEVEFX000001A.PrjPcb

11_MEM_HYPERRAM_FLASH.SchDoc



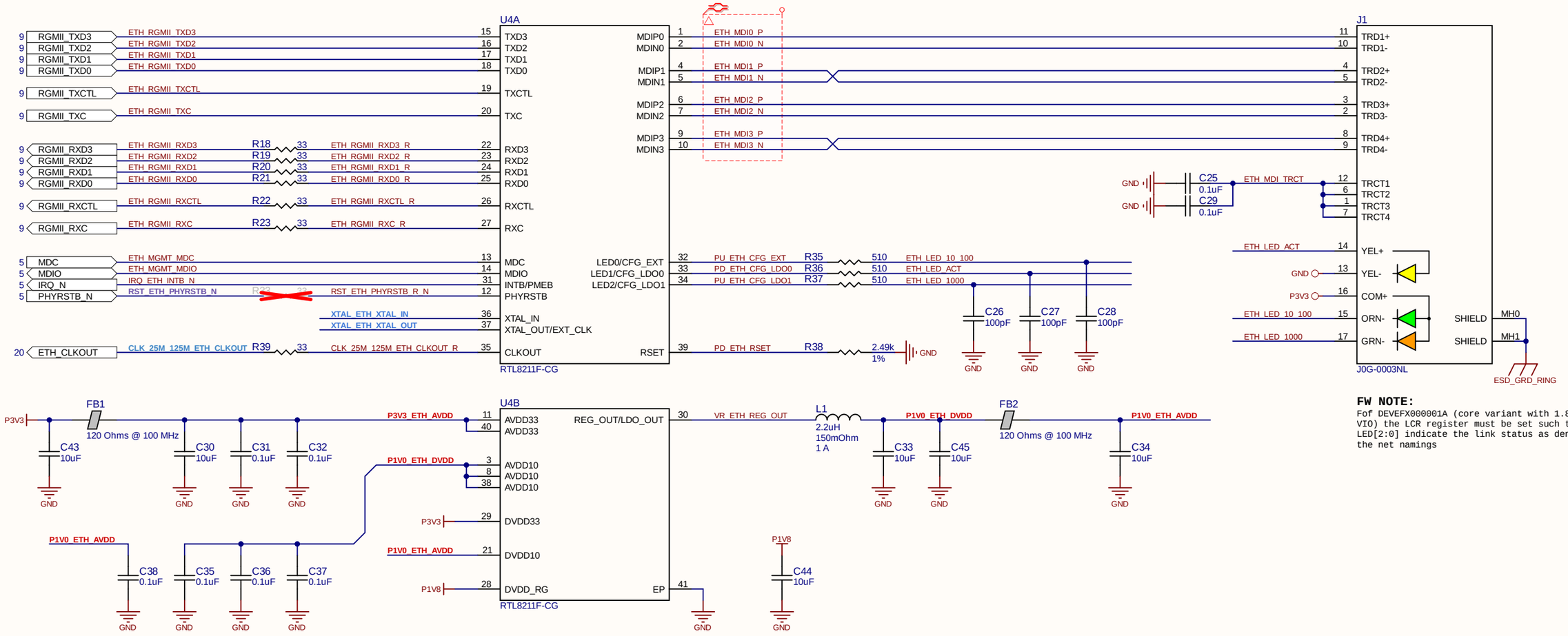
DEVEFX000001A.PrjPcb

12_MEM_DDR3.SchDoc



DEVEFX000001A.PrjPcb

13_IO_ETH.SchDoc



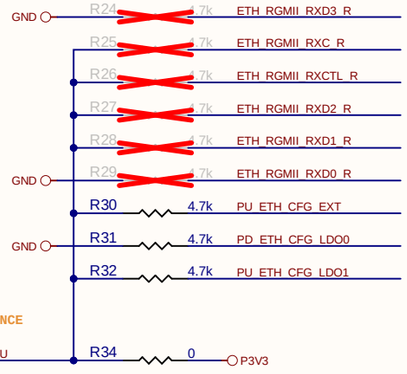
FW NOTE:

Fof DEVEFX000001A (core variant with 1.8 RGMII VIO) the LCR register must be set such that LED[2:0] indicate the link status as denoted by the net namings

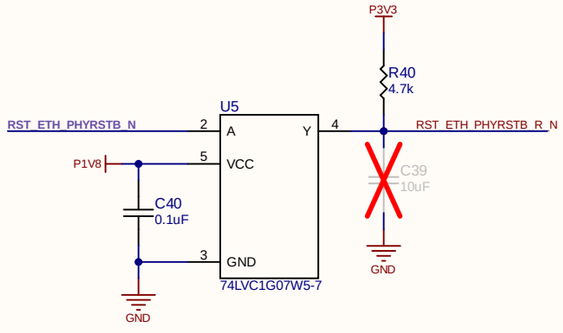
STRAPS

Pin No.	Strap Name	Internal pull
22	PHYAD0	Up
27	PHYAD1	Down
26	PHYAD2	Down
23	PLLOFF	Down
24	TXDLY	Down
25	RXDLY	Up
32	CFG_EXT	Down
33	CFG_LDO0	Up
34	CFG_LDO1	Down

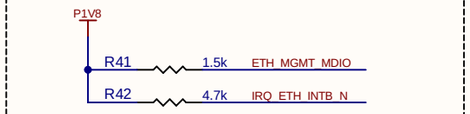
WARNING: BEWARE OF POSSIBLE P3V3 AND P1V8 DOMAIN INTERFERENCE



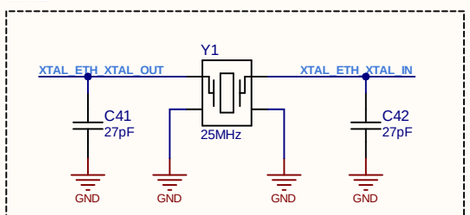
RESET SI



MISC SI

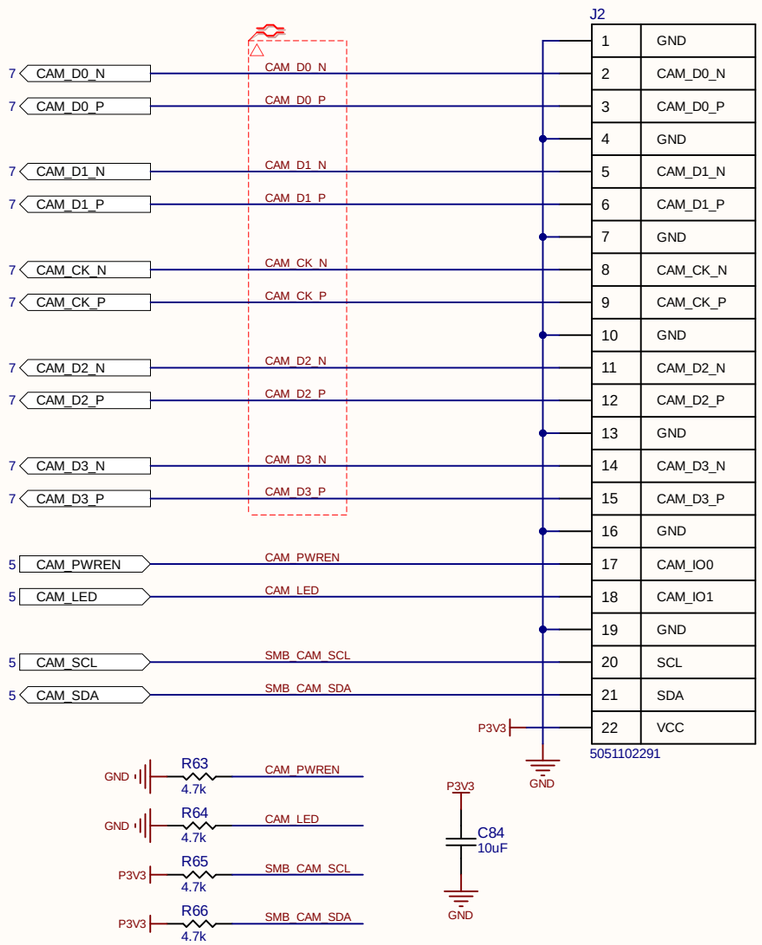


XTAL



DEVEFX000001A.PrjPcb

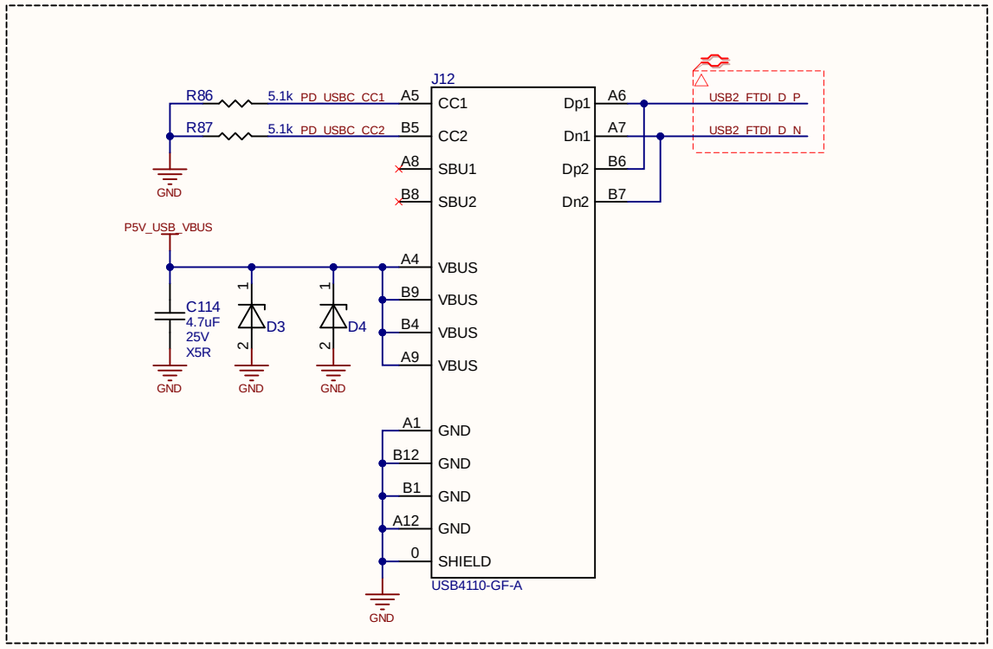
14_IO_MIPI.SchDoc



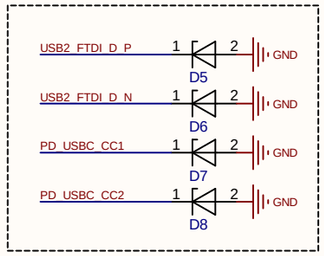
DEVEFX000001A.PrjPcb

15_IO_USB.SchDoc

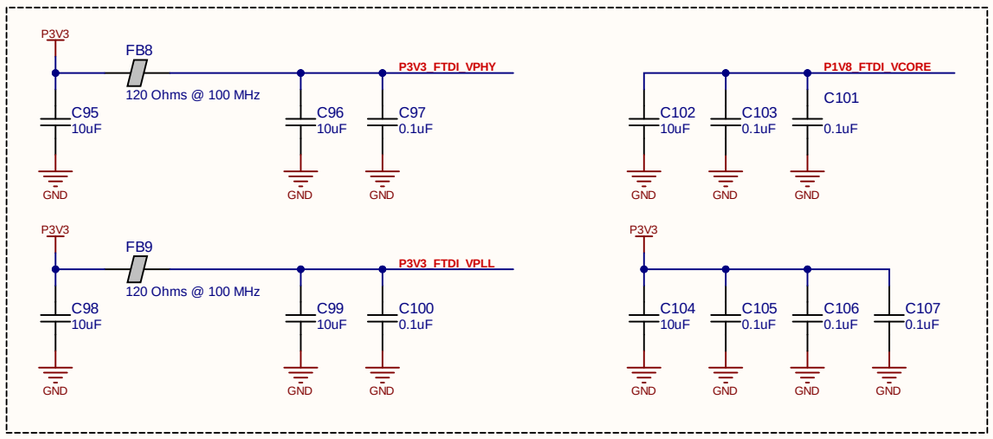
USB



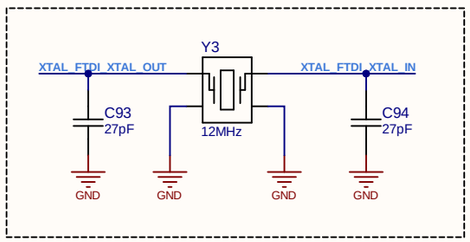
DATALINE TVS



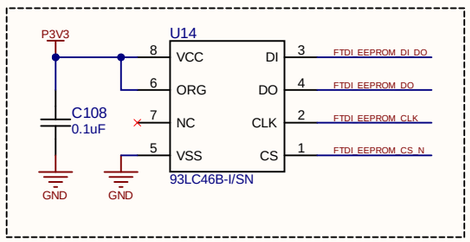
FTDI POWER

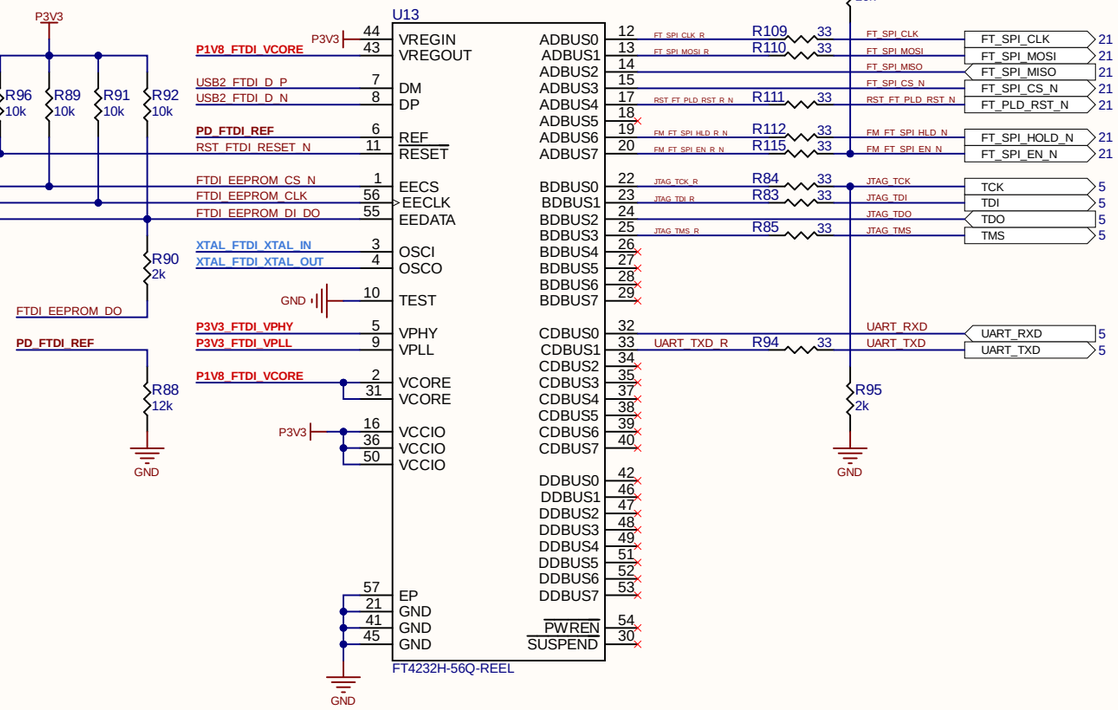


XTAL



EEPROM





DEVEFX000001A.PrjPcb

16_IO_LVDS.SchDoc

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DEVEFX000001A.PrjPcb

17_IO_HEADERS.SchDoc

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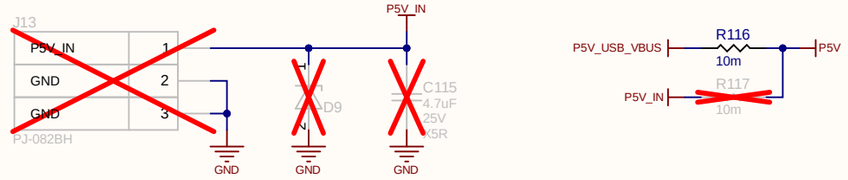
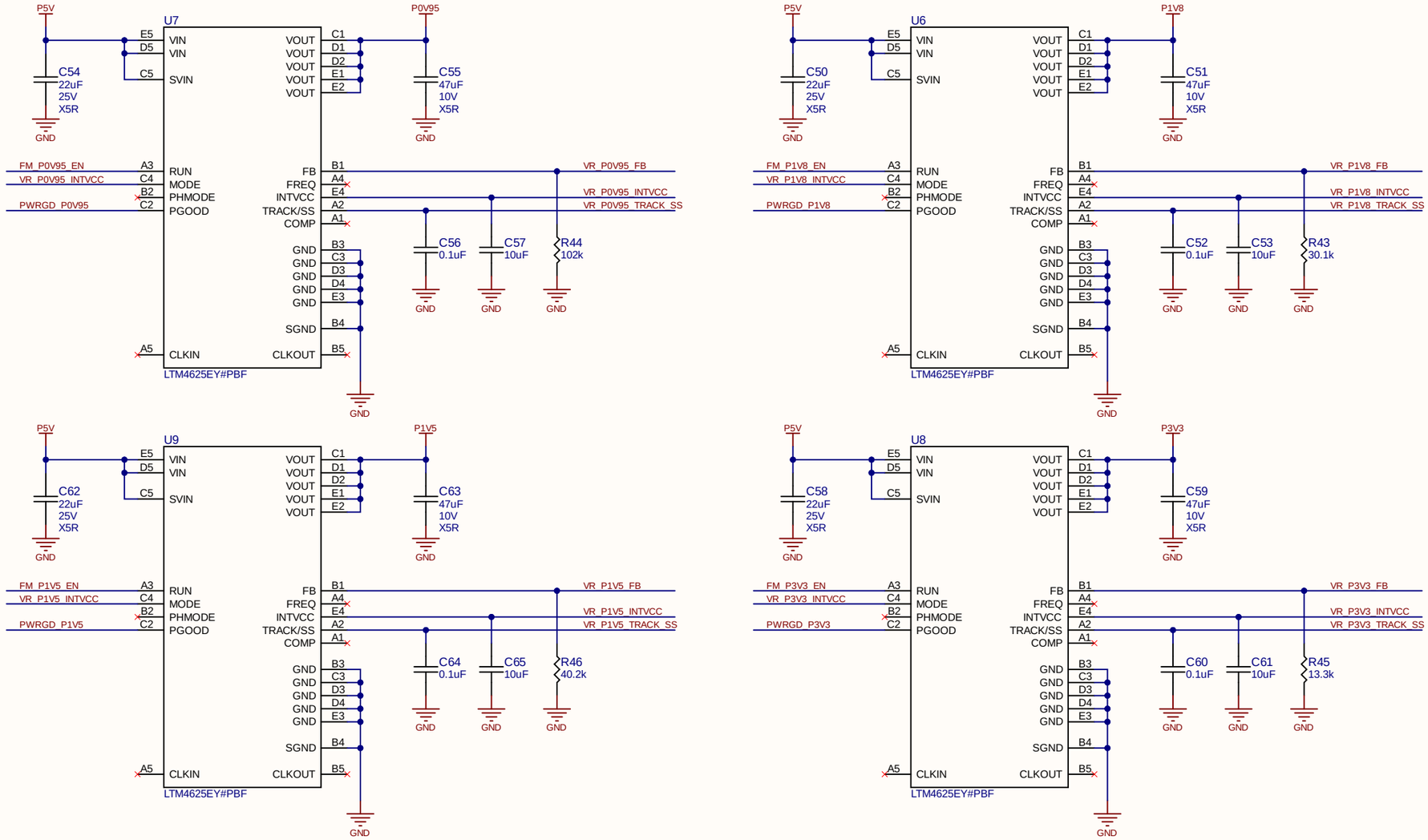
DEVEFX000001A.PrjPcb

18_PWR_INPUT.SchDoc

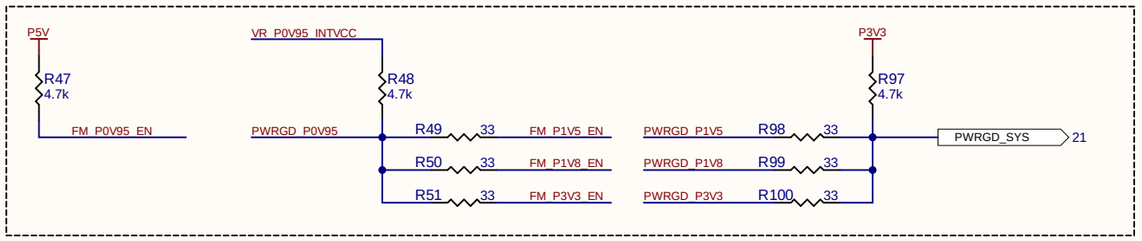


DEVEFX000001A.PrjPcb

19_PWR_VRS.SchDoc



POWER & RESET SEQUENCE



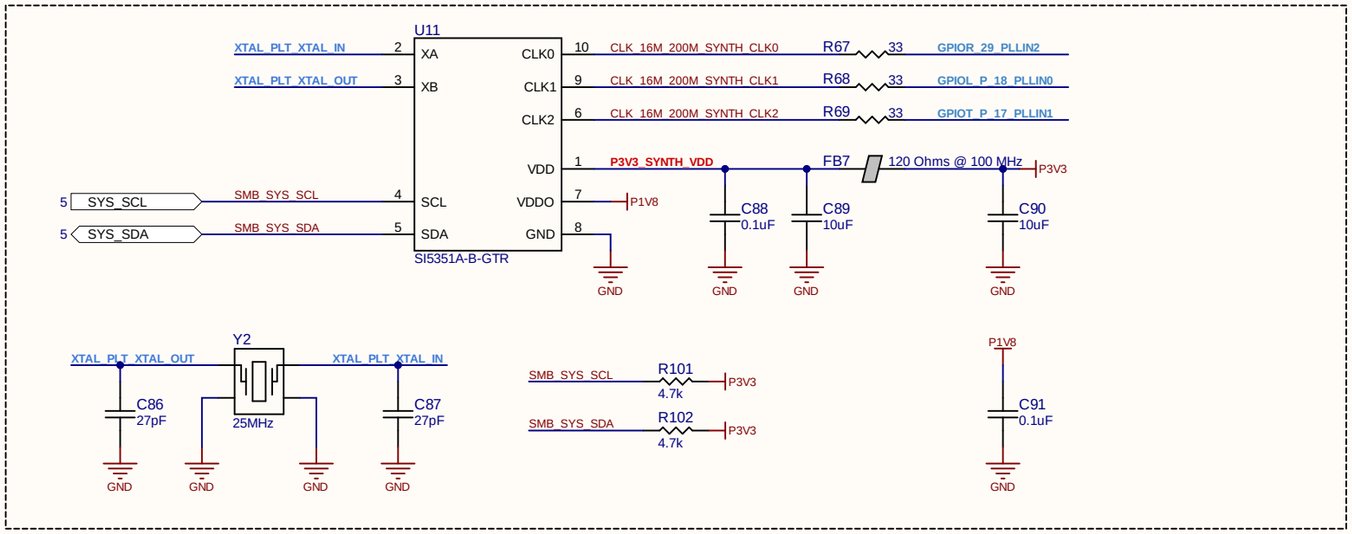
DEVEFX000001A.PrjPcb

20_CLOCKS.SchDoc

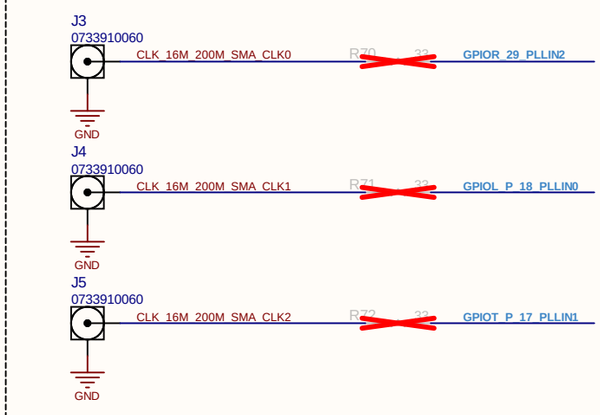
PLL Timing

Symbol	Parameter	Min	Typ	Max	Units
FIN	Input clock frequency	16	–	800	MHz
FOUT	Output clock frequency	0.1342	–	1.000	MHz
FVCO	PLL VCO frequency	2.200	–	5.500	MHz
FPLL	Post-divider PLL VCO frequency	–	–	4.000	MHz
FPFD	Phase frequency detector input frequency	16	–	800	MHz

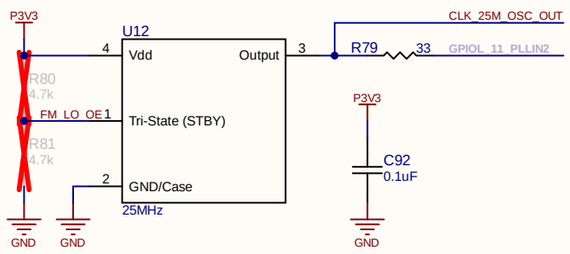
OPTION #0 - LOCAL PLL



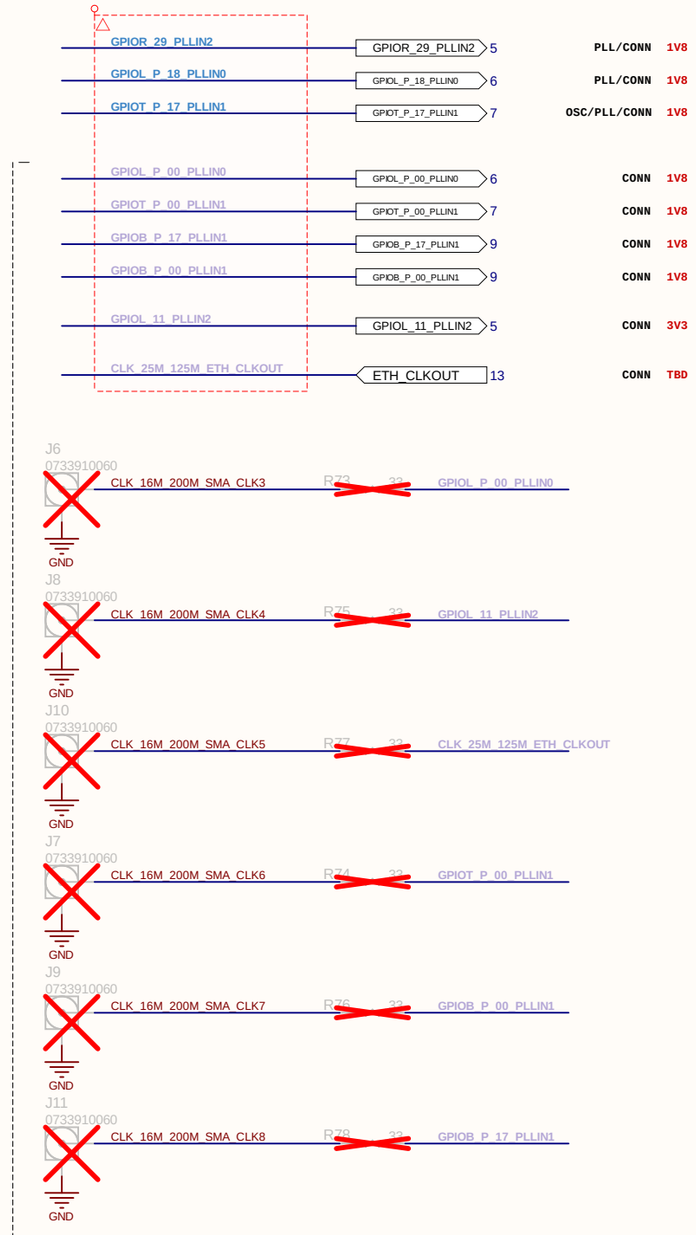
OPTION #1 - SMA (CAN ALSO BE USED FOR PLL PROBING)



OPTION #2 - LO FOR GPIOL_11_PLLIN2



Pad 1	Pad 3
Open	Oscillation
VIH 70% VDD Min.	Oscillation
VIL 30% VDD Max.	No Oscillation



DEVEFX000001A.PrjPcb

21_RESET_MISC.SchDoc