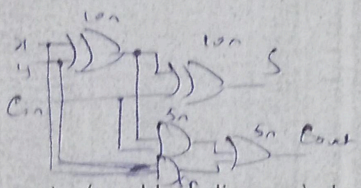
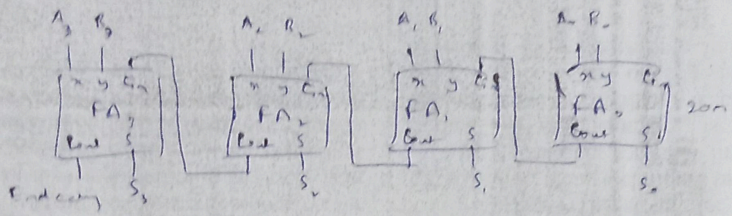
1. [CLO-2, C3]

a. Design full adder. [1]



b. Using the design implemented in part a (use block diagram), design a 4-bit parallel adder. [2]



c. Assume that the XOR gate has a propagation delay of 10ns and that the AND or OR gates have propagation delay of 5ns. What is the total propagation time in the 4-bit adder designed in part b? Can you predict the delay for a 64-bit adder? [1]

$4 \times 20n = 80ns$ (1) $64 \times 20n = 1280ns$

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d. Using the same delays of AND, OR and XOR gates as in part (c), and considering a 64-bit carry lookahead adder, calculate the delay of the complete circuit. [2]

$G = AB$, $P = A \oplus B$ — 3 levels for Cin generation

Gs, Ps are anded together first & then ORed. (2)

1st level to calculate Gs & Ps. $Delay_1 = Max(10n, 5n) = 10ns$

2nd " ANDing $Delay_2 = 5n$

3rd " ORing the results of AND, $delay_3 = 5n$

Cin generation, Total delay $= 10n + 5n + 5n = 20ns$.

Final o/p : total delay for Cin + $Delay_{XOR} + Delay_{XOR}$

$= 20n + 10n + 10n = 40ns$.

e. If A=1, B=1, Cin=1, then the condition is _____ where A and B are bits of addend and augend. [1]

a. a carry generates

b. a carry propagates (1)

c. no carry propagates

d. both a and b (A) & (a) both are marked correct

2. A combinational circuit accepts a 3-bit binary value and generates an output binary number equal to the square of the input number. Implement the design using two 2x4 decoders and minimum number of OR gates. [5] [CLO-2, C3]

A	B	C	U	V	W	X	Y	Z
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	0	0	0	0	1

$U = \Sigma(6,7)$

$V = \Sigma(4,5,7)$

$W = \Sigma(3,5)$

$X = \Sigma(2,6)$

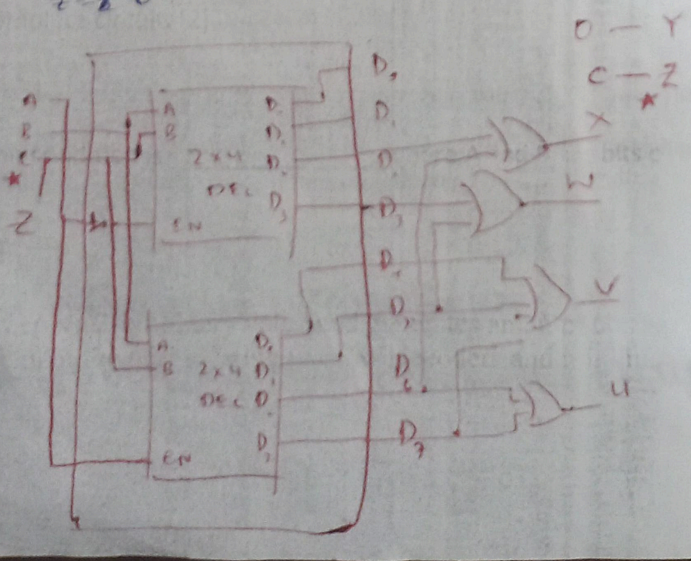
$Y = 0$

$Z = C$

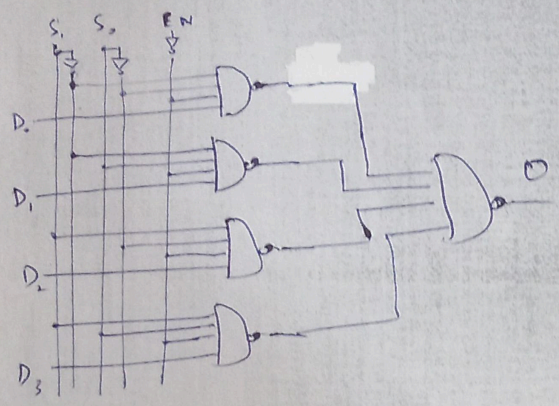
U, V, W, X shall be generated by decoders

Y = 0, Z = C directly derived

1 3x8 bin decoder

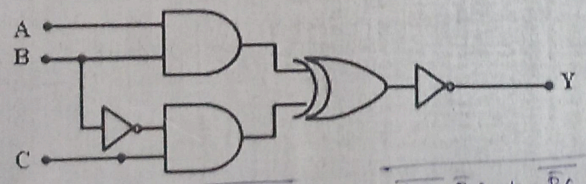


3. Give the logic diagram of a 4x1 multiplexer using NAND gates only. Include an active low enable input. Assume that all other input and output lines are active high. [4] **[CLO-2, C3]**



4. For the logic circuit given in figure 5, find: [4] **[CLO-1, C2]**
   a. standard SOP expression for Y
   b. standard POS expression for Y
   c. simplified expression for Y

Figure 5



a. $Y = \overline{AB \oplus \bar{B}C} = \overline{AB\,\bar{B}C + \bar{B}C\,AB} = (\bar{A}+\bar{B})\bar{B}C + (B+\bar{C})AB = A\bar{B}C + \bar{B}C + AB + AB\bar{C}$

$= A\bar{B}C + AB\bar{C} + (A+\bar{A})\bar{B}C + ABC(+\bar{C}) = ABC + AB\bar{C} + A\bar{B}C + AB\bar{C} =$

$= \overline{A\bar{B}C} \cdot \overline{AB\bar{C}} \cdot \overline{A\bar{B}C} \cdot \overline{ABC} = (A+B+\bar{C})(\bar{A}+\bar{B}+C)(\bar{A}+B+\bar{C})(A+\bar{B}+\bar{C})$

b. $Y = \Pi(1,5,6,7)$

c. $Y = \Sigma(0,2,3,4)$.

$\Rightarrow \overline{\bar{B}C + AB} = (B+\bar{C}).(A+\bar{B}) = AB + A\bar{C} + B\bar{C} = Y$