CHAPTER 3

CASCADED H-BRIDGE MULTILEVEL INVERTER

The cascaded H-bridge inverter has drawn tremendous interest due to the greater demand of medium-voltage high-power inverters. It is composed of multiple units of single-phase H-bridge power cells. The H-bridge cells are normally connected in cascade on their ac side to achieve medium voltage operation and low harmonic distortion. The cascaded H-bridge multilevel inverter requires a number of isolated dc supplies, each of which feeds a H-bridge power cell.

The single phase H-bridge cell, which is the building block for the cascaded H-bridge inverter is associated with separate dc sources.
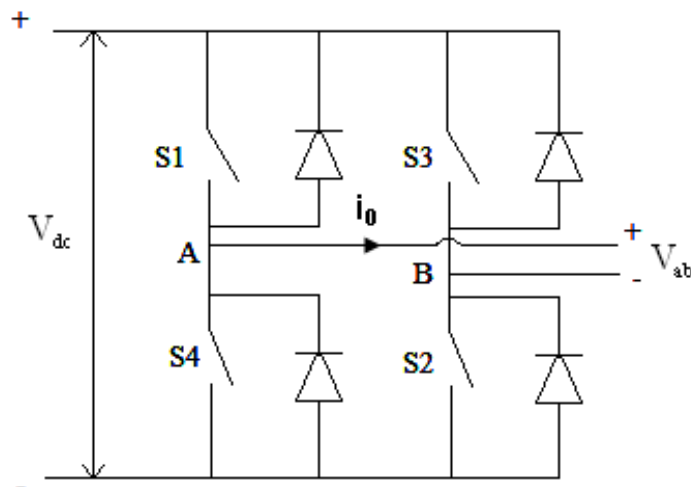

Figure 3.1 (a) Single Phase H-Bridge Inverter

Figure 3.1 shows a simplified circuit diagram of a single phase multilevel cascaded H-bridge inverter. It is composed of two inverter legs
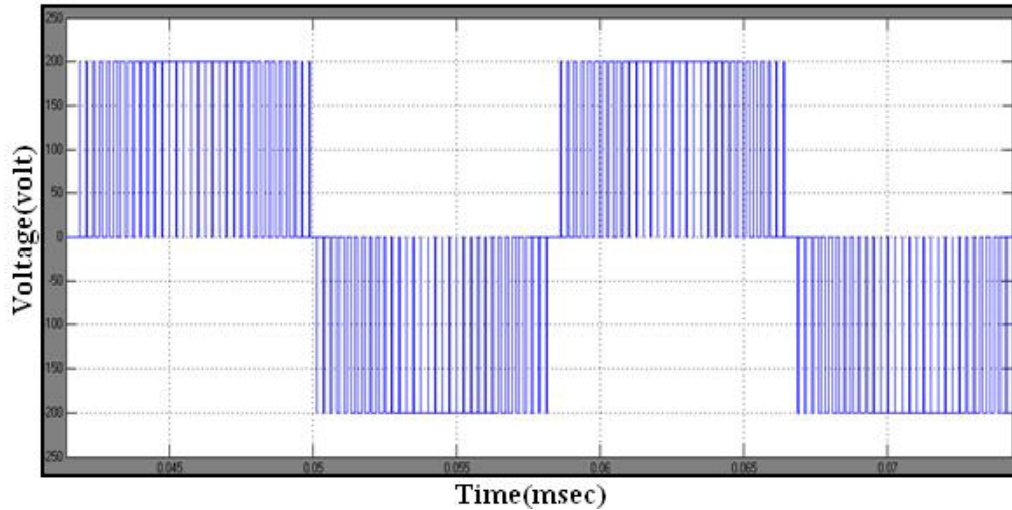

Figure 3.1(b) Output Voltage of Single Phase H-Bridge Inverter

with two power device in each leg. The inverter dc bus voltage V_{dc} is usually fixed, while its ac output voltage V_{ab} can be adjusted by either bipolar or unipolar modulation schemes. With different combinations of four switches, S_1 to S_4, each inverter level can generate three different voltages at the output $+V_{dc}$, $-V_{dc}$ and 0. During inverter operation shown in Figure 3.1, switch S_1 and S_2 are closed at the same time to provide V_{dc} a positive value and a current path for i$_0$. Switch S_3 and S_4 are turned on to provide V_{dc} a negative value with a path for i_0. Depending on the load current angle, the current may flow through the main switch or the freewheeling diodes are connected anti parallel with each switch. The output voltage of single phase H-bridge inverter is shown in Figure 3.1(a).

In case of zero level, there are two possible switching patterns to synthesize zero level, they are i) S_1 and S_3 on , S_2 and S_4 off , and ii) S_1 and

S_3 off and S_2 and S_4 on.   A simple gate signal, repeated zero level patterns is shown in Figure 3.2. All zero levels are generated by turning on S_1 and S_3.
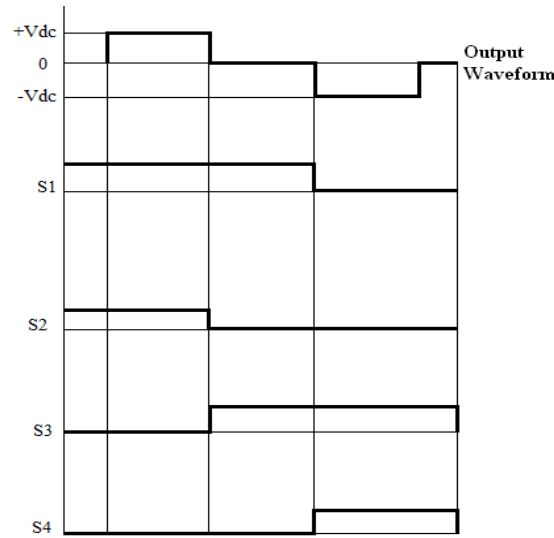

Figure 3.2 Zero-Level Switching Pattern

Note that level 1 represents the state when the gate is turned on, and level 0 represents the state when the gate is turned off. In Figure 3.1, S_1 and S_3 are turned on longer than S_2 and S_4 in each cycle because the same zero level switching patterns are used. As a result, S_1 and S_3 consume more power, getting higher temperature than the other two switches. To avoid this problem, a different switching pattern for zero level is applied.

In the first zero stage S_1 and S_3 are turned on, then in the second zero stage, S_2 and S_4 are turned on instead of S_1 and S_3. By applying this method, turn-on time for each switch turns out to be equal, as shown in Figure 3.3.
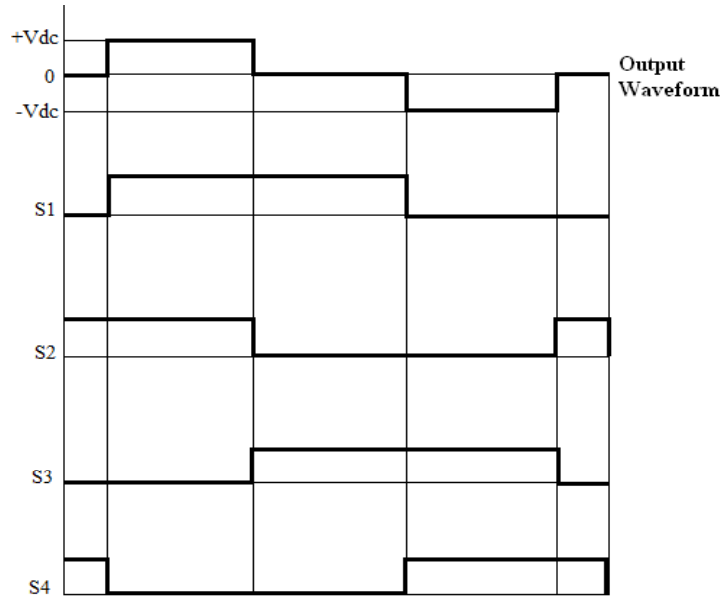
Figure 3.3 Swapped Zero-Level Switching Pattern

3.1   SINGLE-PHASE CASCADE INVERTER STRUCTURE

To synthesize a multilevel waveform, the AC output of each of the different level H-bridge cells are connected in series. The cascaded voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

$$n = 2s + 1 \tag{3.1}$$

where s is the number of dc sources.

A five-level output phase voltage waveform can be obtained with two-separated dc sources and four H-bridge cells. Figure 3.4 shows a general single phase n-level cascaded inverter. From Figure 3.4, the phase voltage is the sum of each H-bridge outputs and is given as

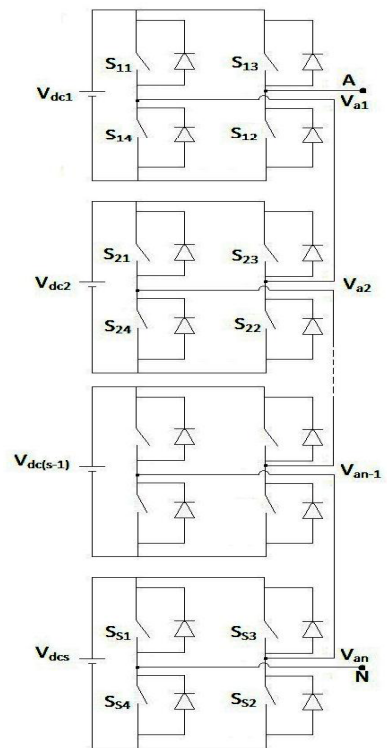$$V_{an} = V_{dc1} + V_{dc2} + \ldots + V_{dc(S-1)} + V_{dcS} \tag{3.2}$$

Figure 3.4   (a) Single-Phase Configuration of an m-Level Cascaded Inverter
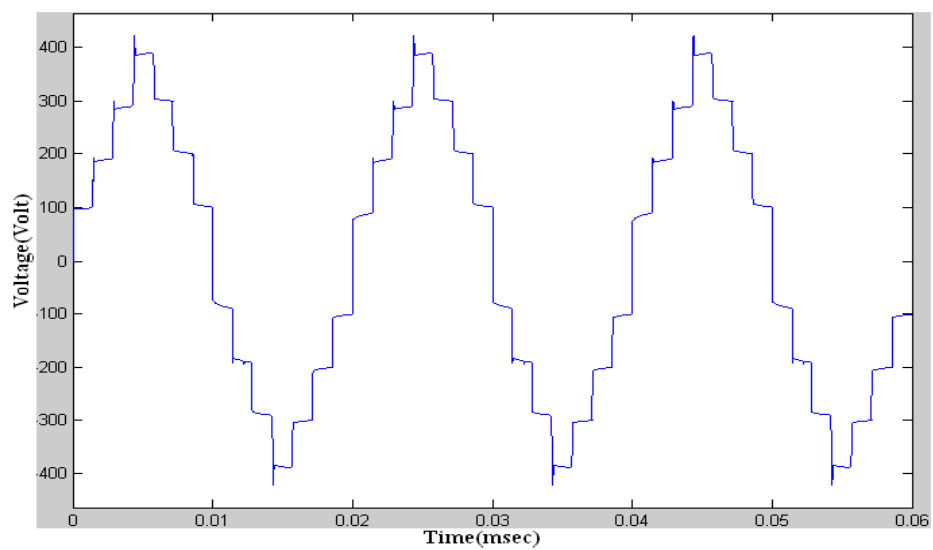

Figure 3.4 (b) Output voltage of Single Phase Seven level Inverter

The output voltage of a single phase seven level cascaded H-bridge inverter is shown in Figure 3.4(a). Because zero voltage is common for all inverter outputs, the total level of output voltage waveform becomes $2s+1$. An example phase voltage waveform for a five-level cascaded inverter and all H-bridge cell output waveforms are shown in Figure 3.5.

According to sinusoidal-linked waveform, each H-bridge output waveform must be quarter-symmetric as illustrated by V_1 waveform in Figure 3.5, no even harmonics components are presented in such a waveform as presented in Tolbert et al (1999).
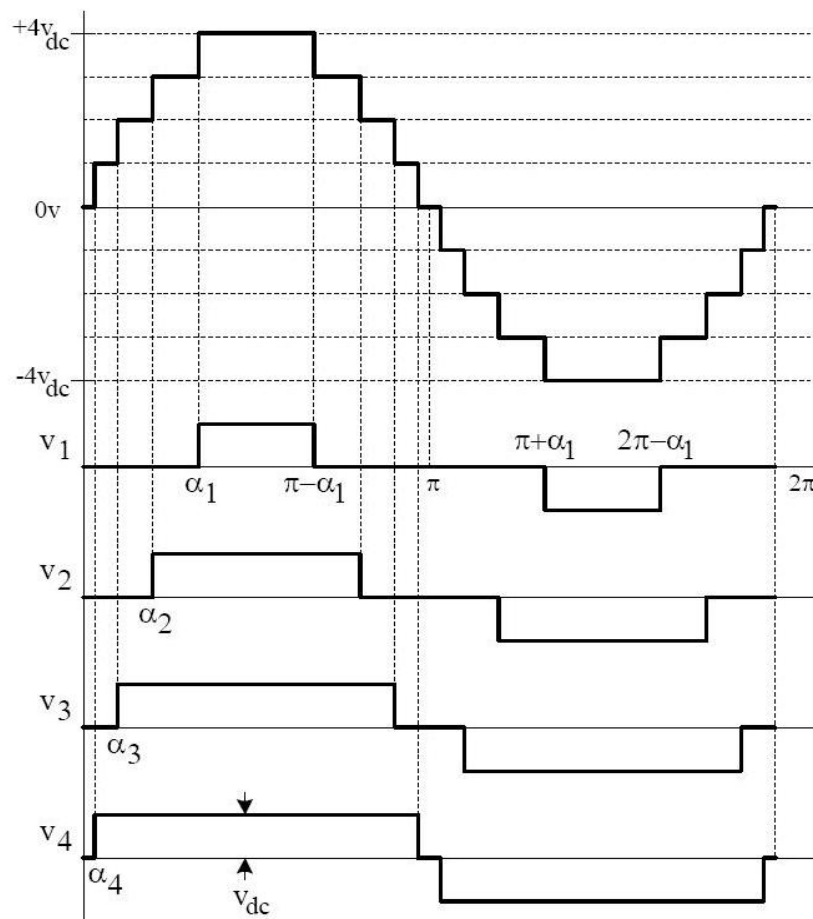

Figure 3.5 Waveform Showing a Nine-Level Output Phase Voltage and Each H-Bridge Output Voltage

3.2 THREE-PHASE CASCADE INVERTER STRUCTURE

For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either star or delta configuration. In Figure 3.6 illustrates the diagram of star-connected seven-level inverter using three H-bridge cells and three separate dc sources per phase. From Figure 3.6, V_{an} is voltage of phase A, which is the sum of V_{a1}, V_{a2} and V_{a3}. The same method is applied to phase B and phase C.
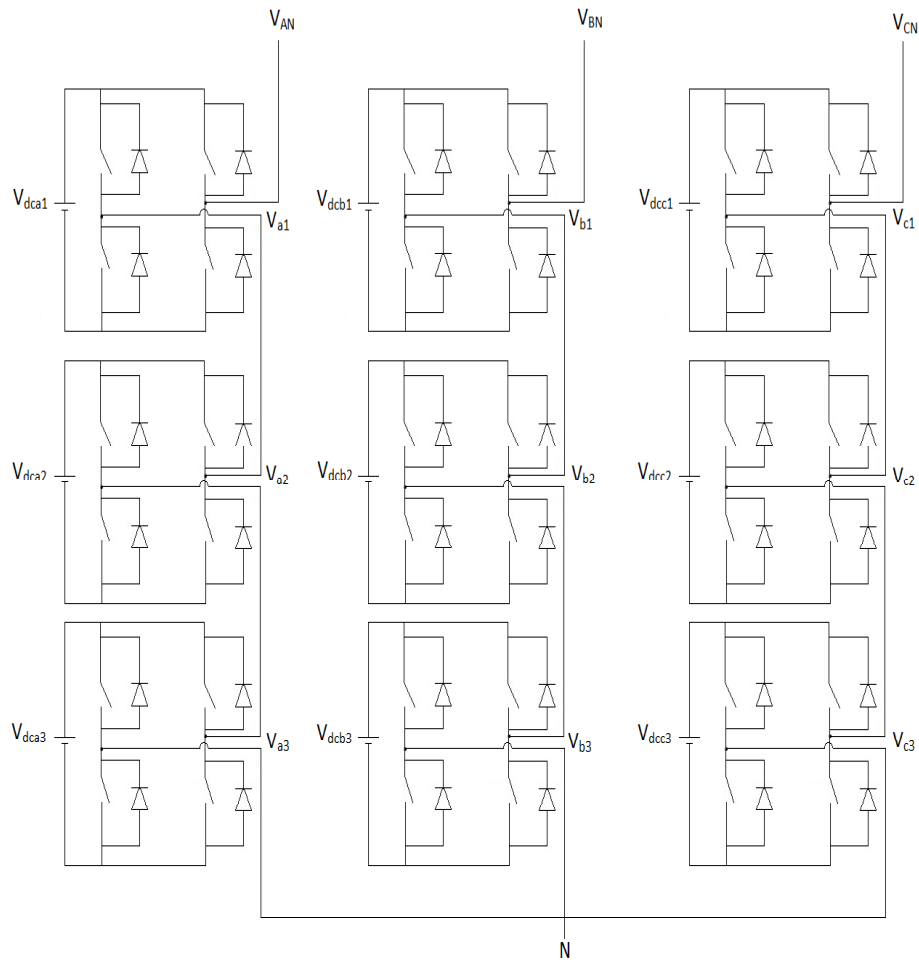

Figure 3.6. (a) Three-Phase Seven Level Cascaded H-Bridge Inverter

To synthesize seven-level phase voltage, three firing angles are required. The same three switching angles can be used in all the three phases with delaying 0^0, 120^0 and 240^0 electrical degree for phase A, B and C respectively. The three-phase seven-level cascaded H-bridge multilevel inverter output voltage is shown in Figure 3.6 (a).
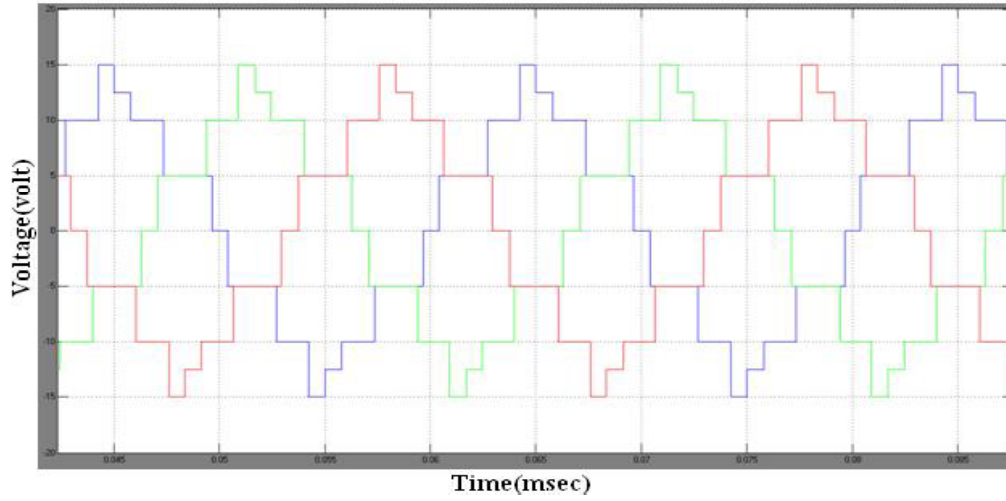

Figure 3.6 (b) Output Voltage of Three Phase Seven Level Inverter

According to the phase theory, line voltage can be expressed in term of two phase voltages. The potential difference between phase A and B is V_{ab}, which can be written as follows,

$$V_{ab} = V_{an} - V_{bn} \tag{3.3}$$

V_{ab} is line voltage

V_{an} is phase A voltage with respect to point N and

V_{bn} is phase B voltage with respect to point N

The maximum number of line voltage levels is $2n - 1$, where n is the number of phase voltage levels. The number of line voltage levels depend on the modulation index and the given harmonics are to be eliminated. The

seven-level cascaded inverter can synthesize up to thirteen-level line voltage. The advantage of three-phase system is that all the triple harmonics components in the line voltage will be eliminated by one-third cycle phase shift feature. Therefore, only non-triple harmonic components need to be eliminated from phase voltage. In single-phase nine-level waveform, the 3rd, 5th and 7th harmonics are eliminated from output phase voltage. Thus, the 9th harmonic is the lowest harmonic component in phase voltage of single phase system, while the 13th harmonic is the lowest harmonic component in phase voltage of three phase system by Menzies and Zhuang (1995).
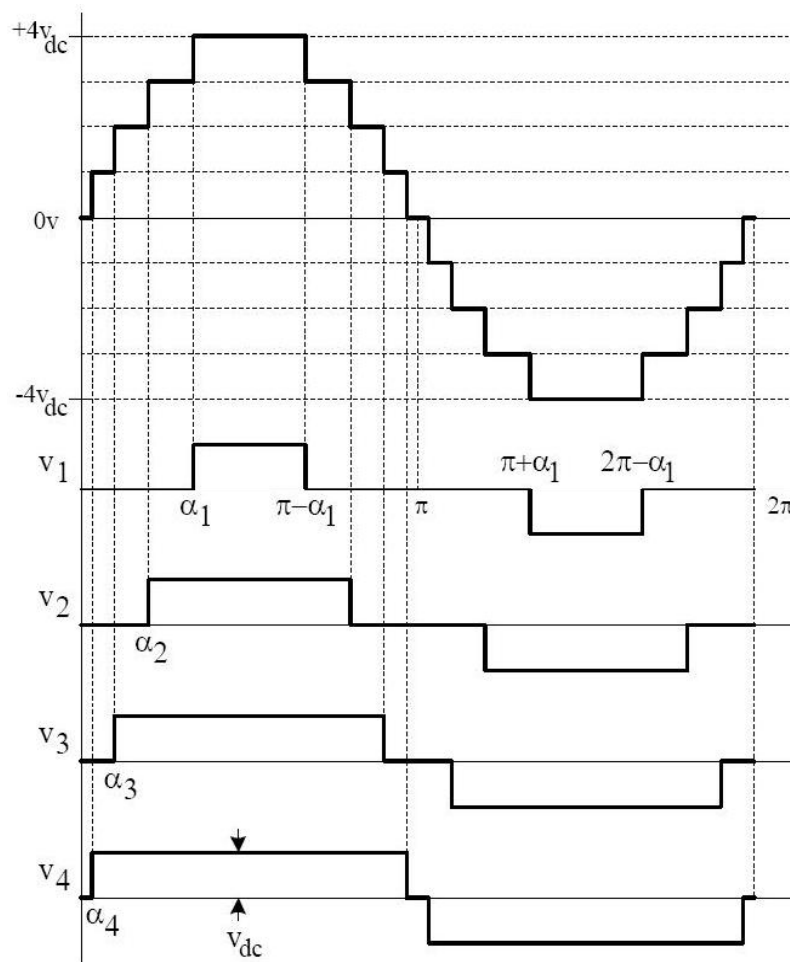

Figure 3.7   Two Phase Voltages and Line Voltages of Three-Phase Seven-Level Cascaded Inverter

Figure 3.7, shows output voltage of phase A, V_{an} and output voltage of phase B, V_{bn}, line voltage waveform, V_{ab} of seven-level cascaded inverter. Assuming the positive sequence three-phase system, output voltage of phase B lags output voltage of phase A by 120^0 electrical degree. The line voltage, V_{ab} therefore leads to the voltage of phase A by 30^0 electrical degree, which is according to the three-phase theory.

3.3   CASCADED H-BRIDGE INVERTER WITH EQUAL DC VOLTAGES

The cascaded H-bridge multilevel inverter uses multiple units of H-bridge power cells connected in a series of chain to produce high ac voltages. A typical configuration of a seven-level cascaded H-bridge inverter is shown in Figure 3.6, where each phase leg consists of two H-bridge cells powered by two isolated dc supplies of equal voltage V_{dc}. The dc supplies are normally obtained by multi pulse diode rectifier.

The cascaded H-Bridge inverter in Figure 3.6 can produce a phase voltage with seven voltage levels. When switches $S_{11}, S_{21}, S_{31}, S_{12}, S_{22}$ and S_{32} conduct, the output voltage of the H-bridge cells H_1, H_2 and H_3 is $V_{a1} = V_{a2} = V_{a3} = V_{dc}$ and the resultant inverter phase voltage is $V_{an} = V_{a1} + V_{a2} + V_{a3} = 3V_{dc}$, which is the voltage at the inverter terminal '0' with respect to the inverter neutral N. Similarly, with $S_{13}, S_{23}, S_{33}, S_{14}, S_{24}$ and S_{34} switched on, $V_{an} = -3V_{dc}$. The other five voltage levels are $2V_{dc}, V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$, which correspond to various switching states. Voltage and switching state of the seven-level CHB inverter is shown in Figure 3.7.

The cascaded H-bridge inverter introduced above can be extended to any number of voltage levels. The total number of active switches used in the cascaded H-Bridge can be calculated by,

$$N_{SW} = 6(n-1) \tag{3.4}$$

3.4 HARMONIC ELIMINATION SWITCHING SCHEMES

This section presents switching schemes involving harmonic elimination besides various multilevel switching schemes which was discussed in previous chapter. More specifically, Bipolar Programmed PWM, Unipolar Programmed PWM, and Virtual Stage PWM are discussed.

3.4.1 Bipolar Programmed PWM

Bipolar Programmed PWM is one of the switching schemes involving harmonic elimination. In Bipolar Programmed PWM, the output voltage is either $+V_{dc}$ or $-V_{dc}$. Figure 3.8 illustrates the Bipolar Programmed PWM switching scheme using three switching angles and an V_{dc} equal to 12 V.
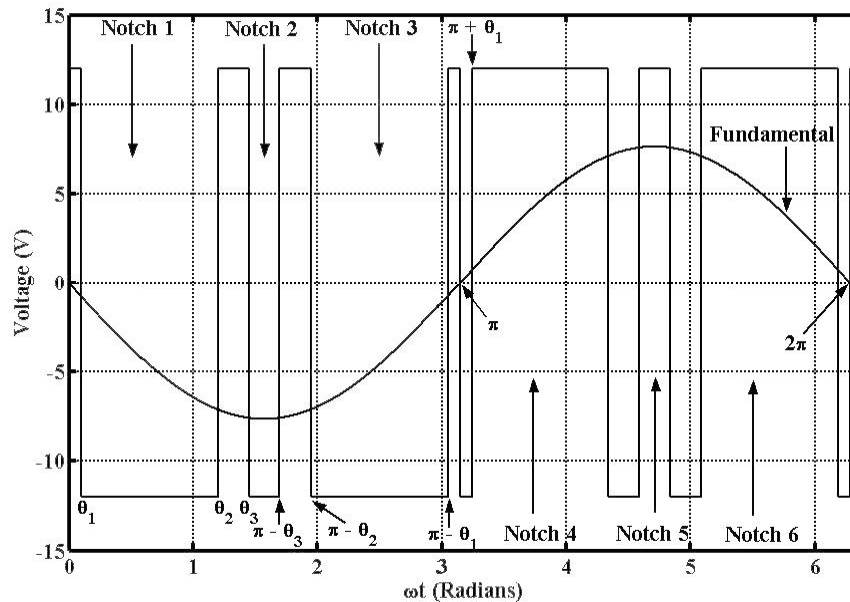

Figure 3.8 Bipolar Programmed PWM Using Three Switching Angles

From the Figure 3.8, it is noticed that Bipolar Programmed PWM uses predetermined switching angles to cut notches into a square-wave output. These notches take the voltage either from $+V_{dc}$ to $-V_{dc}$ or from $-V_{dc}$ to $+V_{dc}$. The number of notches cut per fundamental cycle is equal to twice the number of switching angles used, which was addressed in Mohan et al (1995). By using Fourier series theory, these switching angles can be used to eliminate certain harmonics. For example, three switching angles can be used to eliminate the fifth and seventh order harmonics while at the same time controlling the value of the fundamental.

One of the main advantages of using Bipolar Programmed PWM concerns its applicability when low modulation indices are used. When low modulation indices are used, the fundamental multilevel switching scheme is unable to perform the desired harmonic elimination process. The three switching angles are considered again, when the fundamental multilevel switching schemes are used, it is not able to eliminate both the fifth and seventh order harmonics and control the value of the fundamental. However, Bipolar Programmed PWM can be used with low modulation indices were discussed in Chiasson et al (2004).

When a multilevel inverter utilizes Bipolar Programmed PWM for a low modulation index, typically one H-bridge is used. Another advantage of Bipolar Programmed PWM is redundancy. If one H-bridge fails, another H-bridge can be used to compensate the necessary voltage. Also, the desired voltage can be achieved by using a sequence of switchings for each H-bridge inverter within short periods of time. Bipolar Programmed PWM can be used for higher modulation indices in addition to low modulation indices. If a multilevel inverter needs to use two or more H-bridges in order to produce a desired voltage, one can choose a lower modulation index and use Bipolar Programmed PWM on multiple H-bridges.

Another advantage of Bipolar Programmed PWM is that control is not as complicated as some other switching schemes. Consider one of the H-bridges in   Figure 3.4. neglecting blanking time, switches S_{11} and S_{13} are switched "on" and "off" together. Similarly, switches S_{12} and S_{14} are switched "on" and "off" together.

Bipolar Programmed PWM also has some disadvantages. One disadvantage concerns EMI. As mentioned earlier, Bipolar Programmed PWM produces voltage changes equal to $2V_{dc}$. Therefore, a large V_{dc} can produce a considerable amount of EMI. Furthermore, Bipolar Programmed PWM inherently increases the effective switching frequency. The multilevel fundamental switching scheme can result in each switch being turned "on" and "off" once per cycle. However, if Bipolar Programmed PWM is implemented using three switching angles, each switch is turned "on" and "off" seven times in the switching states. Therefore, the effective switching frequency of each switch is increased by a factor of seven.

Another disadvantage of Bipolar Programmed PWM concerns harmonic distortion. For low modulation indices, using Bipolar Programmed PWM may still lead to a high amount of harmonic content in the output. In fact, the THD may be over 100% for certain modulation indices.

3.4.2   Unipolar Programmed PWM

Unipolar Programmed PWM is another switching scheme involving harmonic elimination. In Unipolar Programmed PWM, the output voltage is $+V_{dc}, -V_{dc}$, or 0. Furthermore, a voltage change is from $\pm V_{dc}$ to 0 and vice versa. Figure 3.9 illustrates the Unipolar Programmed PWM switching scheme using three switching angles and an V_{dc} equal to 12 V.

From Figure 3.9, it is observed that Unipolar Programmed PWM uses predetermined switching angles to produce an output consisting of multiple pulses of varying widths. For the positive half of the fundamental cycle, these pulses have a voltage equal to $+V_{dc}$. For the negative half of the fundamental cycle; these pulses have a voltage equal to $-V_{dc}$. The number of pulses per fundamental cycle is equal to twice the number of switching angles used. Similar to Bipolar Programmed PWM, Fourier series theory can be used to determine the switching angles such that certain harmonics are eliminated. In fact, these two switching schemes produce almost identical equations to solve. The only difference between the two sets of equations is that the Bipolar Programmed PWM equations contain a few extra numerical constants.

Unipolar Programmed PWM shares many of the advantages of Bipolar Programmed PWM. Similar to Bipolar Programmed PWM, Unipolar Programmed PWM can also be used with low modulation indices, even when one may not be able to use the multilevel fundamental switching scheme. Unipolar Programmed PWM also shares the advantage of redundancy when low modulation indices are used. As with Bipolar Programmed PWM, if one H-bridge fails, another H-bridge can be used to provide the necessary voltage. Also, in Unipolar Programmed PWM, the desired voltage can be achieved by using a sequence of switchings for each H-bridge inverter within short periods of time. Unipolar Programmed PWM can also be used for higher modulation indices.
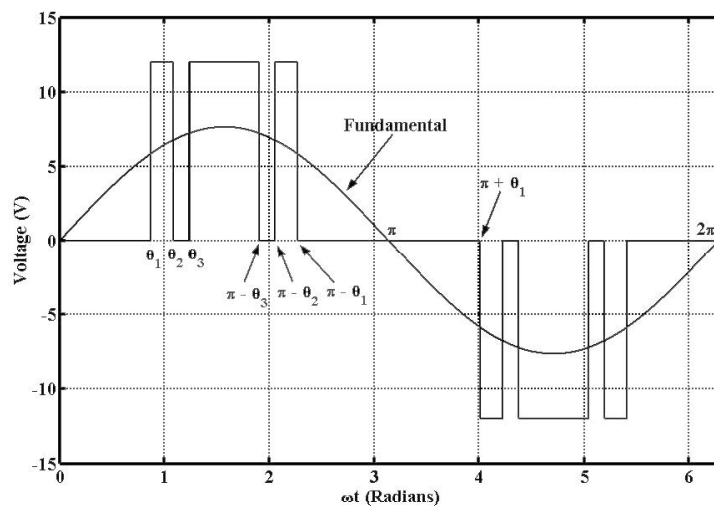
Figure 3.9 Unipolar Programmed PWM Using Three Switching Angles

Like Bipolar Programmed PWM, one disadvantage of Unipolar Programmed PWM concerns harmonic distortion. For low modulation indices, using Unipolar Programmed PWM may still lead to a high output THD. However, Unipolar Programmed PWM tends to produce a lower THD than Bipolar Programmed PWM. From Figures 3.8 and 3.9, it is noticed that Unipolar Programmed PWM seems to provide a more natural approximation to a sinusoidal waveform.

Unipolar Programmed PWM will also tend to produce less EMI than Bipolar Programmed PWM. Bipolar Programmed PWM produces voltage changes equal to $2V_{dc}$. However, Unipolar Programmed PWM produces voltage changes equal to V_{dc} only. Also, Unipolar Programmed PWM increases the effective switching frequency by a smaller factor. If Unipolar Programmed PWM is implemented using three switching angles, each switch can be made to turn "on" and "off" three times per cycle. Hence, the effective switching frequency of each switch is increased by a factor of three, instead of the factor of seven increase caused by using Bipolar Programmed PWM.

However, Unipolar Programmed PWM does require more complicated control compared to Bipolar Programmed PWM. For example, consider once again one of the H-bridges in Figure 3.4. Switches S_{11} and S_{13} are no longer switched "on" and "off" together. They must now be controlled independently. The same situation occurs with switches S_{12} and S_{14}

3.4.3   Virtual Stage PWM

Virtual Stage PWM is another switching scheme involving harmonic elimination. The Virtual stage PWM is used in order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveform was proposed by Li et al (2000), Shyu and Lai (2002) and Sirisukprasert et al (2002).

The Virtual Stage PWM is a combination of Unipolar Programmed PWM and fundamental frequency switching scheme. The output waveform of Unipolar Programmed PWM is shown in Figure 3.9. When Unipolar Programmed PWM is employed on a multilevel inverter, typically one dc source voltage is involved, where the switches connected to the dc source voltage are switched "on" and "off" several times per fundamental cycle. The switching pattern decides what the output voltage waveform looks like (Refer Figure 3.7).

When the multilevel fundamental switching method is used, all of the dc voltages are typically involved, where all of the switches are turned "on" and "off" only once per fundamental cycle. The multilevel fundamental switching method also refers to exactly one switching pattern. (Refer Figure 3.5). For fundamental switching frequency method, the number of switching angles is equal to the number of dc sources. However, for the Virtual Stage PWM method, the number of switching angles is not equal to the number of dc voltages i.e., the number of dc sources used varies. In Figure 3.10, only two dc voltages are used, whereas there are four switching angles.
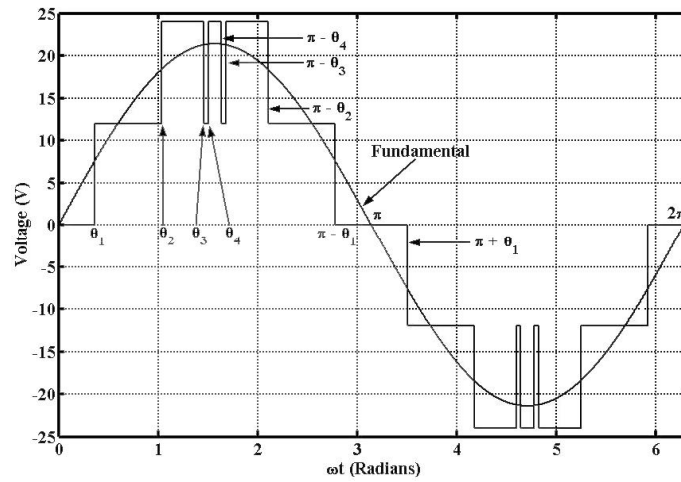
Figure 3.10 Virtual Stage PWM Using Two DC Sources

The third switching angle forces the second H-bridge to produce a zero output voltage. Effectively, the switching pattern in Figure 3.10 is comparable to using the multilevel fundamental switching scheme on one H-bridge with θ_1 as the switching angle and Unipolar Programmed PWM on a second H-bridge with θ_2, θ_3 and θ_4 as the switching angles. Figure 3.11 provides an illustration of another Virtual Stage PWM switching pattern. In this figure, three dc sources are used, whereas once again there are four switching angles. The fourth switching angle forces the third H-bridge to produce a zero output voltage. Effectively, the switching pattern in Figure 3.11 is comparable to using the multilevel fundamental switching scheme on two H-bridges with θ_1 and θ_2 as the switching angles and Unipolar Programmed PWM on a third H-bridge with θ_3 and θ_4 as the switching angles. One of the main reasons for considering Virtual Stage PWM concerns THD. For some modulation indices, using Virtual Stage PWM on a multilevel inverter will result in a lower THD than if the multilevel fundamental switching scheme were used.
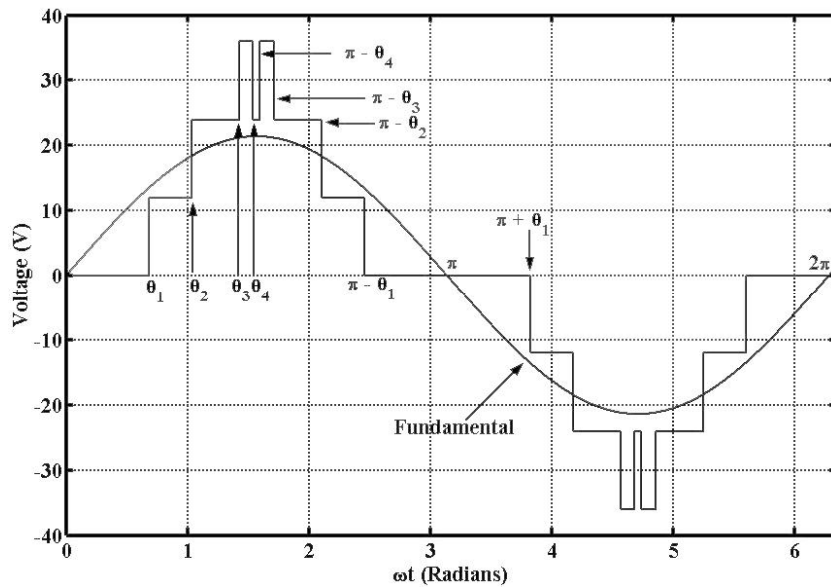
Figure 3.11 Virtual Stage PWM Using Three DC Sources

By using this technique, low switching frequencies with minimized harmonic content in the output waveforms can be achieved with wide modulation indexes. Consider a multilevel inverter using three dc sources. If the multilevel fundamental switching scheme is used, typically the fifth and seventh order harmonics are eliminated. However, the Virtual Stage PWM switching scheme described above utilizes four switching angles. In this case, the eleventh order harmonic can also be eliminated in addition to the fifth and seventh order harmonics. As a result, it is reasonable to use the Virtual Stage PWM switching scheme for certain modulation indices which will produce an output waveform with a lower THD.

The Bipolar Programmed PWM and Unipolar Programmed PWM can be used for modulation indices too low for the applicability of the multilevel fundamental frequency switching method. Virtual Stage PWM can also be used for low modulation indices. Virtual Stage PWM will produce output waveforms with a lower THD most of the time. Therefore, Virtual

Stage PWM provides another alternative to Bipolar Programmed PWM and Unipolar Programmed PWM for low modulation index control.

3.5   H-BRIDGES WITH UNEQUAL DC VOLTAGES

The switching schemes discussed above assumed that the dc sources used by the multilevel inverter were all equal to one another. However, quite often these dc sources are not equal to one another. Even if one tries to keep the various dc sources equal to one another, it is quite difficult to accomplish. As a result, research has been conducted where multilevel inverters are used with unequal dc sources. Cunnyngham (2001) has worked on finding appropriate switching angles for multilevel inverters with unequal dc sources. The idea of applying Resultant theory to this same problem was proposed by Chiasson et al (2003) and McKenzie (2004). One reason, why one will have the problem of unequal dc sources deals with the idea that each dc source will charge and discharge differently from another dc source. A multilevel inverter may use batteries as its dc sources. However, one battery will have a different internal resistance than a different battery. This factor alone will contribute to different charging/discharging rates.

Another reason for the problem of using unequal dc sources can be seen from observing Figure 3.13. In this figure, it is noticed that the H-bridge on the bottom is producing an output voltage for a longer period of time than the rest of the H-bridges. If real power flow is required, this particular H-bridge will transfer more power than the other H-bridges. As a result, the energy contained within that particular dc source will decrease more rapidly. Figure 3.13 implements the multilevel fundamental switching scheme on a multilevel inverter using three unequal dc sources. Even when the dc sources are not equal, the switching angles can be determined such that the fifth and seventh order harmonics are eliminated while at the same time controlling the

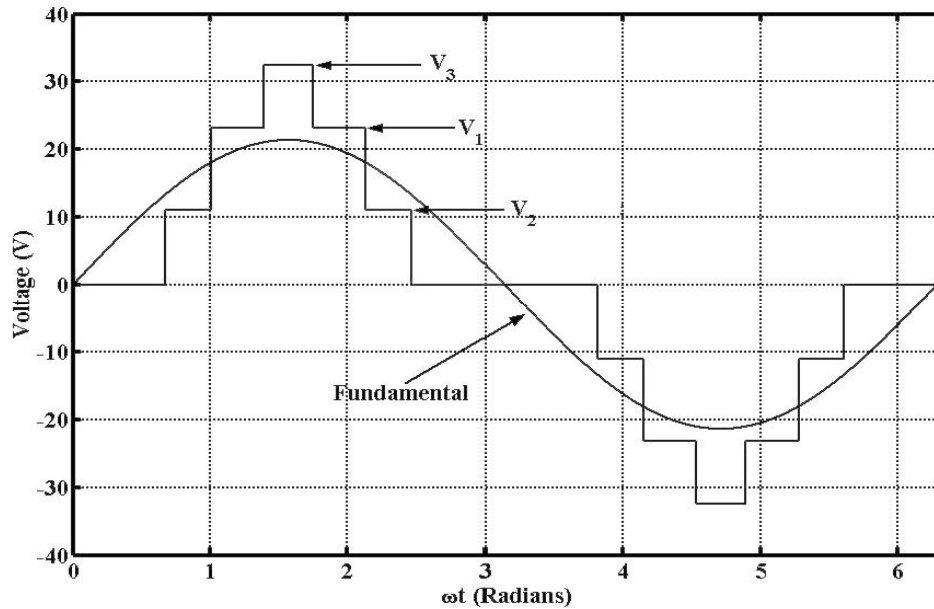value of the fundamental. In the figure, the nominal dc voltage of each dc source is 12 V.

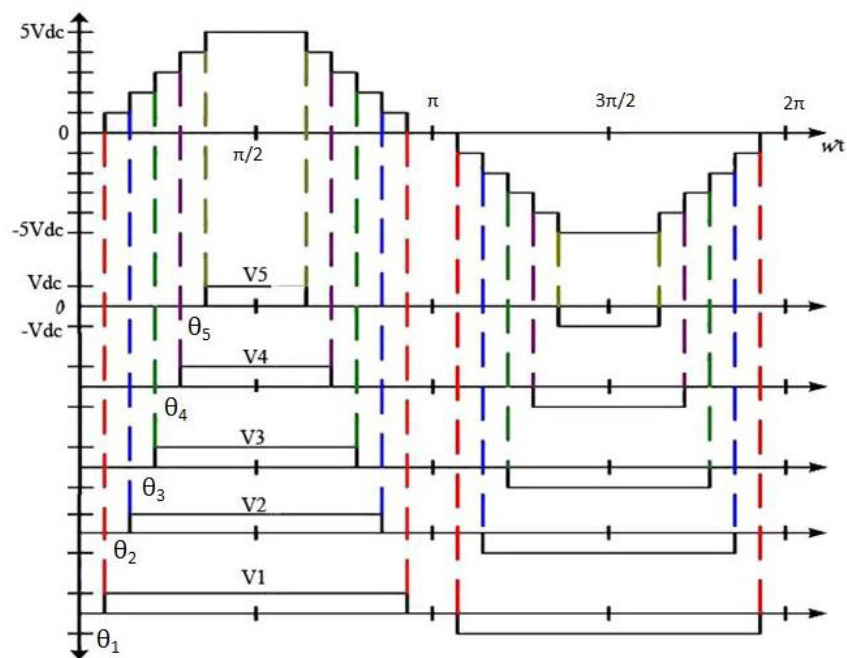**Figure 3.12 Multilevel Inverter Using Three Unequal DC Sources**

Figure 3.13 Output Voltage of Cascaded H-Bridges Multilevel Inverter

Also, the voltages of the three dc sources are 12.1V, 11.125V, and 9.1925V. Therefore, the three dc sources are operating at 100.8%, 92.7%, and 76.6% of their nominal values.

3.6   DUTY CYCLE SWAPPING

When a multilevel inverter is used for applications requiring real power flow, it can be undesirable to have a particular H-bridge to produce a particular output voltage for an extended period. As explained above, the dc sources could become unequal. This problem can be soothed by performing "duty cycle swapping". Figure 3.14 shows the utilization of duty cycle swapping on a multilevel inverter using five dc sources. When duty cycle swapping is used, after each half cycle the switching angle for a particular H-bridge is effectively rotated to a different H-bridge.
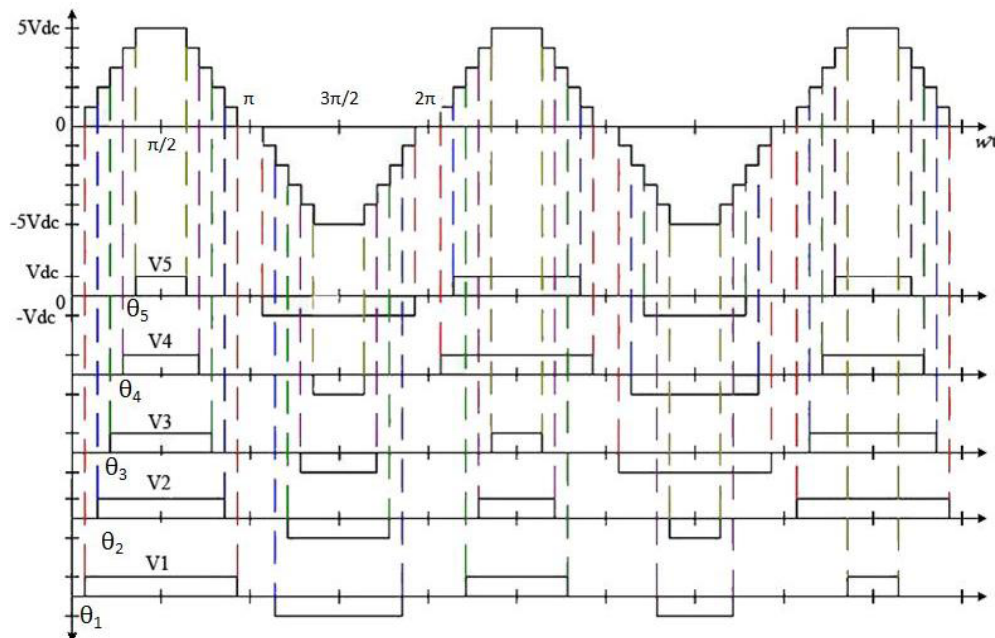

Figure 3.14 Duty Cycle Swapping Using Five DC Sources

The result is that every half cycle a single H-bridge produces a pulse of different time duration than the previous half cycle. By performing duty cycle swapping, each dc source will be utilized equally was presented in Tolbert and Peng (2000).

3.7   SUMMARY

In this chapter, the cascaded H-bridges multilevel inverter was discussed in more detail. Following the discussion on cascaded H-bridges multilevel inverters, switching schemes involving harmonic elimination besides multilevel fundamental switching were discussed. More specifically, the Bipolar Programmed PWM, Unipolar Programmed PWM and Virtual Stage PWM switching schemes were presented. The method of using unequal dc sources with multilevel inverters was discussed, followed by the concept of "duty cycle swapping."

The next chapter explains briefly about Space Vector Pulse Width Modulation (SVPWM). Also, this chapter presents methods of using SVPWM for three-legged voltage source inverter. The SVPWM control methods for multilevel inverters with equal and unequal DC voltages are discussed in the next chapter. More specifically, two-dimensional (2-D) SVPWM and three-dimensional (3-D) SVPWM algorithms are discussed in detail. The next chapter presents a new three-dimensional space vector modulation schemes for computing the switching state vectors and the nearest switching sequence. The optimized 3-D space vector modulation algorithm (3-D OSVPWM) is proposed for multilevel inverter with varying dc sources and unbalanced load. It is analyzed how optimized 3-D space vector modulation algorithm can be used to find solutions for reducing the total harmonic distortion (THD).