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Design and Analysis of a 7-Level Cascaded Multilevel Inverter with Dual SDCSs

Ilhami Colak*, Member IEEE, Ramazan Bayindir*, Member IEEE, Ersan Kabalci**, Member IEEE
Gazi Electrical Machines and Energy Control (GEMEC) Group
* Department of Electrical Education, Faculty of Technical Education, Gazi University, Besevler, Ankara 06500, Turkey
** Department of Technical Programs, Vocational Collage of Haci Bektas, Nevsehir University, Hacibektas, Nevsehir-Turkey
icolak@gazi.edu.tr, bayindir@gazi.edu.tr, ekabalci@gazi.edu.tr

***Abstract*- Multilevel inverters with a large number of steps can generate high quality voltage waveforms, good enough to be considered as suitable voltage source generators. A modified Sinusoidal Pulse Width Modulation (SPWM) modulator with phase disposition that increases output waveform up to 7-level while reducing output harmonics is presented in this paper. The proposed modulation technique can easily be applied to any multilevel inverter topology carrying out the necessary calculations. The modulator block is designed to control multilevel inverter that is constituted using dual H-bridge cells with IGBTs on each phase legs. The supply voltages of cells are defined at V_{dc}÷$2V_{dc}$ ratio to obtain an asymmetrical output. The output waveform of asymmetrical topology is increased up to 7-level by using dual separate DC sources (SDCSs). The DC supply requirement of asymmetrical cascaded topology is solved using dual sources instead of 6 SDCSs. The cascaded multilevel inverter is switched by the proposed 24-channel SPWM modulator. The harmonic analysis of proposed inverter has been performed under several working conditions such as various switching frequencies and modulation indexes. The detailed comparisons are performed to determine the best working conditions of voltage source inverters (VSI) and presented in this paper.**

I. INTRODUCTION

The preliminary studies on multilevel inverters (MLI) have been performed using three level inverters proposed by Nabae. In the study, the third level has been constituted by using neutral point of DC line and the topology has been defined as Diode Clamped (DC-MLI) [1]-[2]. In recent years, MLIs have gained much attention in the application areas of medium voltage and high power owing to their various advantages such as lower common mode voltage, lower voltage stress on power switches, lower dv/dt ratio to supply lower harmonic contents in output voltage and current, good electromagnetic compatibility, reduced switching losses and improved reliability on fault tolerance [2]-[9].

The most common MLI topologies classified into three types are Diode Clamped MLI (DC-MLI), Flying Capacitor MLI (FC-MLI), and Cascaded H-Bridge MLI (CHB-MLI). The Hybrid and Asymmetric Hybrid inverter topologies have been developed according to the combination of existing MLI topologies or applying different DC bus levels respectively [7], [10]-[13]. The cascaded multilevel topology that contains dual H-bridge cells on each phase legs to constitute a staircase waveform has been shown in Fig.1. Each single

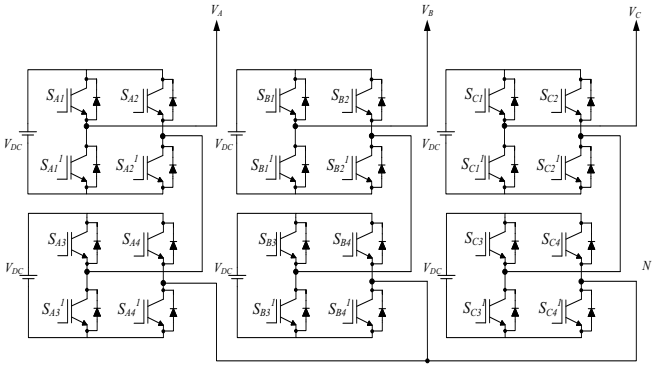

Fig. 1. Three phase five-level topology of cascaded H-bridge multilevel inverter

phase H-bridge generates three voltage levels as $+V_{dc}$, 0, $-V_{dc}$ connecting the DC source to the AC output by different combinations of four switches, S_{A1}, S_{A1}^1, S_{A2}, and S_{A2}^1 as seen in first cell of Fig. 1. The CHB-MLI depicted in Fig. 1 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain $+V_{dc}$, S_{A1} and S_{A2}^1 switches are turned on, whereas $-V_{dc}$ level can be obtained by turning on the S_{A2} and S_{A1}^1. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase as seen in (1). The switching states of a CHB-MLI can be determined using (2) [14]-[19].

$$m = 2n+1 \quad (1)$$

$$sw = 3^m \quad (2)$$

New topologies based on the existing multilevel topologies have been proposed and classified as hybrid topologies. The hybrid multilevel topologies are constituted using combination of two basic topologies of DC-MLI and FC-MLI. The topology utilizes DC-MLI or FC-MLI to replace the H-bridge as the basic module of the CHB-MLI in order to reduce the number of the separated DC sources. The asymmetric hybrid MLIs synthesize the output voltage waveforms with reduced harmonic content while increasing output levels with rational SDCSs [20]-[23].

Different types of feed-forward and feed-back PWM control schemes have been developed to control VSIs. SPWM technique is one of the most popular modulation techniques among the others applied in power switching inverters. In SPWM, a sinusoidal reference voltage waveform

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is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. The carrier signal in SPWM modulation technique typically has a frequency in the range up to 20 kHz. The switching angle of multi-switching control signal ($S_{sw}(t)$) of the inverter is calculated by Fourier series to eliminate selected harmonics as in (3);

$$S_{sw}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n \cos(n\omega t) + b_n \sin(n\omega t)) \qquad (3)$$

where a_0 is the average dc value of the switching signal [24]-[27].

This paper investigates a CHB-MLI with asymmetric voltage supplies and an improved modulator block to obtain 7-level output. In the proposed design, the CHB-MLI topology is supplied by various SDCSs at 1÷2 ratios as in hybrid topologies. The modulator block has been developed to generate more efficient switching signals according to regular SPWM at the output of modulator. The modulator block is based on generating 24 separate switching signals to control cascaded power block robustly. The switching orders are obtained comparing regular and phase dispositional carrier signals with modulating sinusoidal signals in the modulator block. The results obtained from simulation of Matlab-Simulink shows that the harmonic contents are greatly reduced by using mathematically well designed phase dispositional SPWM modulator. The accuracy of design will be verified with the results of continuing experimental studies.

II. ASYMMETRIC CASCADED TOPOLOGY OF MLI

A. Basic Principle of Multilevel Inverter and Design

Fig. 2 shows the main H-bridge cell of an inverter used for implementation of the multilevel inverter. The full bridge inverter module includes four power switches and four clamping diodes to form an H-bridge. A multilevel cascade inverter consists of a number of H-bridge cells that connected series per phase, and each module requires a separate DC source to generate voltage levels at the output of inverter. The switching inputs shown as $In_{1..4}$ in the Fig. 2 will allow obtaining output voltages of each H-bridge as follows;

$$V_{out} = \begin{cases} +V_{dc} & In1, In4 \quad on \\ 0V_{dc} & In1, In3 \quad on \\ -V_{dc} & In2, In3 \quad on \end{cases} \qquad (4)$$

The ratio of DC voltage source naturally affects the output levels of a cascade multilevel inverter. The considered full bridge module generates 3-level output voltage itself as seen in (4). The Fourier series expansion of the general multilevel stepped output voltage is shown in (5) and the transform is applied for Fig. 1 in (6), where n is the harmonic number of the output voltage of inverter.

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \begin{bmatrix} \cos(n\theta_1) + \cos(n\theta_2) + \ldots \\ +\cos(n\theta_5) \end{bmatrix} \frac{\sin(n\omega t)}{n} \qquad (5)$$

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2)] \frac{\sin(n\omega t)}{n} \qquad (6)$$

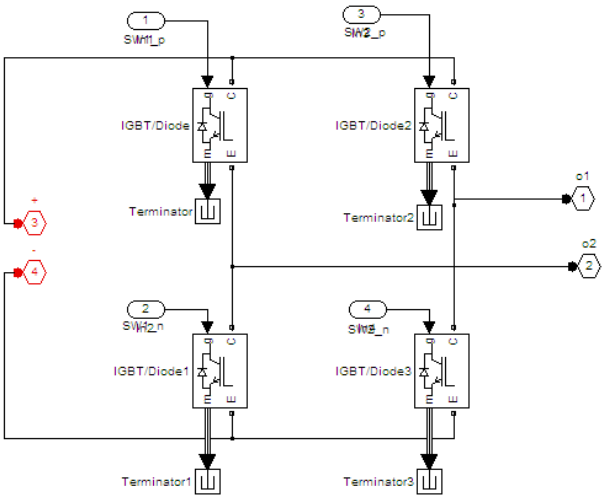

Fig. 2. Three-level full bridge module

The switching angles that are indicated as $\Theta_1 \ldots \Theta_5$ in (6) can be chosen to obtain minimum voltage harmonics. CHB-MLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared an interface with renewable energy sources due to using separate DC sources [18]-[19], [26].

Fig. 2 depicts one cell of the phase of Fig. 1. The first leg phase voltage (V_{an}) of Fig. 1 is constituted by multiplying V_{a1} and V_{a2} values of series connected H-bridge cells and will generate a stepped waveform as seen in Fig. 3. Positive output pulses are shown with P_1 and P_2 while the negative ones are indicated as P_1^1 and P_2^1.

B. The Power Block of Designed Multilevel Inverter

The cascaded MLI has been constituted using IGBT H-bridges which have $2V_{dc}$ supply at the upper side of phase legs and V_{dc} supply at the lower side. The complete design which contains switching devices and control block is depicted in Fig. 4. The cascaded MLI block is switched by the proposed 24-channel SPWM modulator to obtain 7-level output at the back-end of the 3-phase voltage source inverter. The SPWM modulator generates the control signals

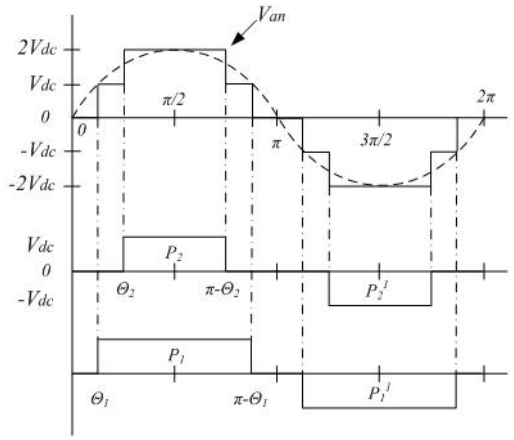

Fig. 3. Phase output voltage waveforms of a five-level topology CHB-MLI with 2 separate DC sources

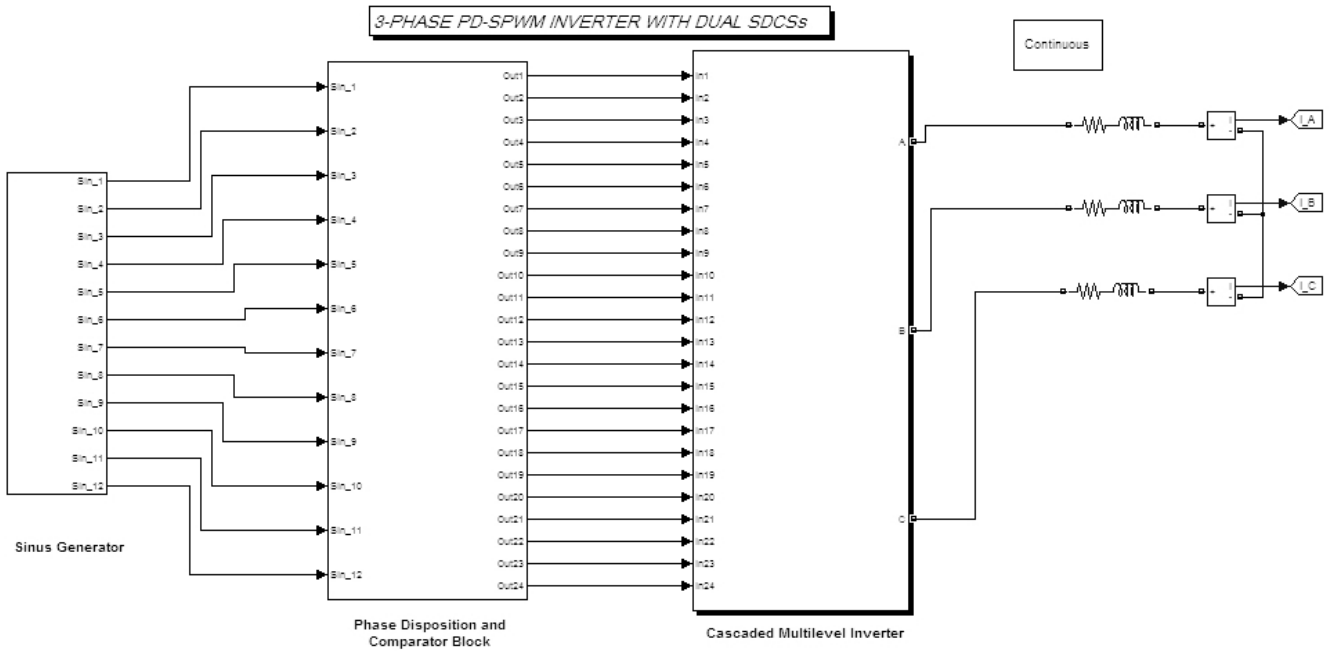

Fig. 4. The Simulink design of cascaded multilevel inverter containing SPWM modulator and Y-wired RL load

according to phase disposition (PD) carrier signals to calculate the most accurate switching angles. The cascaded MLI inverter block is shown in Fig. 5. The H-bridge cells are constituted as seen in Fig. 2 using IGBTs and parallel diodes to achieve fast and reliable switching cells. All the phase legs has dual switching cells which are controlled using complementary switching orders to generate a staircase voltage waveform at the output.

The output voltage waveform is generated according to addition of V_{out1} and V_{out2} as shown in (7) and (8). The switching orders of Fig. 2 has been utilized to indicate number of devices as $In_{1}\ldots_{4}$ for the upper H-bridge cell and $In_{1\_2\ldots4\_2}$ for the lower cell in a phase leg. The switching orders of Fig. 2 is utilized to indicate number of devices as $In_{1\ldots4}$ for the upper H-bridge cell and $In_{1\_2\ldots4\_2}$ for the lower cell in a phase leg. The output voltage of cascaded inverter is obtained by adding the output voltage of each cell and the staircase waveform illustrates 7-level output.

$$V_{out1} = \begin{cases} +V_{dc} & In_1, In_4 \quad on \\ 0V_{dc} & In_1, In_3 \quad on \\ -V_{dc} & In_2, In_3 \quad on \end{cases} \tag{7}$$

$$V_{out2} = \begin{cases} +2V_{dc} & In_{1\_2}, In_{4\_2} \quad on \\ 0V_{dc} & In_{1\_2}, In_{3\_2} \quad on \\ -2V_{dc} & In_{2\_2}, In_{3\_2} \quad on \end{cases} \tag{8}$$

The line-to-line voltage rates of inverter is determined according to modulation indexes (m_i), and working areas are defined as linear modulation ($m_i \leq 1$) or over-modulation ($m_i > 1$) ranges. The line-to-line voltages are limited to ($\sqrt{3}V_d/2$) of dc line in linear modulation range and to ($4/\pi$).($\sqrt{3}V_d/2$) in over- modulation range. The V_{dc} voltage is defined as 250 V while modulation index is between 0.6 and 1.4 to analyze linear and over modulation conditions. The load of MLI is selected a series RL load as values of 5 Ω resistance and 5 mH inductance. Various modulation frequencies in a band range of 1 kHz-10 kHz are applied to modulator block to determine minimum total harmonic distortion (THD) ratios of current THD (THD_i) and voltage THD (THD_v).

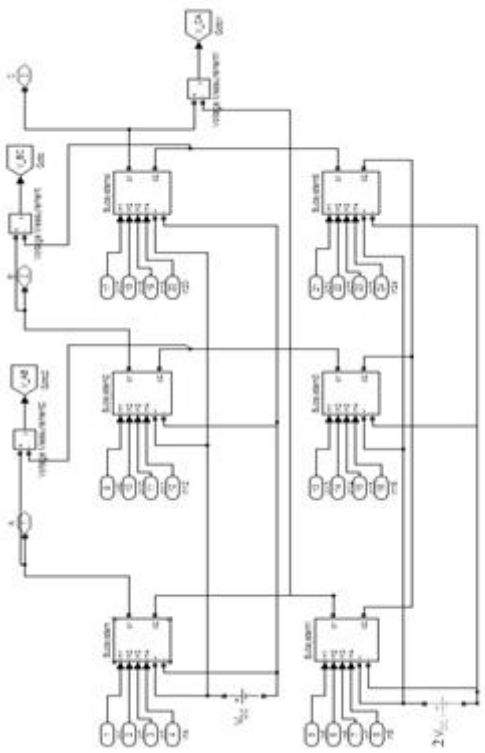

Fig.5. Block diagram of cascaded H-bridges with 2 separate DC sources

III. DESIGN OF MODULATOR BLOCK

The most well known SPWM which can be applied to cascaded multilevel inverters is phase shifted SPWM and is same as that of the conventional SPWM technique as seen in Fig. 3 of [28]. The multi-carrier SPWM control methods also are implemented to increase the performance of multilevel inverters and are classified according to vertical or horizontal arrangements of carrier signal. The vertical carrier distribution techniques are defined as Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD), while horizontal arrangement is known as Phase Shifted (PS) control technique [29]-[31].

The vertical multi-carrier modulation strategies do not increase the equivalent carrier frequency and can be utilized as proper modulation techniques for hybrid and asymmetric hybrid topologies. In the PD SPWM technique, the most significant harmonics are centered as the sidebands around the carrier frequency due to its co-phase components. The harmonic contents in the sidebands and at the center frequencies of carrier signals prevent the harmonic effect in the line voltage. For a voltage source SPWM controlled DC-AC inverter, the amplitude distortion of the PWM waveforms will decline the amplitude of the fundamental component and introduce unexpected low order harmonic contents as analyzed in [28].

The control signal patterns which switch the inverter block to generate $+V_{dc}$ and $+2V_{dc}$ levels at the output of Phase A has been depicted in Fig. 6. Fig. 6 (a) shows triangular carrier signals and modulating signal. Control signal of the upper H-bridge cell is generated according to comparing the first carrier and is shown in Fig. 6 (b) while the second carrier comparison result is illustrated in Fig. 6 (c). The left 22 modulating signals are generated according to this comparison algorithm and applied to inverter as being 8 control signals per phase.

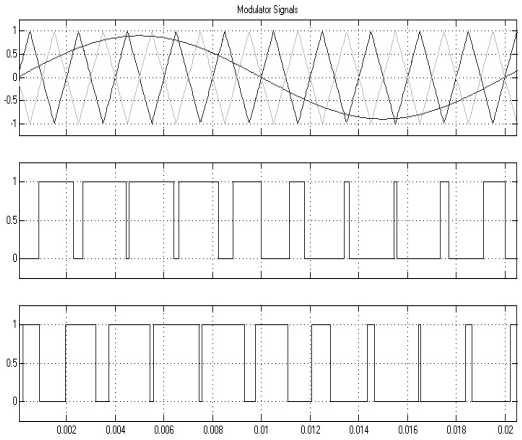

Fig. 6. Modulator signals (a) phase disposition carrier signals and modulating signal (b) SPWM output of 1st carrier (c) SPWM output of 2nd carrier

Fig. 7 shows the control signals of a phase generated by the phase disposition and modulator block in Matlab/Simulink. 1st and 3rd control signals are obtained according to initial carrier signal and 2nd and 4th signals are generated by comparing 2nd carrier with the modulating sinusoidal signal. The other four switching signals are achieved as negative complements of the first part of control signals.

Fig. 8 shows the line-to-line voltage output of cascaded MLI with PD-SPWM control algorithm. The output patterns are obtained using modulation index (m_i) value of 0.8 and the switching frequency (f_{sw}) is 2.5 kHz. The harmonic analyses for current and voltage of the proposed system is limited up to 50th harmonic according to recommendations of IEEE in THD analyze topics [32]. The THD_v ratio of the inverter is determined as 2.81% by controlling the MLI with designed PD modulator. The effects of modulation index and switching frequency on THD have been analyzed for various values to determine the most appropriate working conditions.

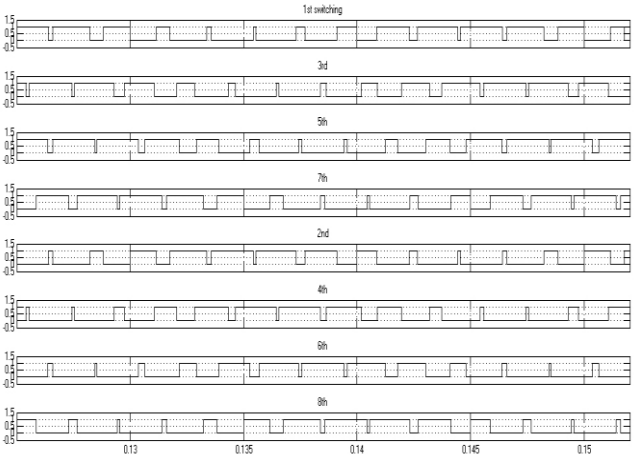

Fig. 7. Generated PD-SPWM switching signals for Phase A

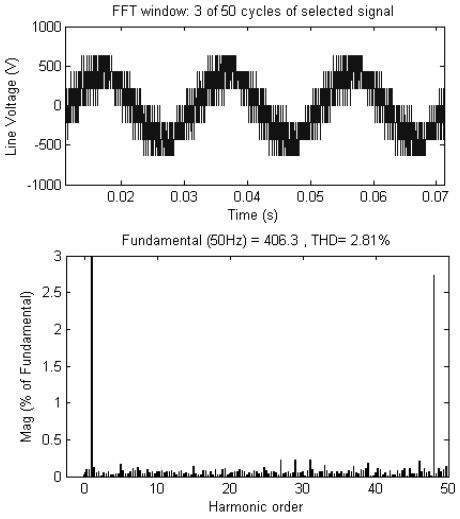

Fig. 8. 7-level line-to-line output voltage of inverter obtained at 2.5 kHz switching frequency

IV. HARMONIC ANALYSIS AND SIMULATION RESULTS

The mathematical model of PD-SPWM modulator has been developed in Simulink and the success on harmonic preventing has been compared to various working conditions.

The SPWM modulator has a switching bandwidth between 0- 20 kHz to control H-bridges and Fig. 9 shows the values which are obtained at 5 kHz switching conditions while m_i= 0.8. Fig. 9(a) and Fig. 9(b) represent the FFT analysis of the current THD (THD_i) and voltage THD (THD_v) ratios in Simulink. The lowest THD for current has been measured as 0.00% during 5 kHz switching frequency and m_i= 0.8 conditions. The switching frequency of SPWM modulator has been limited to 1-10 KHz, and modulation indexes are selected in $0.6 \leq m_i \leq 1.4$ ranges to analyze the effect of f_{sw} and m_i on THD of inverter. It has been observed by the performed tests that reducing the THD of current and voltage is depended on increasing the switching frequency in linear modulation range up to 5 kHz. The output voltage waveform has been distorted when the modulation ratio exceed 100 around 5 kHz as compared in Fig. 10 (a) and Fig. 10 (b). The THD for voltage has been measured as 0.42% while switching frequency was 10 kHz for m_i= 1 as shown in Fig. 10 (b). Fig. 11 (a) represents a pattern of FFT analyses which have been performed to constitute similar states as in the Fig. 10 (a) and (b). Fig. 11 (b), as another example, shows the THD for current at 10 kHz switching frequency, and the modulation index is 1 for both.

The harmonic analyses have shown that harmonic contents are depended on carrier frequency of the modulator. The lowest THD ratios for both of current and voltage have been obtained at the switching band over 2.5 kHz. The modulation index is effective on gain of inverter. The linear modulation area which is defined for $mi \leq 1$ condition is the trade-off border for harmonic elimination and gain. The increments of modulation index over 1 cause to increase harmonic contents at the output waveform of inverter. The nominal working conditions can be defined at the switching frequencies of 5 or 10 kHz while m_i=0.8 or m_i=1. The highest triplen harmonics THD of current have been measured as 0.1% as 3rd and 6th harmonics at switching frequencies up to 2.5 kHz, and 0% over 2.5 kHz switching conditions in linear modulation range.

V. CONCLUSIONS

In this paper, a three-phase 7-level cascaded multilevel inverter with phase disposition SPWM control has been presented, achieving output signals with high quality and very low THD owing to robustly designed mathematical model of multi-carrier modulator. The spectral errors, such as switching fall and rise times and the amplitude distortions of the SPWM waveforms which cause distortions at output signals have been reduced by using multi-carrier SPWM according to previous studies and literature. The switching actions have been modeled in Simulink by using interpolation processes to obtain properly queued modulation signals. The

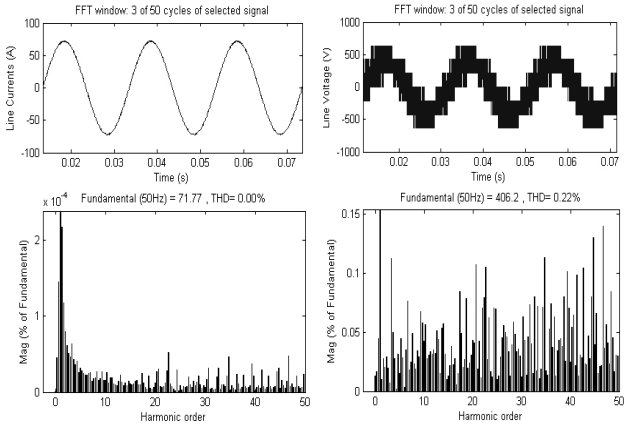

Fig. 9. THD analysis of inverter while f_{sw}= 5 kHz and m_i=0.8 (a) THD for current is 0.00% (b) THD for phase voltage is 0.22%

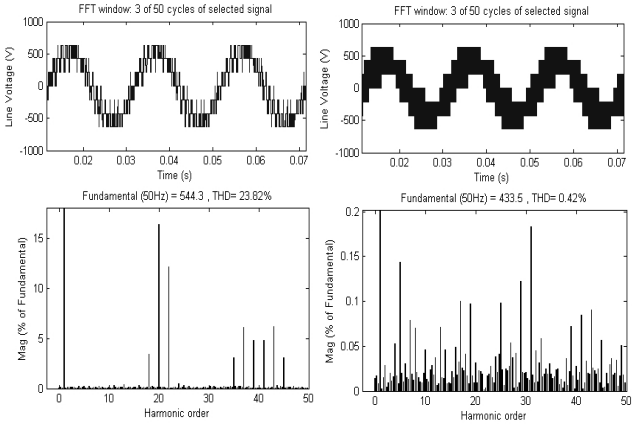

Fig. 10. THD voltage analysis while m_i=1 (a) THD for voltage is 23.82% at 1 kHz switching (b) THD for voltage is 0.42 % at 10 kHz switching

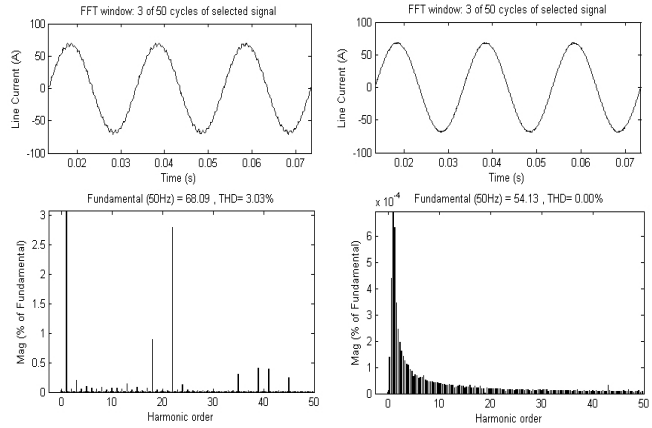

Fig. 11. THD current analysis while m_i=1 (a) THD for current is 3.03% at 1 kHz switching (b) THD for current is 0.0 % at 10 kHz switching

phase shift and disposition orders of modulating signals are another important point of design to reduce THD of line current and voltages. The switching orders are important due to transferring switching signals to semiconductors appropriately and also preventing DC bus short circuit. The inverter block has been designed using dual H-bridges per phase and the MLI design has been supplied by dual SDCSs instead of 6 supplies to decrease cost of experimental design. The DC level of H-bridges has been intended to construct output levels and dual DC supplies at $V_{dc} \div 2V_{dc}$ ratio have been constituted 7-level output voltage. The proposed model has been tested and compared to its precedent conventional models for THD rates and switching bandwidth. The measurement results have presented perfect outcomes on THD analysis. The modulation indexes in over modulation range have caused non linear changes in THD values of output current and voltages. On other hand, the THD of output current and voltages have seen extremely low in linear modulation range according to IEEE 519-1992 (THD<5%). It is also seen that the switching frequency is directly effective on THD. The increment in switching frequency has showed its reducer effect on THD of output current and voltages. In addition, the measured harmonic contents have seen as fundamental (50 Hz, 1st), 46th, and 48th harmonics over 2.5 kHz switching conditions of linear modulation area ($m_i \leq 1$). The lowest THD of output voltage has been measured as 0.22% in linear modulation band at 5 kHz switching frequency. The most effective harmonic contents of output current have seen lower than 0.1% at 46th and 48th in analysis. The accuracy of design will be verified with the results of continuing experimental studies.

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