Chapter 7

Cascaded H-Bridge Multilevel Inverters

7.1 INTRODUCTION

Cascaded H-bridge (CHB) multilevel inverter is one of the popular converter topologies used in high-power medium voltage (MV) drives [1–3]. It is composed of multiple units of single-phase H-bridge power cells. The H-bridge cells are normally connected in cascade on their ac side to achieve medium voltage operation and low harmonic distortion. In practice, the number of power cells in a CHB inverter is mainly determined by its operating voltage and manufacturing cost. For instance, in the MV drives with a rated line-to-line voltage of 3300 V, a seven-level inverter can be used, where the CHB inverter has a total of 12 power cells using 600 V class components [1]. The use of identical power cells leads to a modular structure, which is an effective means for cost reduction.

The CHB multilevel inverter requires a number of isolated dc supplies, each of which feeds an H-bridge power cell. The dc supplies are normally obtained from multipulse diode rectifiers presented in Chapter 3. For the seven- and nine-level inverters, 18- and 24-pulse diode rectifiers can be employed, respectively, to achieve low line-current harmonic distortion and high input power factor.

In this chapter, the single-phase H-bridge power cell, which is the building block for the CHB inverter, is reviewed. Various inverter topologies are introduced. Two carrier-based PWM schemes, phase-shifted and level-shifted modulations, are analyzed and their performance is compared. A staircase modulation with selective harmonic elimination is also presented.

High-Power Converters and AC Drives, Second Edition. Bin Wu and Mehdi Narimani.

7.2 H-BRIDGE INVERTER

Figure 7.2-1 shows a simplified circuit diagram of a single-phase H-bridge inverter. It is composed of two **inverter legs** with two IGBT devices in each leg. The inverter dc bus voltage V_d is usually fixed while its ac output voltage v_{AB} can be adjusted by either bipolar or unipolar modulation schemes.

7.2.1 Bipolar Pulse Width Modulation

Figure 7.2-2 shows a set of typical waveforms of the H-bridge inverter with bipolar modulation, where v_m is the sinusoidal modulating wave, v_{cr} is the triangular carrier wave, and v_{g1} and v_{g3} are the gate signals for the upper switches S_1 and S_3, respectively. The upper and the lower switches in the same inverter leg operate in a complementary manner with one switch turned on and the other turned off. Thus, we only need to consider two independent gate signals, v_{g1} and v_{g3}, which are generated by comparing v_m with v_{cr}. Following the same procedures given in Chapter 6, the waveforms of the inverter terminal voltages v_{AN} and v_{BN} can be derived, from which the inverter output voltage can be found from $v_{AB} = v_{AN} - v_{BN}$. Since the waveform of v_{AB} switches between the positive and negative dc voltages $\pm V_d$, this scheme is known as **bipolar modulation** [4].

The harmonic spectrum of the inverter output voltage v_{AB} normalized to its dc voltage V_d is shown in Fig. 7.2-2b, where V_{ABn} is the rms value of the nth order harmonic voltage. The harmonics appear as sidebands centered around the frequency modulation index m_f and its multiples such as $2m_f$ and $3m_f$. The voltage harmonics with the order lower than $(m_f - 2)$ are either eliminated or negligibly small. The switching frequency of the IGBT device, referred to as **device switching frequency** $f_{sw,dev}$ is equal to the carrier frequency f_{cr}.

Figure 7.2-3 shows the harmonic content of v_{AB} versus the amplitude modulation index m_a. The fundamental voltage V_{AB1} (rms) increases linearly with m_a. The

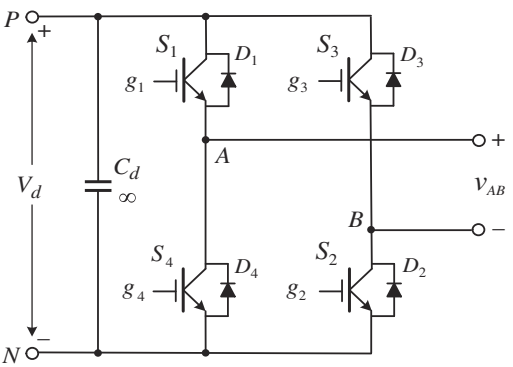


Figure 7.2-1 Single-phase H-bridge inverter.

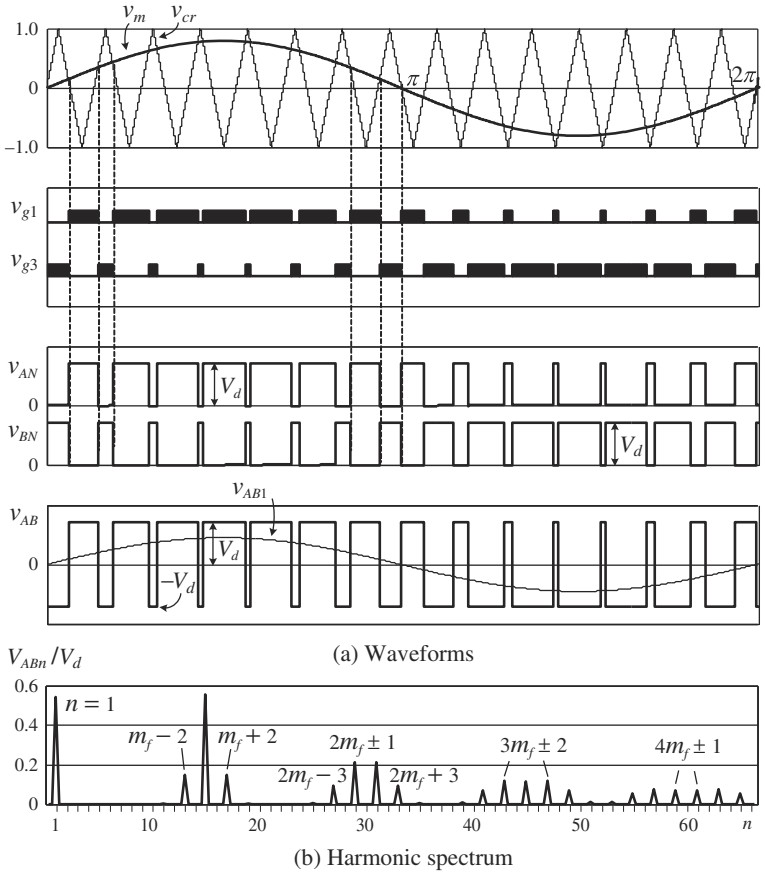


Figure 7.2-2 Bipolar PWM for the H-bridge inverter operating at $m_f = 15$, $m_a = 0.8$, $f_m = 60$ Hz, and $f_{cr} = 900$ Hz.

dominant harmonic m_f has a high magnitude, which is even higher than V_{AB1} for $m_a < 0.8$. This harmonic along with its sidebands can be eliminated by the unipolar pulse width modulation scheme.

7.2.2 Unipolar Pulse Width Modulation

The unipolar modulation normally requires two sinusoidal modulating waves, v_m and v_{m-}, which are of the same magnitude and frequency but 180° out of phase as shown in Fig. 7.2-4. The two modulating waves are compared with a common triangular carrier wave v_{cr}, generating two gating signals, v_{g1} and v_{g3}, for the upper switches, S_1 and S_3, respectively. It can be observed that the two upper switches do not commutate simultaneously, which is distinguished from the bipolar PWM where all four devices are commutated at the same time. The inverter output voltage v_{AB} switches either

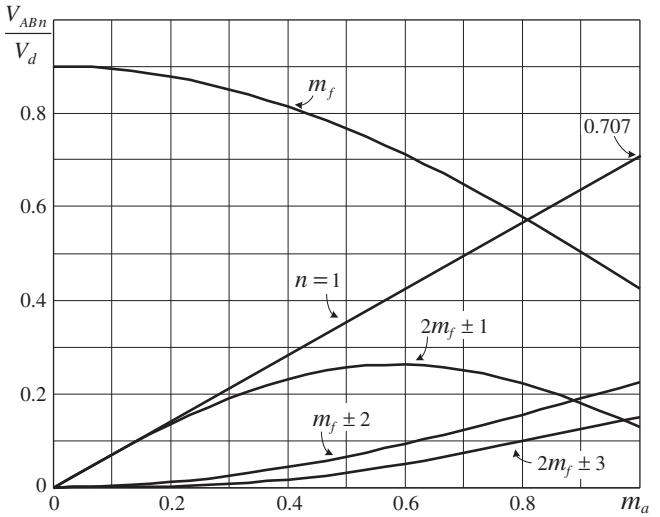


Figure 7.2-3 Harmonic content of v_{AB} produced by the H-bridge inverter with bipolar PWM.

between zero and $+V_d$ during the positive half cycle or between zero and $-V_d$ during the negative half cycle of the fundamental frequency. Thus, this scheme is known as **unipolar modulation** [4].

Figure 7.2-4b shows the harmonic spectrum of the inverter output voltage v_{AB}. The harmonics appear as sidebands centered around $2m_f$ and $4m_f$. The low-order harmonics generated by the bipolar modulation, such as m_f and $m_f \pm 2$, are eliminated by the unipolar modulation. The dominant harmonics are distributed around $2m_f$, and their frequencies are in the neighborhood of 1800 Hz. This is essentially the equivalent **inverter switching frequency** $f_{sw,inv}$, which is also the switching frequency seen by the load. Compared with the device switching frequency of 900 Hz, the inverter switching frequency is doubled. This phenomenon can also be explained from another perspective. The H-bridge inverter has two complementary switch pairs switching at 900 Hz. But the two pairs normally switch at different time instants, leading to $f_{sw,inv} = 2f_{sw,dev}$.

It is interesting to note that the dominant harmonics, $2m_f \pm 1$ and $2m_f \pm 3$, produced by the unipolar modulation have exactly the same magnitude as those generated by bipolar modulation. As a result, Fig. 7.2-3 can also be used to determine the magnitude of these harmonics at various m_a.

The unipolar modulation can also be implemented by using only one modulating wave v_m but two phase-shifted carrier waves, v_{cr} and v_{cr-}, as shown in Fig. 7.2-5. The two carrier waves are of same amplitude and frequency, but 180° out of phase. Switch S_1 is turned on by v_{g1} when $v_m > v_{cr}$ whereas S_3 is on when $v_m < v_{cr-}$. The waveform of v_{AB} is identical to that shown in Fig. 7.2-4. This modulation technique is often used in the CHB multilevel inverters.

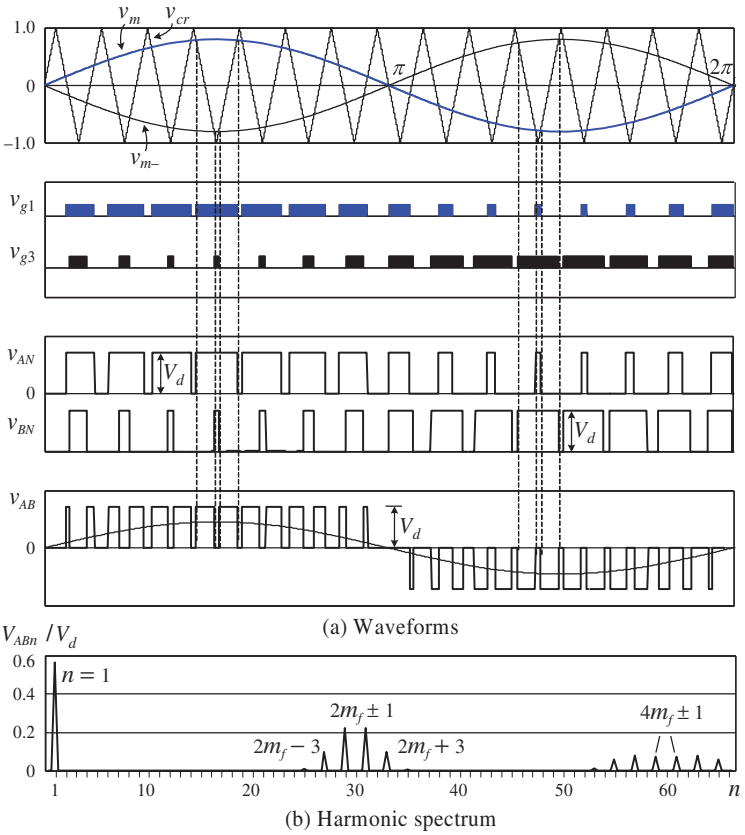


Figure 7.2-4 Unipolar PWM with two phase-shifted modulating waves ($m_f = 15$, $m_a = 0.8$, $f_m = 60$ Hz, and $f_{cr} = 900$ Hz).

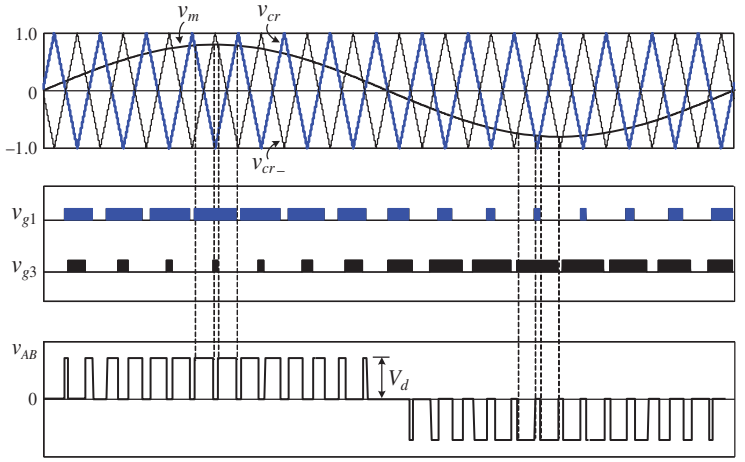


Figure 7.2-5 Unipolar PWM with two phase-shifted carriers ($m_f = 15$, $m_a = 0.8$, $f_m = 60$ Hz, and $f_{cr} = 900$ Hz).

7.3 MULTILEVEL INVERTER TOPOLOGIES

7.3.1 CHB Inverter with Equal DC Voltage

As the name suggests, the CHB multilevel inverter uses multiple units of H-bridge power cells connected in a series chain to produce high ac voltages. A typical configuration of a five-level CHB inverter is shown in Fig. 7.3-1, where each phase leg consists of two H-bridge cells powered by two isolated dc supplies of equal voltage E. The dc supplies are normally obtained by multipulse diode rectifiers discussed in Chapter 3.

The CHB inverter in Fig. 7.3-1 can produce a phase voltage with five voltage levels. When switches S_{11}, S_{21}, S_{12}, and S_{22} conduct, the output voltage of the H-bridge cells $H1$ and $H2$ is $v_{H1} = v_{H2} = E$, and the resultant **inverter phase voltage** is $v_{AN} = v_{H1} + v_{H2} = 2E$, which is the voltage at the inverter terminal A with respect to the inverter neutral N. Similarly, with S_{31}, S_{41}, S_{32}, and S_{42} switched on, $v_{AN} = -2E$. The other three voltage levels are E, 0, and $-E$, which correspond to various switching states summarized in Table 7.3-1. It is worth noting that the inverter phase voltage v_{AN} may not necessarily equal the **load phase voltage** v_{AO}, which is the voltage at node A with respect to the load neutral O.

It can be observed from Table 7.3-1 that some voltage levels can be obtained by more than one switching state. The voltage level E, for instance, can be produced by four sets of different (redundant) switching states. The switching state redundancy is a common phenomenon in multilevel converters. It provides a great flexibility for switching pattern design, especially for space vector modulation schemes.

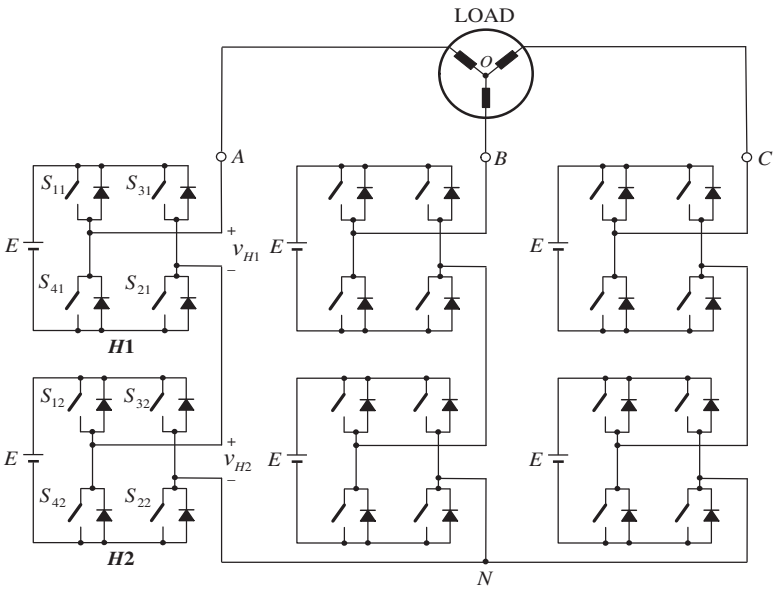


Figure 7.3-1 Five-level cascaded H-bridge inverter.

Table 7.3-1 Voltage Level and Switching State of the Five-Level CHB Inverter

Output Voltage v_{AN}	Switching State				v_{H1}	v_{H2}
	S_{11}	S_{31}	S_{12}	S_{32}		
$2E$	1	0	1	0	E	E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	1	1	1	0	0	E
	0	0	1	0	0	E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	$-E$
	0	1	1	0	$-E$	E
$-E$	0	1	1	1	$-E$	0
	0	1	0	0	$-E$	0
	1	1	0	1	0	$-E$
	0	0	0	1	0	$-E$
$-2E$	0	1	0	1	$-E$	$-E$

The number of voltage levels in a CHB inverter can be found from

$$m = (2H + 1) \tag{7.3-1}$$

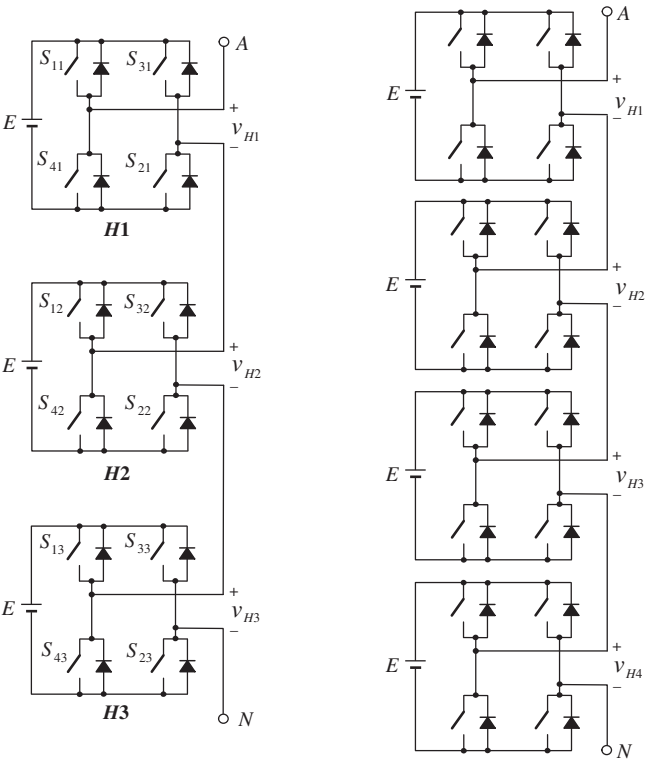
where H is the number of H-bridge cells per phase leg. The voltage level m is always an odd number for the CHB inverter while in other multilevel topologies such as diode-clamped inverters, it can be either an even or odd number.

The CHB inverter introduced above can be extended to any number of voltage levels. The per-phase diagram of seven- and nine-level inverters are depicted in Fig. 7.3-2, where the seven-level inverter has three H-bridge cells in cascade while the nine-level has four cells in series. The total number of active switches (IGBTs) used in the CHB inverters can be calculated by

$$N_{sw} = 6\,(m - 1) \tag{7.3-2}$$

7.3.2 H-Bridges with Unequal DC Voltages

The dc supply voltages of the H-bridge power cells introduced in the previous section are all the same. Alternatively, different dc voltages may be selected for the power



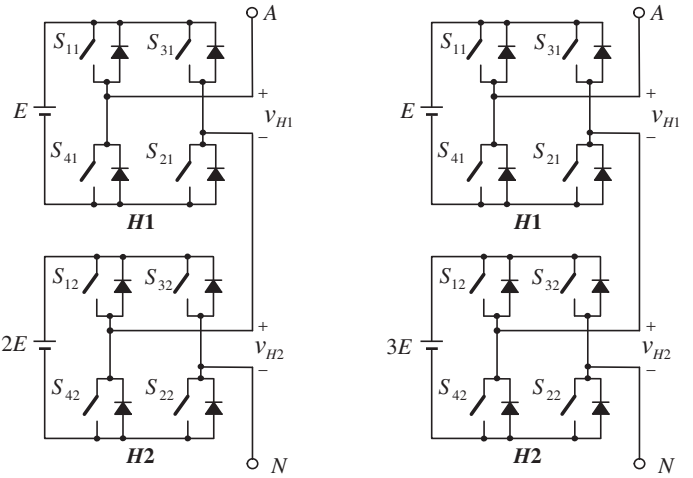
(a) Seven-level inverter (b) Nine-level inverter

Figure 7.3-2 Per-phase diagram of seven- and nine-level CHB inverters.

cells. With unequal dc voltages, the number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This allows more voltage steps in the inverter output voltage waveform for a given number of power cells [5, 6].

Figure 7.3-3 shows two inverter topologies, where the dc voltages for the H-bridge cells are not equal. In the seven-level topology, the dc voltages for $H1$ and $H2$ are E and $2E$, respectively. The two-cell inverter leg is able to produce seven voltage levels: $3E, 2E, E, 0, -E, -2E$, and $-3E$. The relationship between the voltage levels and their corresponding switching states is summarized in Table 7.3-2. In the nine-level topology, the dc voltage of $H2$ is three times that of $H1$. All the nine voltage levels can obtained by replacing the $H2$ output voltage of $v_{H2} = \pm 2E$ in Table 7.3-2 with $v_{H2} = \pm 3E$ and then calculating the inverter phase voltage v_{AN}.

There are some drawbacks associated with the CHB inverter using unequal dc voltages. The merits of the modular structure are essentially lost. In addition, switching pattern design becomes much more difficult due to the reduction in redundant switching states [5]. Therefore, this inverter topology has limited industrial applications.



(a) Two-cell seven-level topology

(b) Two-cell nine-level topology

Figure 7.3-3 Per-phase diagram of CHB inverters with unequal dc voltages.

Table 7.3-2 Voltage Level and Switching State of the Two-Cell Seven-Level CHB Inverter with Unequal dc Voltages

Output Voltage v_{AN}	Switching State				v_{H1}	v_{H2}
	S_{11}	S_{31}	S_{12}	S_{32}		
$3E$	1	0	1	0	E	$2E$
$2E$	1	1	1	0	0	$2E$
	0	0	1	0	0	$2E$
E	1	0	1	1	E	0
	1	0	0	0	E	0
	0	1	1	0	$-E$	$2E$
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
$-E$	1	0	0	1	E	$-2E$
	0	1	1	1	$-E$	0
	0	1	0	0	$-E$	0
$-2E$	1	1	0	1	0	$-2E$
	0	0	0	1	0	$-2E$
$-3E$	0	1	0	1	$-E$	$-2E$

7.4 CARRIER-BASED PWM SCHEMES

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: **phase-shifted** and **level-shifted modulations**. Both modulation schemes can be applied to the CHB inverters.

7.4.1 Phase-Shifted Multicarrier Modulation

In general, a multilevel inverter with m voltage levels requires $(m - 1)$ triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by

$$\varphi_{cr} = 360^\circ/(m - 1) \tag{7.4-1}$$

The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves.

Figure 7.4-1 shows the principle of the phase-shifted modulation for a seven-level CHB inverter, where six triangular carriers are required with a 60° phase displacement

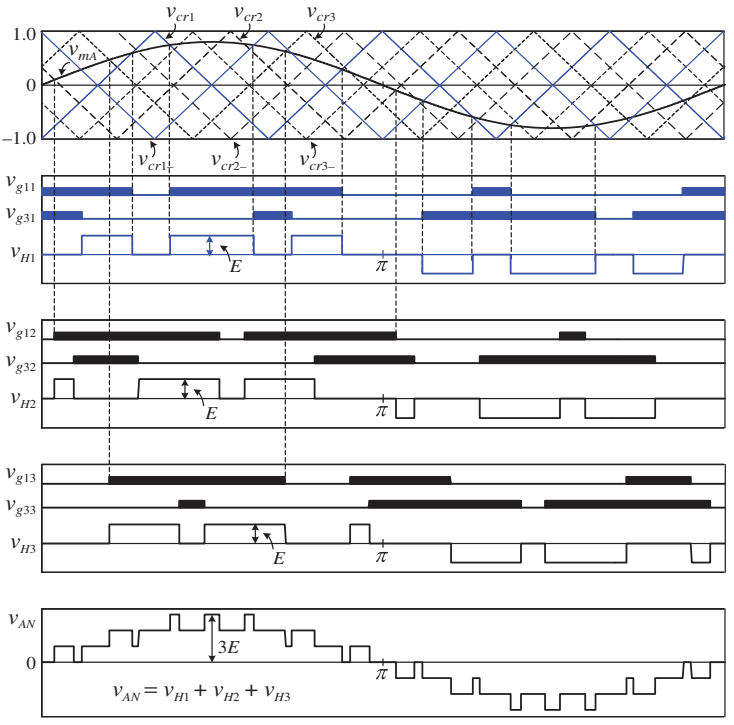


Figure 7.4-1 Phase-shifted PWM for seven-level CHB inverters ($m_f = 3$, $m_a = 0.8$, $f_m = 60$ Hz, and $f_{cr} = 180$ Hz).

between any two adjacent carriers. Of the three-phase sinusoidal modulating waves, only the phase A modulating wave v_{mA} is plotted for simplicity. The carriers v_{cr1}, v_{cr2}, and v_{cr3} are used to generate gatings for the upper switches S_{11}, S_{12}, and S_{13} in the left legs of power cells $H1, H2$, and $H3$ in Fig. 7.3-2a, respectively. The other three carriers, v_{cr1-}, v_{cr2-}, and v_{cr3-}, which are 180° out of phase with v_{cr1}, v_{cr2}, and v_{cr3}, respectively, produce the gatings for the upper switches S_{31}, S_{32}, and S_{33} in the right legs of the H-bridge cells. The gate signals for all the lower switches in the H-bridge legs are not shown since these switches operate in a complementary manner with respect to their corresponding upper switches.

The PWM scheme discussed above is essentially the unipolar modulation. As shown in Fig. 7.4-1, the gatings for the upper switches S_{11} and S_{31} in $H1$ are generated by comparing v_{cr1} and v_{cr1-} with v_{mA}. The $H1$ output voltage v_{H1} is switched either between zero and E during the positive half cycle or between zero and $-E$ during the negative half cycle of the fundamental frequency. The frequency modulation index in this example is $m_f = f_{cr}/f_m = 3$ and the amplitude modulation index is $m_a = \hat{V}_{mA}/\hat{V}_{cr} = 0.8$, where f_{cr} and f_m are the frequencies of the carrier and modulating waves, and $\hat{V}_{mA}$ and $\hat{V}_{cr}$ are the peak amplitudes of v_{mA} and v_{cr}, respectively.

The inverter phase voltage can be found from

$$v_{AN} = v_{H1} + v_{H2} + v_{H3} \tag{7.4-2}$$

where v_{H1}, v_{H2}, and v_{H3} are the output voltages of cells $H1, H2$, and $H3$, respectively. It is clear that the inverter phase voltage waveform is formed by seven voltage steps: $+3E$, $2E$, E, 0, $-E$, $-2E$, and $-3E$.

Figure 7.4-2 shows the simulated voltage waveforms and their harmonic content of the seven-level inverter operating under the condition of $f_m = 60$ Hz, $m_f = 10$, and $m_a = 1.0$. The device switching frequency can be calculated by $f_{sw,dev} = f_{cr} = f_m \times m_f = 600$ Hz, which is a typical value for the switching devices in high-power converters. The waveforms of v_{H1}, v_{H2}, and v_{H3} are almost identical except a small phase displacement caused by the phase-shifted carriers.

The waveform of v_{AN} is composed of seven voltage levels with a peak value of $3E$. Since the IGBTs in the different H-bridges do not switch simultaneously, the magnitude of voltage step change during switching is only E. This leads to a low *dv/dt* and reduced electromagnetic interference (EMI). The line-to-line voltage v_{AB} has 13 voltage levels with an amplitude of $6E$.

The harmonic spectrum for the waveforms of v_{H1}, v_{AN}, and v_{AB} is shown in Fig. 7.4-2b. The harmonics in v_{H1} appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$ and $6m_f$. The harmonic content of v_{H2} and v_{H3} is identical to that of v_{H1}, and thus not given in the figure. The inverter phase voltage v_{AN} does not contain any harmonics of the order lower than $4m_f$, which leads to a significant reduction in THD. The THD for v_{AN} is only 18.8% in comparison to 53.9% for v_{H1}. It can be observed that v_{AN} contains triplen harmonics such as $(6m_f \pm 3)$ and $(6m_f \pm 9)$. However, these harmonics do not appear in the line-to-line voltage v_{AB} due to the balanced three-phase system, resulting in a further reduction in THD to 15.5%.

As stated earlier, the frequency of the dominant harmonic in the inverter output voltage represents the inverter switching frequency $f_{sw,inv}$. Since the dominant

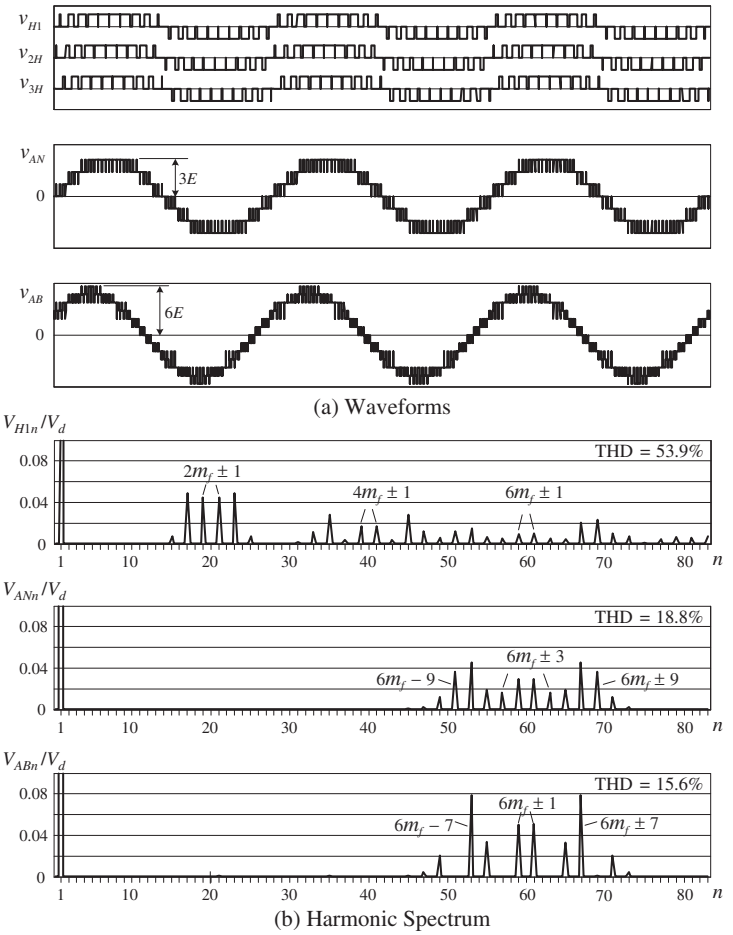


Figure 7.4-2 Simulated waveforms for a seven-level CHB inverter with phase-shifted PWM ($m_f = 10$, $m_a = 1.0$, $f_m = 60$ Hz, and $f_{cr} = 600$ Hz).

harmonics in v_{AN} and v_{AB} in Fig. 7.4-2 are distributed around $6m_f$, the inverter switching frequency can be found from $f_{sw,inv} = 6m_f \times f_m = 6f_{sw,dev}$, which is six times the device switching frequency. This is a desirable feature attained by the multilevel inverter since a high value of $f_{sw,inv}$ allows more harmonics in v_{AB} to be eliminated while a low value of $f_{sw,dev}$ helps to reduce device switching losses. In general, the switching frequency of the inverter using the phase-shifted modulation is related to the device switching frequency by

$$f_{sw,inv} = 2Hf_{sw,dev} = (m-1)f_{sw,dev} \tag{7.4-3}$$

The harmonic content of v_{AB} versus the modulation index m_a is shown in Fig. 7.4-3. Since the high-order harmonic components can be easily attenuated by filters or load inductances, only the dominant harmonics centered around $6m_f$ are plotted.

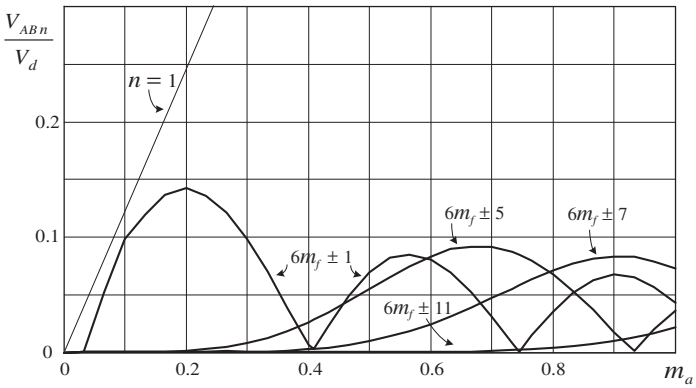


Figure 7.4-3 Harmonic content of v_{AB} produced by a seven-level CHB inverter with phase-shifted PWM.

The nth order harmonic voltage V_{ABn} (rms) is normalized with respect to the total dc voltage

$$V_d = \frac{m-1}{2}E \tag{7.4-4}$$

For a seven-level inverter, $V_d = 3E$. The maximum fundamental-frequency voltage can be found from

$$V_{AB1,\max} = 1.224V_d = 0.612(m-1)E \quad \text{for} \quad m_a = 1 \tag{7.4-5}$$

As discussed in Chapter 6, the maximum voltage $V_{AB1,\max}$ can be boosted by 15.5% by the **third harmonic injection method**. This technique can also be applied to the phase- and level-shifted modulation schemes for the CHB inverters.

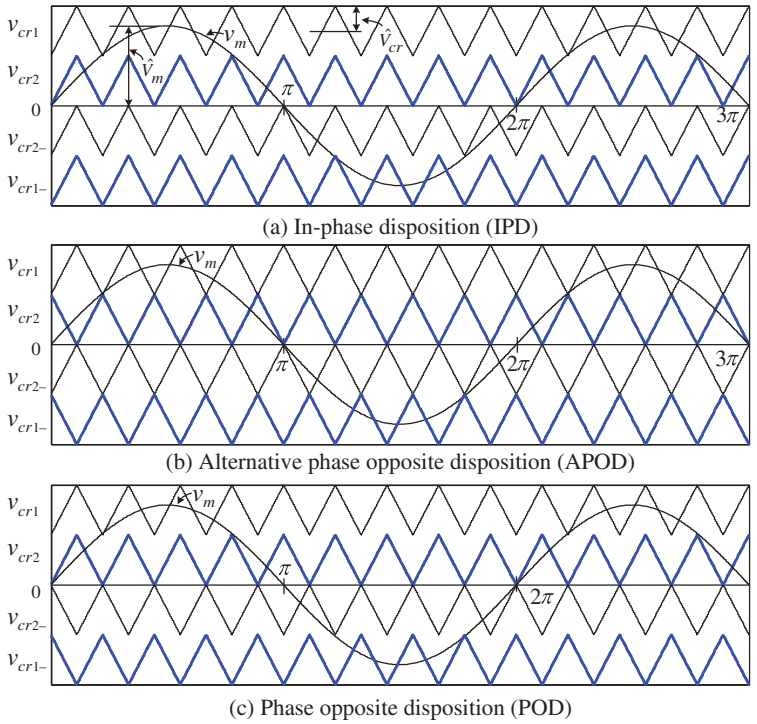
7.4.2 Level-Shifted Multicarrier Modulation

Similar to the phase-shifted modulation, an m-level CHB inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. The frequency modulation index is given by $m_f = f_{cr}/f_m$, which remains the same as that for the phase-shifted modulation scheme whereas the amplitude modulation index is defined as

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}(m-1)} \quad \text{for} \quad 0 \le m_a \le 1 \tag{7.4-6}$$

where $\hat{V}_m$ is the peak amplitude of the modulating wave v_m and $\hat{V}_{cr}$ is the peak amplitude of each carrier wave.

Figure 7.4-4 shows three schemes for the level-shifted multicarrier modulation: (a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase



(a) In-phase disposition (IPD)

(b) Alternative phase opposite disposition (APOD)

(c) Phase opposite disposition (POD)

Figure 7.4-4 Level-shifted multicarrier modulation for five-level inverters.

opposite disposition (APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. In what follows, only IPD modulation scheme is discussed since it provides the best harmonic profile of all three modulation schemes [7].

Figure 7.4-5 shows the principle of the IPD modulation for a seven-level CHB inverter operating under the condition of $m_f = 15$, $m_a = 0.8$, $f_m = 60$ Hz, and $f_{cr} = f_m \times m_f = 900$ Hz. The uppermost and lowermost carrier pair, v_{cr1} and v_{cr1-}, are used to generate the gatings for switches S_{11} and S_{31} in power cell $H1$ of Fig. 7.3-2a. The innermost carrier pair, v_{cr3} and v_{cr3-}, generate gatings for S_{13} and S_{33} in $H3$. The remaining carrier pair, v_{cr2} and v_{cr2-}, are for S_{12} and S_{32} in $H2$. For the carriers above the zero reference (v_{cr1}, v_{cr2}, and v_{cr3}), the switches S_{11}, S_{12}, and S_{13} are turned on when the phase A modulating signal v_{mA} is higher than the corresponding carriers. For the carriers below the zero reference (v_{cr1-}, v_{cr2-}, and v_{cr3-}), S_{31}, S_{32} and S_{33} are switched on when v_{mA} is lower than the carrier waves. The gate signals for the lower switches are complementary to their corresponding upper switches, and thus not shown for simplicity. The resultant H-bridge output voltage waveforms v_{H1}, v_{H2}, and v_{H3} are all unipolar as shown in Fig. 7.4-5. The inverter phase voltage waveform v_{AN} is formed with seven voltage levels.

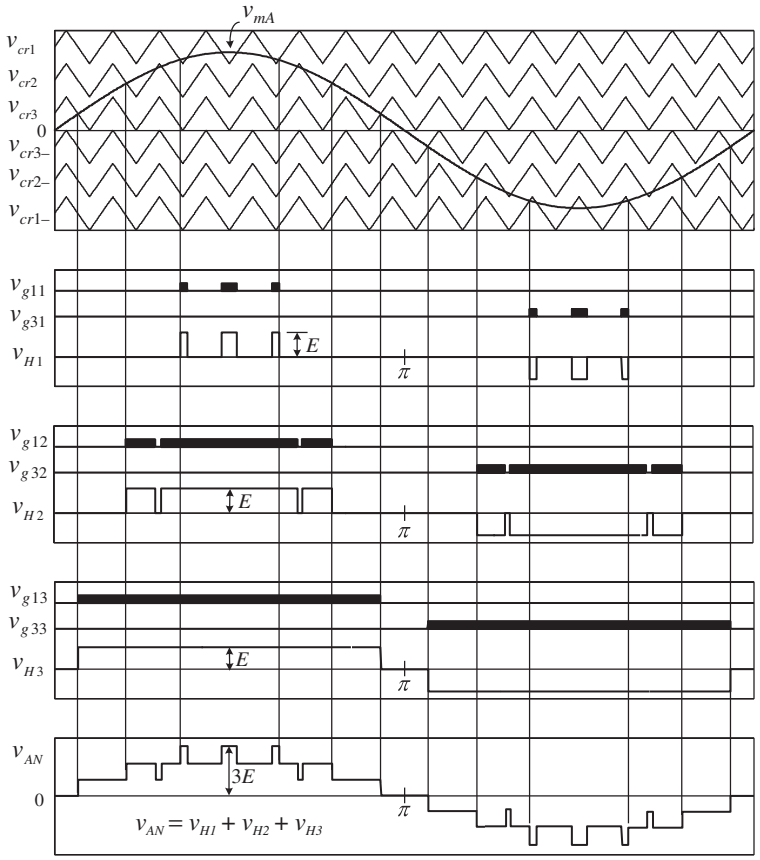


Figure 7.4-5 Level-shifted PWM for a seven-level CHB inverter ($m_f = 15$, $m_a = 0.8$, $f_m =$ 60 Hz, and $f_{cr} = 900$ Hz).

In the phase-shifted modulation, the device switching frequency is equal to the carrier frequency. This relationship, however, is no longer held true for the IPD modulation. For example, with the carrier frequency of 900 Hz in Fig. 7.4-5, the switching frequency of the devices in $H1$ is only 180 Hz, which is obtained by the number of gating pulses per cycle multiplied by the frequency of the modulating wave (60 Hz). Further, the switching frequency is not the same for all the devices. The switches in $H3$ are turned on and off only once per cycle, which translates into a switching frequency of 60 Hz. In general, the switching frequency of the inverter using the level-shifted modulation is equal to the carrier frequency, that is,

$$f_{sw,inv} = f_{cr} \tag{7.4-7}$$

from which the average device switching frequency is

$$f_{sw,dev} = f_{cr}/(m-1) \tag{7.4-8}$$

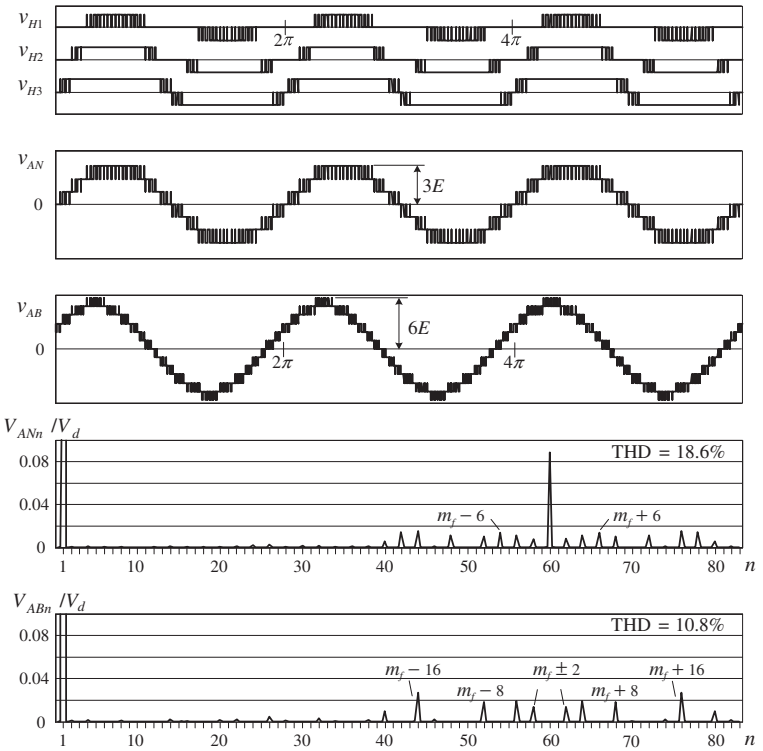


Figure 7.4-6 Simulated waveforms for a seven-level CHB inverter with IPD modulation ($m_f = 60$, $m_a = 1.0$, $f_m = 60$ Hz, $f_{cr} = 3600$ Hz, and $f_{sw,dev} = 600$ Hz).

In addition to the unequal device switching frequencies, the conduction time of the devices is not evenly distributed either. For example, the device S_{11} in $H1$ conduct much less time than S_{13} in $H3$ per cycle of the fundamental frequency. To evenly distribute the switching and conduction losses, the switching pattern should rotate among the H-bridge cells.

Figure 7.4-6 shows the simulated waveforms for a seven-level inverter operating under the condition of $m_f = 60$, $m_a = 1.0$, $f_m = 60$ Hz, and $f_{cr} = 3600$ Hz. Although the carrier frequency of 3600 Hz seems high for high-power converters, the average device switching frequency is only 600 Hz. The output voltages of the H-bridge cells, v_{H1}, v_{H2}, and v_{H3}, are all different, signifying that the IGBTs operate at different switching frequencies with various conduction times.

Similar to the voltage waveforms produced by the phase-shifted modulation, the inverter phase voltage v_{AN} is composed of seven voltage levels while the line-to-line voltage v_{AB} has thirteen voltage levels. The dominant harmonics in v_{AN} and v_{AB} appear as sidebands centered around m_f. The phase voltage contains triplen harmonics, such as m_f and $m_f \pm 6$, with m_f being a dominant harmonic. Since these harmonics do not appear in the line-to-line voltage, the THD of v_{AB} is only 10.8% in comparison

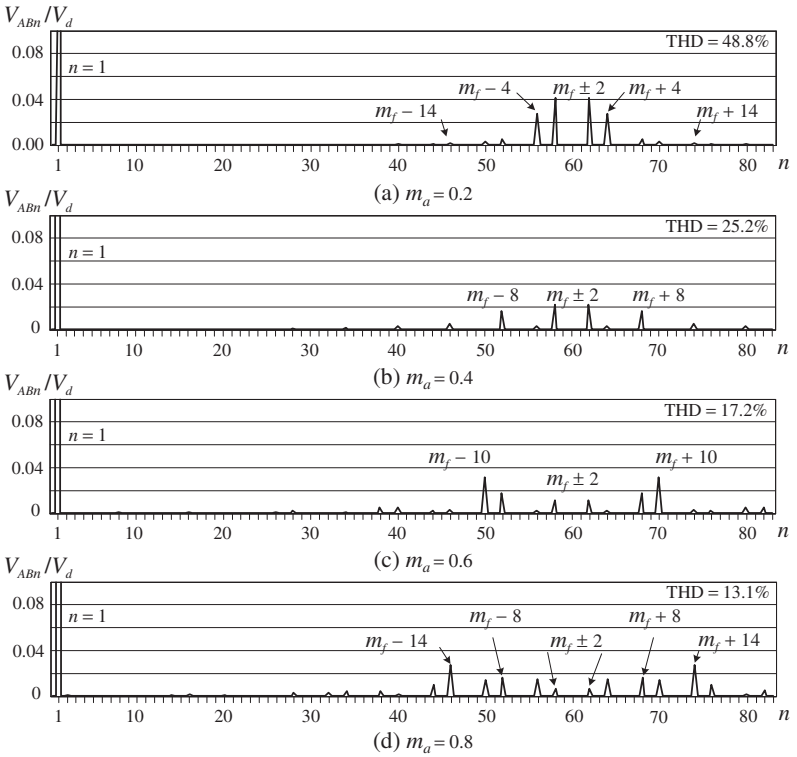


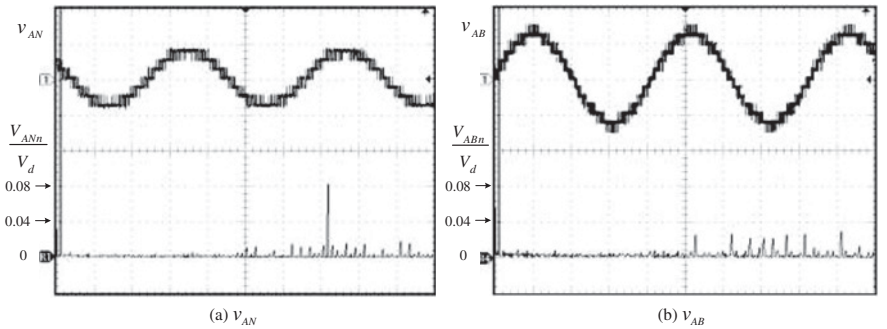
Figure 7.4-7 Harmonic content of v_{AB} produced by a seven-level CHB inverter with IPD modulation ($m_f = 60$, $f_m = 60$ Hz, $f_{cr} = 3600$ Hz, and $f_{sw,dev} = 600$ Hz).

to 18.6% for v_{AN}. The spectra of v_{AB} at other modulation indices m_a are shown in Fig. 7.4-7. The THD of v_{AB} decreases from 48.8% at $m_a = 0.2$ to 13.1% at $m_a = 0.8$.

The waveforms for v_{AN} and v_{AB} measured from a laboratory seven-level CHB inverter are illustrated in Fig. 7.4-8. The inverter operates under the condition of $m_f = 60$, $m_a = 1.0$, $f_m = 60$ Hz, and $f_{cr} = 3600$ Hz. The measured waveforms and their harmonic spectra are consistent with the simulation results shown in Fig. 7.4-6.

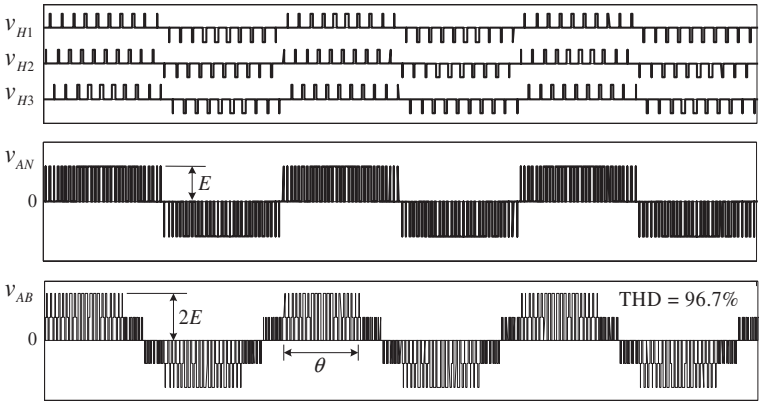
7.4.3 Comparison Between Phase- and Level-Shifted PWM Schemes

To compare the performance of phase- and level-shifted modulation schemes, it is assumed that the average switching frequency of the solid-state devices is the same for both schemes. Figure 7.4-9 shows the output voltage waveforms of a seven-level inverter operating with $f_{sw,dev} = 600$ Hz and $m_a = 0.2$, at which the differences between the two modulation schemes can be easily distinguished.

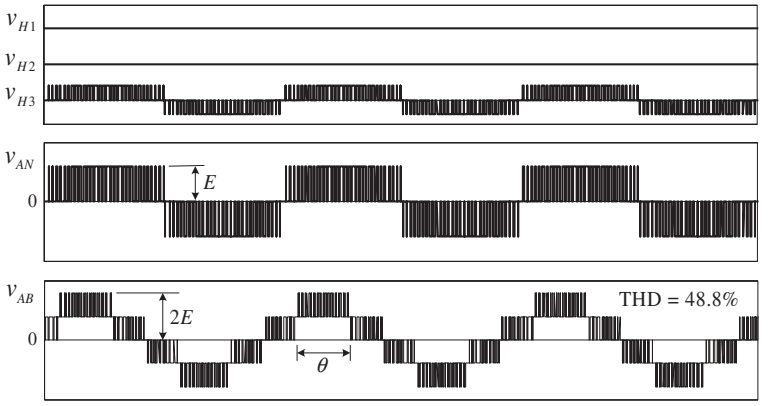


(a) v_{AN} (b) v_{AB}

Figure 7.4-8 Waveforms measured from a laboratory seven-level CHB inverter with IPD modulation ($m_f = 60$, $m_a = 1.0$, $f_m = 60$ Hz, $f_{cr} = 3600$ Hz, and $f_{sw,dev} = 600$ Hz).



(a) Phase-shifted modulation



(b) Level-shifted modulation (IPD)

Figure 7.4-9 Output voltage waveforms of the seven-level inverter operating at a low modulation index.

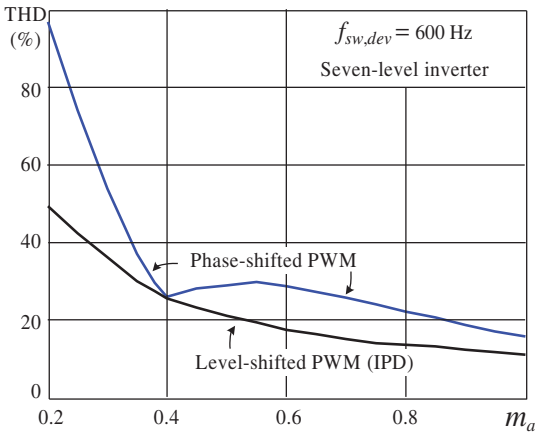


Figure 7.4-10 THD profile of v_{AB} produced by the seven-level CHB inverter with phase- and level-shifted modulation schemes.

The H-bridge output voltages, v_{H1}, v_{H2}, and v_{H3}, produced by the phase-shifted modulation are almost identical except for a small phase displacement among them. All the devices operate at the same switching frequency and conduction time. However, v_{H1} and v_{H2} produced by the level-shifted modulation are equal to zero and thus no switchings occur in power cells $H1$ and $H2$. The devices in $H3$ switch at the carrier frequency of 3600 Hz. To evenly distribute the switching and conduction losses, the switching pattern for the devices in the H-bridge cells should rotate.

The inverter phase voltage v_{AN} produced by both modulation schemes looks similar. It contains only three voltage levels instead of seven due to the low modulation index. The voltage levels of the inverter line-to-line voltage v_{AB} are reduced accordingly. Further, the THD of v_{AB} produced by the phase-shifted modulation is 96.7%, much higher than 48.8% for the level-shifted modulation. This is mainly caused by the waveform differences in the center portion of the positive and negative half cycles of v_{AB}.

Figure 7.4-10 shows the THD profile of the line-to-line voltage v_{AB} modulated by the phase- and level-shifted schemes. A summary of the carrier-based modulation schemes for the CHB multilevel inverters is given in Table 7.4-1.

Table 7.4-1 Comparison Between the Phase- and Level-Shifted PWM Schemes

Comparison	Phase-Shifted Modulation	Level-Shifted Modulation (IPD)
Device switching frequency	Same for all devices	Different
Device conduction period	Same for all devices	Different
Rotating of switching patterns	Not required	Required
Line-to-line voltage THD	Good	Better

7.5 STAIRCASE MODULATION

The staircase modulation can be easily implemented for the CHB inverter due to its unique structure [8, 9]. The principle of this modulation scheme is illustrated in Fig. 7.5-1, where v_{H1}, v_{H2}, and v_{H3} are the output voltages of the H-bridge cells in a seven-level inverter shown in Fig. 7.3-2a. The inverter phase voltage v_{AN} is formed by a seven-level staircase.

The waveform of v_{AN} can be expressed in terms of Fourier series as

$$v_{AN} = \frac{4E}{\pi} \sum_{n=1,3,5...}^{\infty} \frac{1}{n} \{\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)\} \sin(n\omega t) \quad \text{for}$$
$$0 \le \theta_3 < \theta_2 < \theta_1 \le \pi/2 \tag{7.5-1}$$

where n is the harmonic order, and θ_1, θ_2, and θ_3 are the independent switching angles. The coefficient $4E/\pi$ represents the peak value of the maximum fundamental voltage $\hat{V}_{H,\max}$ of an H-bridge cell, which occurs when the switching angle θ_1 of v_{H1}, for example, reduces to zero.

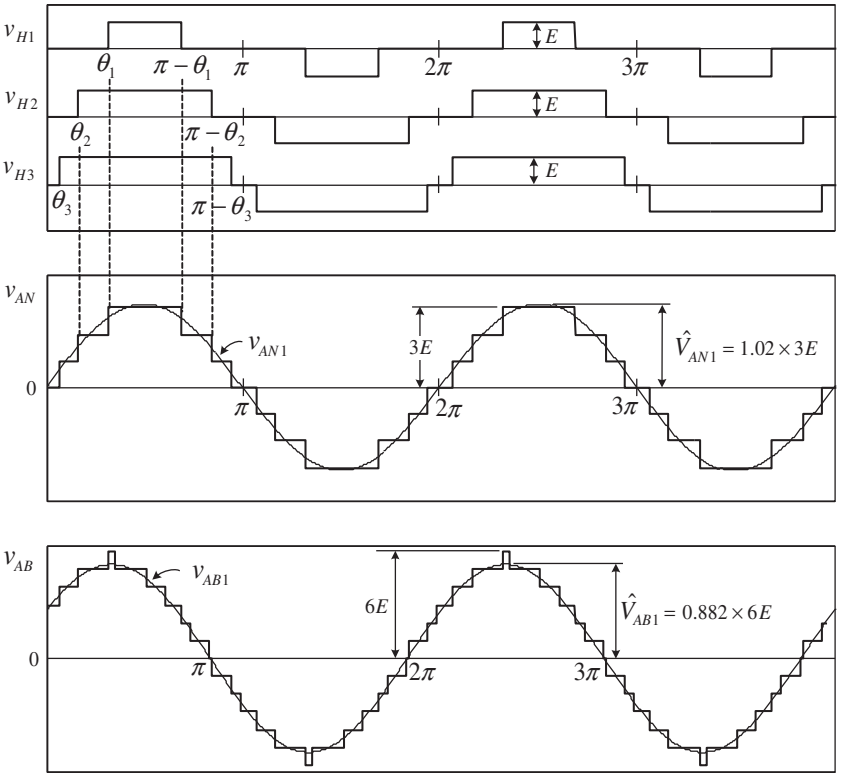


Figure 7.5-1 Staircase modulation with 5th and 7th harmonic elimination ($m_a = 0.8$).

The three independent angles can be used to eliminate two harmonics in v_{AN} and also provide an adjustable modulation index, defined by

$$m_a = \frac{\hat{V}_{AN1}}{H \times \hat{V}_{H,\max}} = \frac{\hat{V}_{AN1}}{H \times 4E/\pi} \tag{7.5-2}$$

where $\hat{V}_{AN1}$ is the peak value of the fundamental inverter phase voltage v_{AN1} and H is the number of H-bridge cells per phase.

For the seven-level CHB inverter with 5th and 7th harmonic elimination, the following equations can be formulated

$$\begin{cases} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = 3m_a \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \end{cases} \tag{7.5-3}$$

from which

$$\theta_1 = 57.106°,\ \theta_2 = 28.717°, \quad \text{and} \quad \theta_3 = 11.504° \quad \text{for} \quad m_a = 0.8 \tag{7.5-4}$$

The inverter output voltage waveforms based on (7.5-4) are shown in Fig. 7.5-1, and their spectrum is illustrated in Fig. 7.5-2. The waveform of v_{AN} does not contain the 5th or 7th harmonics and its THD is 12.5%. The inverter line-to-line voltage v_{AB} does not have any triplen harmonics such as 3rd, 9th, and 15th, resulting in a further reduction in THD.

The staircase modulation scheme is simple to implement. All the switching angles can be calculated off-line and then stored in a look-up table for digital implementation. Compared with the carrier-based PWM schemes, the staircase modulation features low switching losses since all the IGBTs operate at the fundamental frequency.

It is worth noting that the equations such as (7.5-3) for the switching angle calculation are nonlinear and transcendental, and thus may not always have a valid

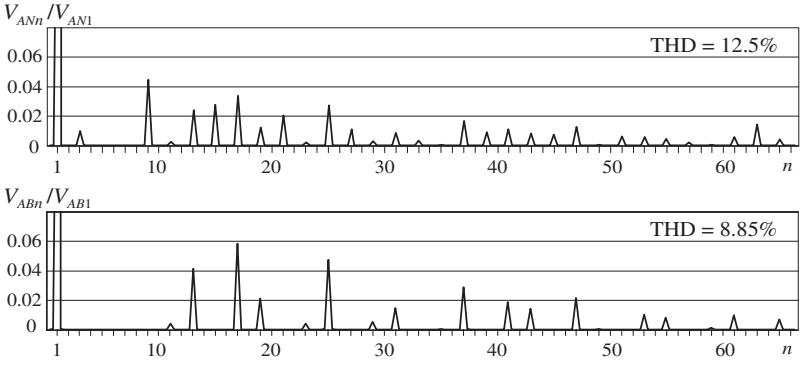


Figure 7.5-2 Harmonic spectrum for the waveforms of v_{AN} and v_{AB} in Fig. 7.5-1

solution over the full range of m_a [10]. When it happens, the switching angles should be calculated to minimize the magnitude of those harmonics that cannot be eliminated.

7.6 SUMMARY

This chapter focuses on the configurations and modulation schemes for the CHB multilevel inverters. The inverter is mainly composed of a number of identical CHB power cells. In practice, the number of H-bridge cells in a CHB inverter is primarily determined by the inverter operating voltage, harmonic requirements, and manufacturing cost. The CHB inverter with 7–11 voltage levels has been increasingly used in high-power medium (MV) voltage drives, where the low-voltage (1200 V or 1700 V) IGBTs are normally used as switching devices.

Two multi-carrier-based PWM schemes, the phase- and level-shifted modulations, are presented. Various aspects associated with the modulation schemes for the CHB multilevel inverters are discussed, which include gate signal arrangements, spectrum analyses, and THD profiles. The performance of the modulation schemes is compared. Another commonly used modulation technique, space vector modulation, is not discussed in this chapter. The reader can refer to Chapters 6 and 8 for details.

The CHB multilevel inverter has a number of features and drawbacks, including:

- Modular structure. The multilevel inverter is composed of multiple units of identical H-bridge power cells, which leads to a reduction in manufacturing cost.
- Lower voltage THD and *dv/dt*. The inverter output voltage waveform is formed by several voltage levels with small voltage steps. Compared with a two-level inverter, the CHB multilevel inverter can produce an output voltage with much lower THD and *dv/dt.*
- High voltage operation without switching devices in series. The H-bridge power cells are connected in cascade to produce high ac voltages. The problems associated with equal voltage sharing for series-connected devices are avoided.
- Large number of isolated dc supplies. The dc supplies for the CHB inverter are usually obtained from a multipulse diode rectifier employing an expensive phase-shifting transformer.
- High component count. The CHB inverter uses a large number of IGBTs. A nine-level CHB inverter requires 48 IGBTs with the same number of gate drivers.

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