



HPCA-19 Call for Papers

19th International Symposium on **High-Performance Computer Architecture**

ShenZhen, China, February 23-27, 2013

General Chair

Lixin Zhang, ICT/Chinese Academy of Sciences

Program Chair

Dean M. Tullsen, University of California, San Diego

Program Committee TBD

Financial Chair

Rajeev Balasubramonian, University of Utah Yinhe Han, ICT/Chinese Academy of Sciences

Local Arrangement Chair

Shengzhong Feng, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences Guoliang Chen, Shenzhen University

Publicity Chair

Onur Mutlu, Carnegie Mellon University Zane Wei, Huawei Technologies Co. Ltd. Xiaoyao Liang, Shanghai JiaoTong University

Publications Chair

Zhibin Yu, Huazhong University of Science and Technology

Registration Chair

Evan Speight, IBM Austin Research Lab Junmin Wu, University of Science and Technology of China

Workshop/Tutorial Chair

Mattan Erez, University of Texas at Austin Binyu Zang, Fudan University

Web Chair

Rui Hou, ICT/Chinese Academy of Sciences

Submission Chair

Hung-Wei Tseng, University of California, San Diego

Industry Session Chair TBD

Steering Committee

Antonio Gonzalez, Intel and UPC David Brooks, Harvard Laxmi Bhuyan, UC Riverside Pradip Bose, IBM Research David Christie, AMD Chita Das, Penn State Matthew Jacob, IISc Bangalore Daniel A. Jim énez, University of Texas at San Antonio David Kaeli, Northeastern University David Koppelman, LSU Shubu Mukherjee, Cavium Networks Yale Patt, University of Texas at Austin Josep Torrellas, University of Illinois, Urbana-Champaign

http://www.hpcaconf.org/hpca19 (collocated with PPoPP-2013 and CGO-2013)

The International Symposium on High-Performance Computer Architecture provides a high-quality forum for scientists and engineers to present their latest research findings in this rapidly-changing field. Authors are invited to submit papers on all aspects of high-performance computer architecture. Topics of interest include, but are not limited to:

- Processor, cache, and memory architectures
- Parallel computer architectures
- Multicore architectures
- Impact of technology on architecture
- Power-efficient architectures and techniques
- Dependable/secure architectures
- High-performance I/O systems
- Embedded and reconfigurable architectures
- Interconnect and network interface architectures
- Architectures for cloud-based HPC
- Innovative hardware/software trade-offs
- Impact of compilers and system software on architecture
- Performance modeling and evaluation
- Architectures for emerging technology and applications

Authors should submit an abstract by Thursday, August 30, 2012, 11:59 PM EDT. They should submit the full version of the paper by Friday, September 7, 2012, 11:59 PM EDT. No extensions will be granted. The full version should be a PDF file that does not exceed 25 pages according to the instructions in http://www.hpcaconf.org/hpca19. Papers that exceed the length limit or that cannot be viewed using Adobe Reader (version 3.0 or higher) may not be reviewed. Papers should be submitted for double-blind review. We anticipate making a Best Paper award; all papers will be evaluated based on their novelty, fundamental insights, and potential for long-term impact. Newidea papers are encouraged. Submission issues should be directed to the program chair at <tullsen@cs.ucsd.edu>. Workshop and tutorial submissions directed to the workshop and tutorial (mattan.erez@mail.utexas.edu, byzang@fudan.edu.cn). HPCA-19 will host an *Industrial Paper Session* presenting novel insights from industry (see Call for Industry Papers at http://www.hpcaconf.org/hpca19).

Accepted papers will be published in the conference proceedings distributed to conference attendees. Papers will also be uploaded to IEEE Xplore.

Important dates

- Abstract deadline: August 30, 2012, 11:59 PM EDT (firm deadline)
- Paper deadline: September 7, 2012, 11:59 PM EDT (firm deadline)
- Workshop and tutorial proposals due: September 7, 2012
- Notification of paper outcome: November 13, 2012



Sponsored by the IEEE Computer Society TC on Computer Architecture