Nanosystems Design and Tools

Pierre-Emmanuel Gaillardon
Department of Electrical and Computer Engineering – University of Utah

Architecture Reading Group
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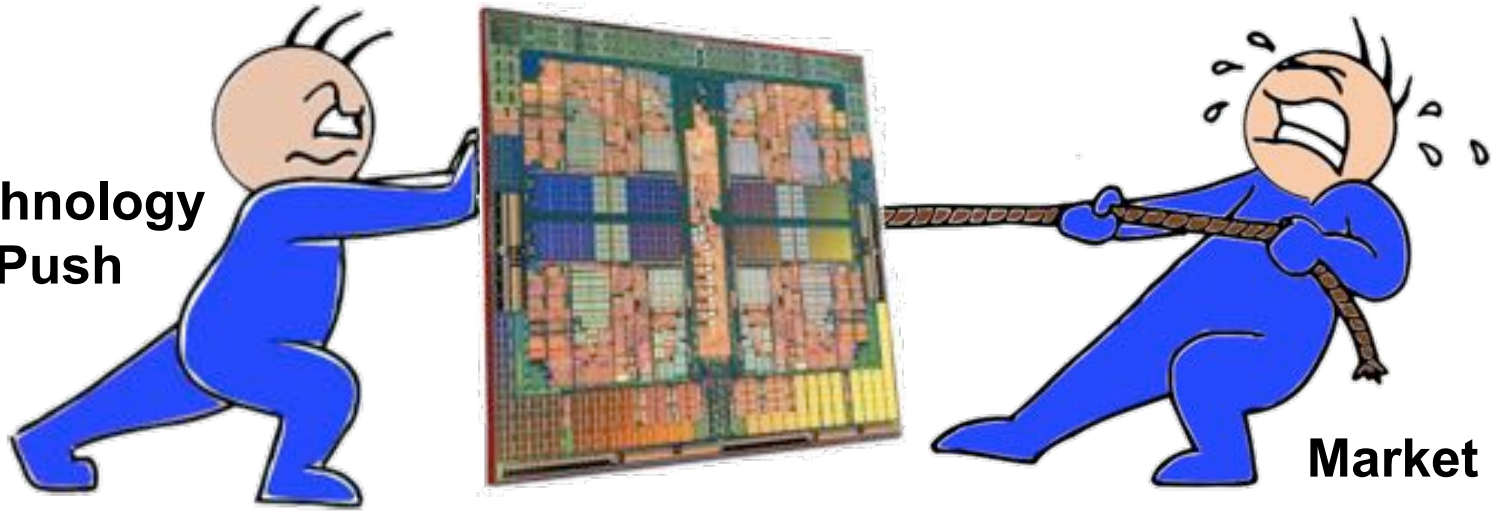
A Novel Offer for Microelectronics



Keeping the pace towards more functionality

"Increase the numbers of devices per area unit"

"Increase the device capabilities for a given area"

Functionality-Enhanced Devices

"Increase the circuit capabilities for a given area"

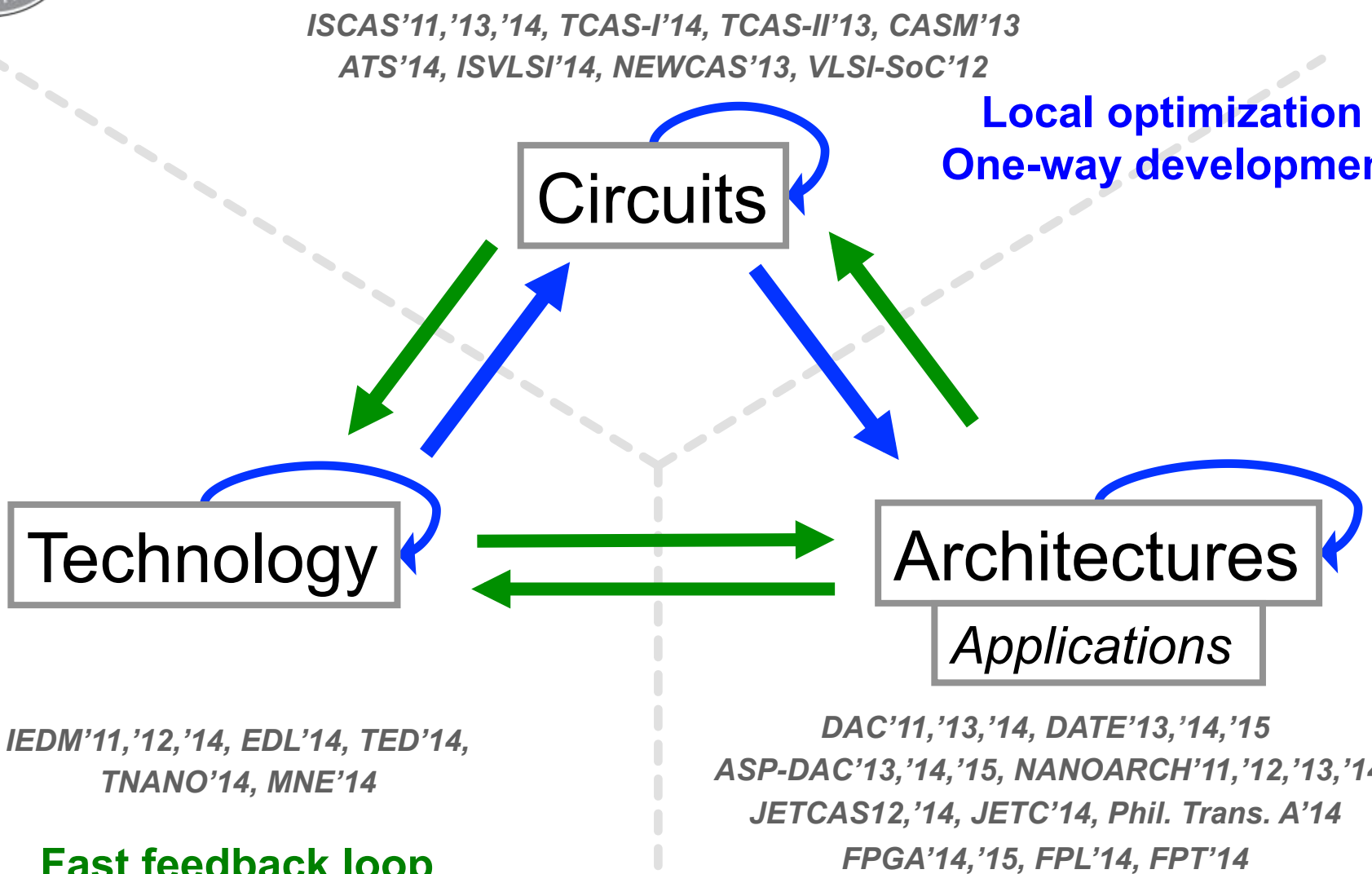
Functionality-Enhanced Circuits

Inspired from

Novel EDA

Inspiring

A Transversal Research Methodology



Outline

- Introduction
- Functionality-enhanced Devices
  - Controllable-polarity transistors: concept and fabrication
  - Circuit design and associated physical design
- Emerging *Electronic Design Automation* techniques
  - Biconditional Binary Decision Diagrams (BBDDs)
  - Majority Inverter Graphs (MIGs)
  - Application to reconfigurable logic architectures
- Functionality-enhanced Circuits
  - RRAM: A low-power system enabler
  - RRAM-based FPGA design
- Conclusion

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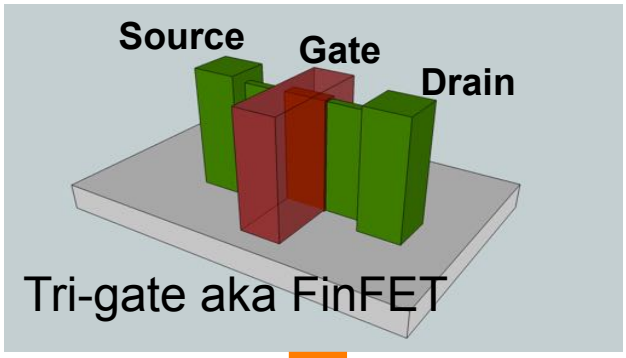
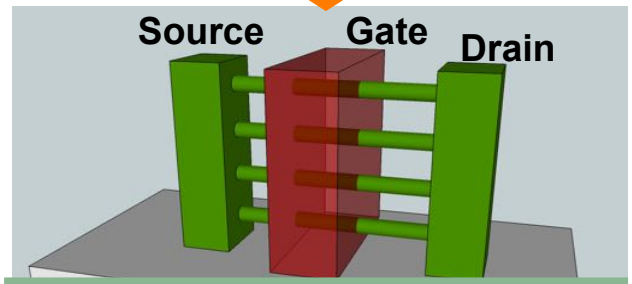
What is hidden behind Doped S/D CMOS ?

Ultimate Devices





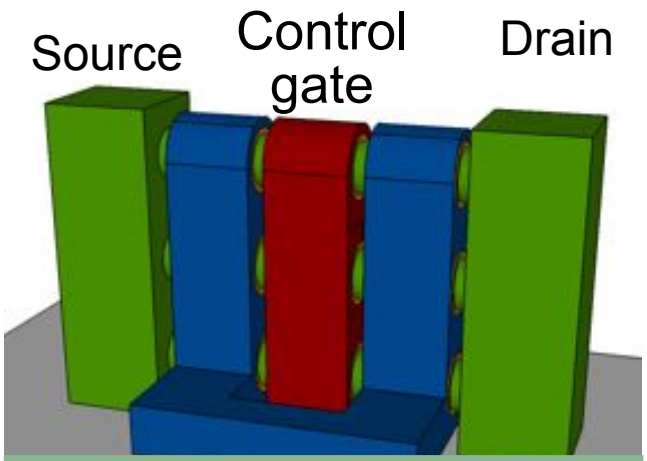
1D Transistors
Vertical Stacked Nanowires
Gate-All-Around Structures

Novel Conduction Properties

Ambipolar Conduction

n-type and *p*-type carriers

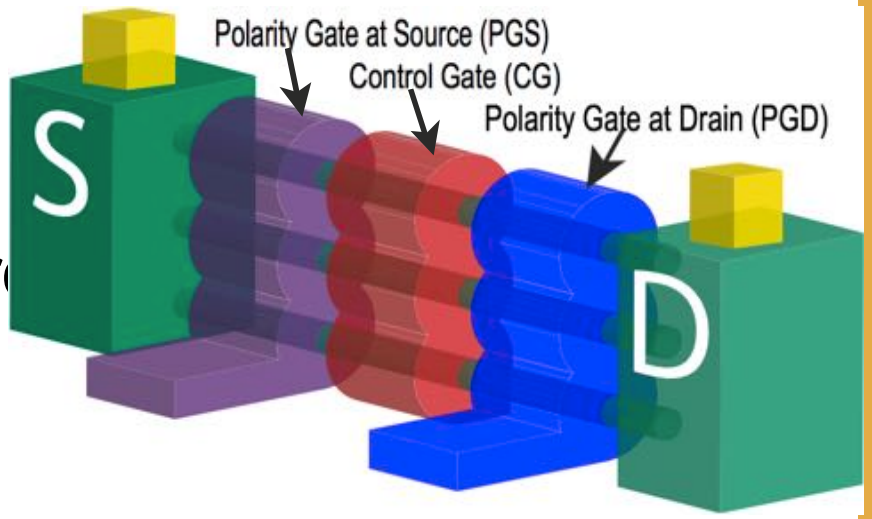
CONTROL IT

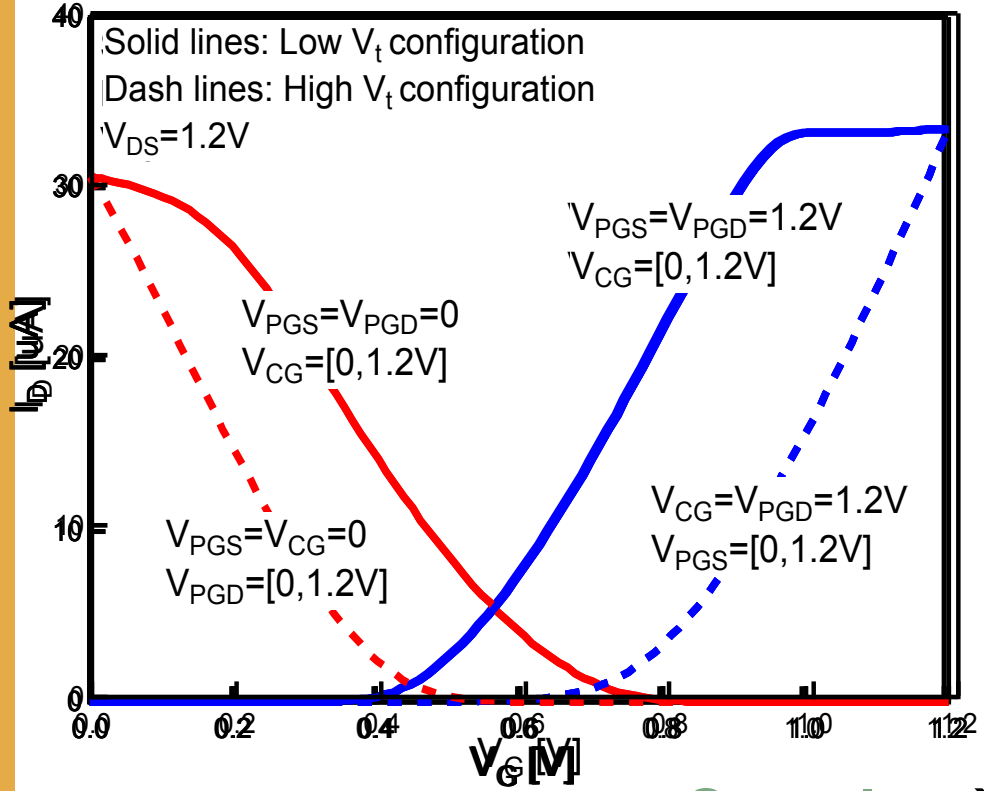


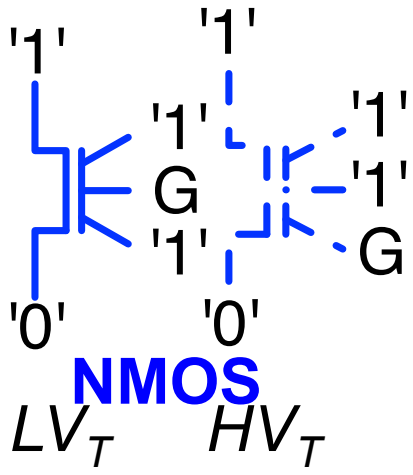
Enhanced Functionality
In-field reconfiguration

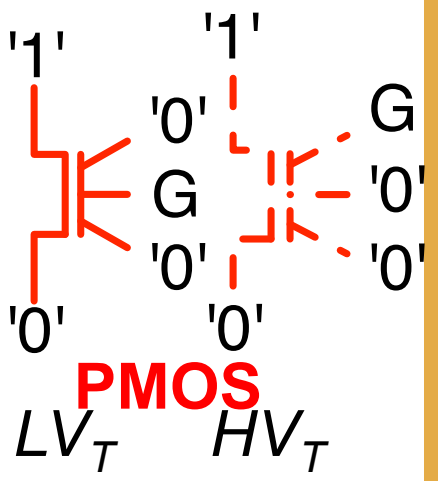
Multiple-Independent-Gate SiNWFET

- 3-independent gate regions
- Schottky barriers at S and D
- Polarity and Threshold contr





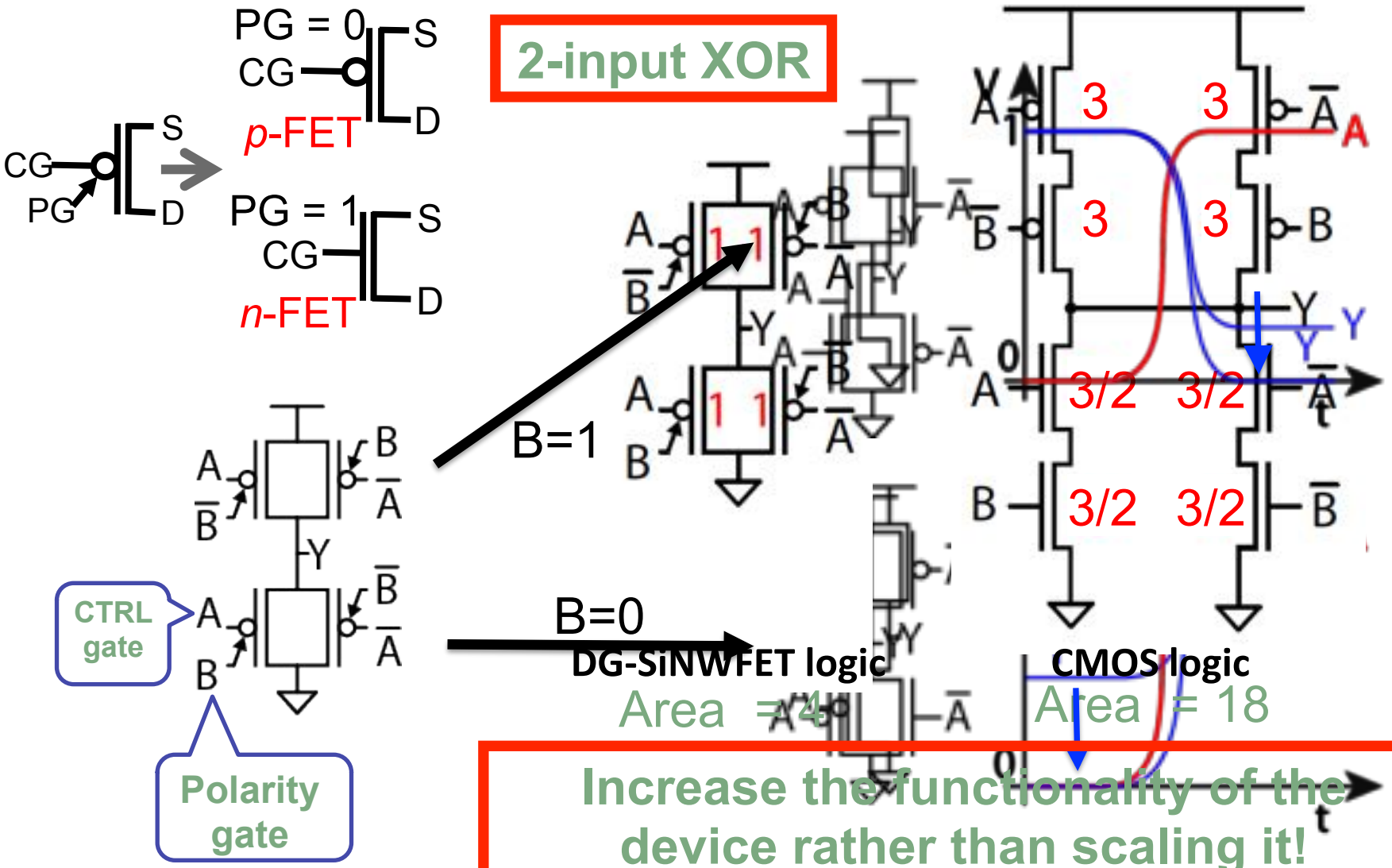


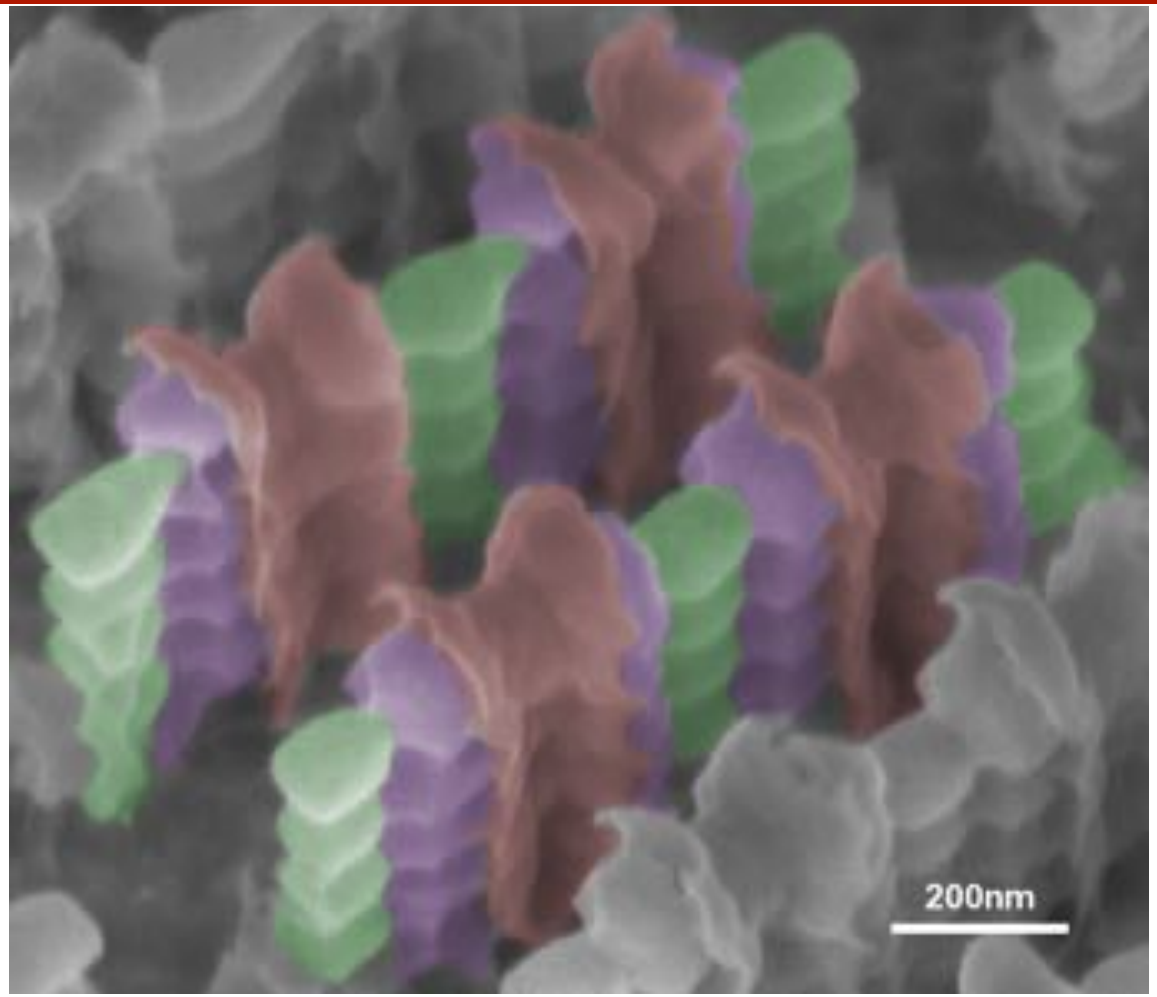


Same I_{ON} → Limited performance compromise

J. Zhang *et al*, *TED'14*

More Expressive Device Switching Functions

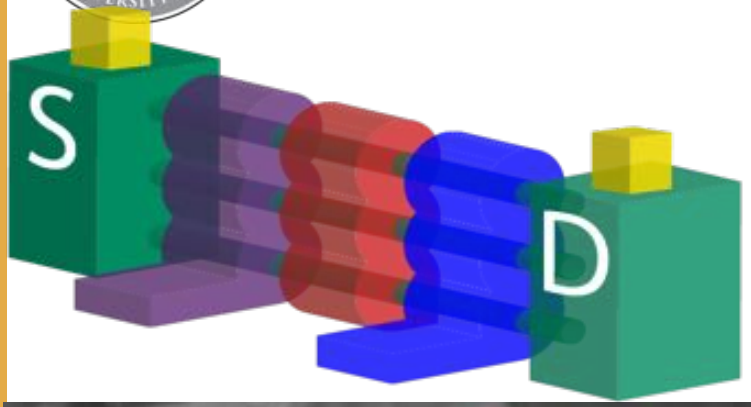


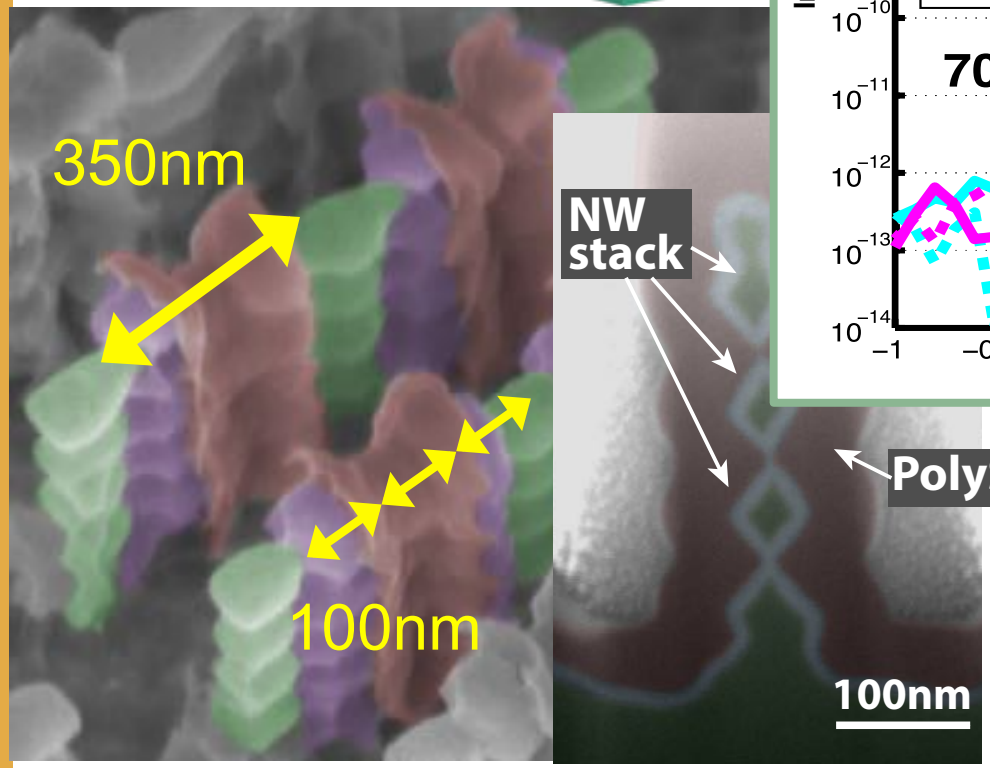


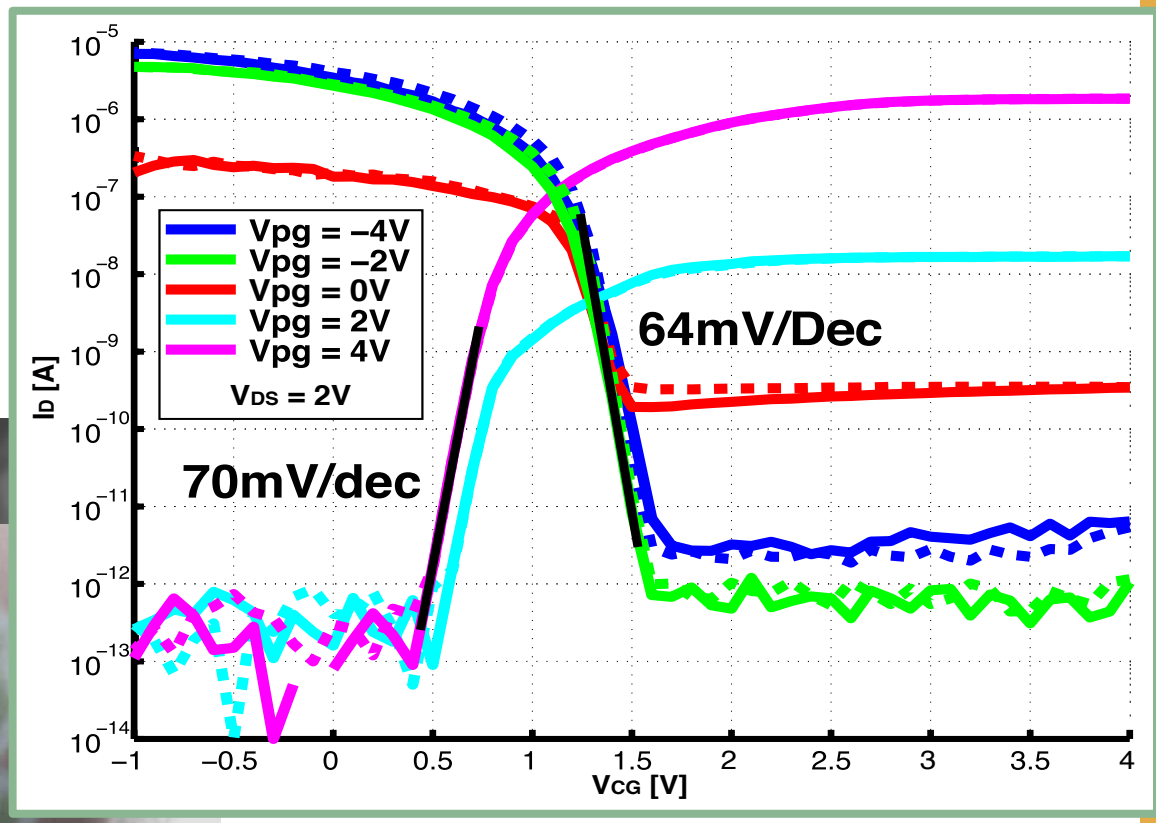
These are not “Castles in the Air” !

M. De Marchi *et al*, *IEDM’12*

Fabricated Device Overview







$I_{ON}/I_{OFF} > 10^6$ S~64mV/Dec

I_{OFF} in the range of 100 fA

Ultra Low Standby Power Technology

M. De Marchi *et al*, *IEDM'12*

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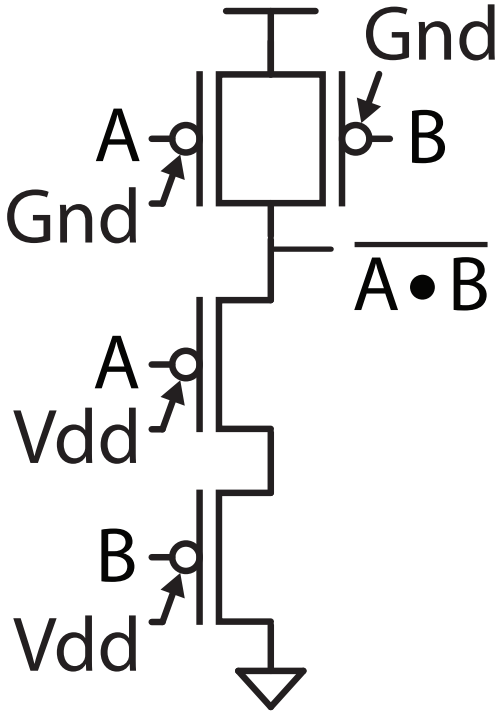
Circuit Design with Controllable-Polarity Transistors

Negative Unate functions

NAND, NOR, AOI, OAI,..

Bias the polarity gates!
(unipolar behavior)

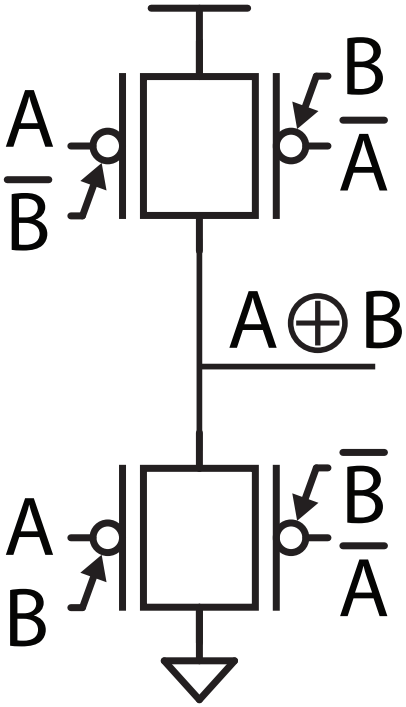


2-input NAND

Binate functions

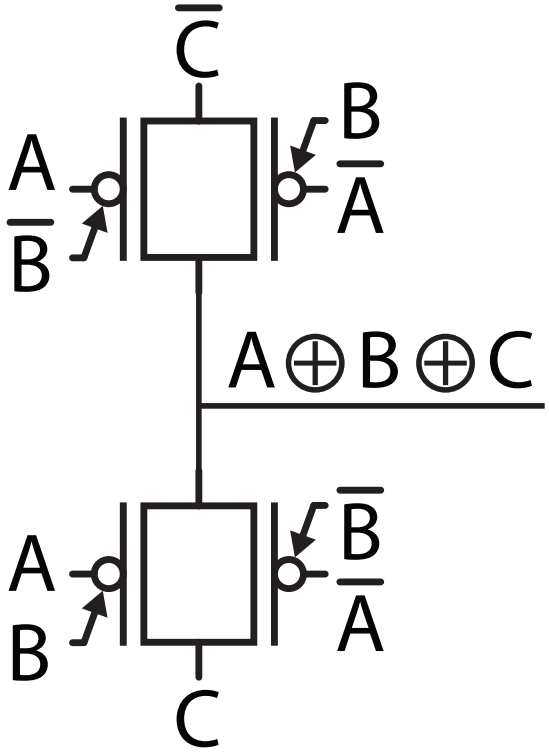
XOR, XNOR,..

Inputs to the polarity gates!
(Exploit the device behavior)



2-input XOR

H. Ben Jamaa *et al.*, *DATE'09*

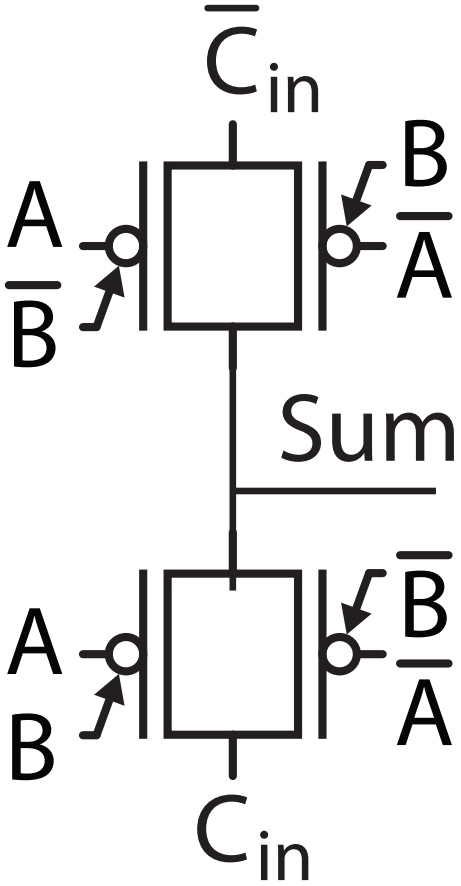


3-input XOR

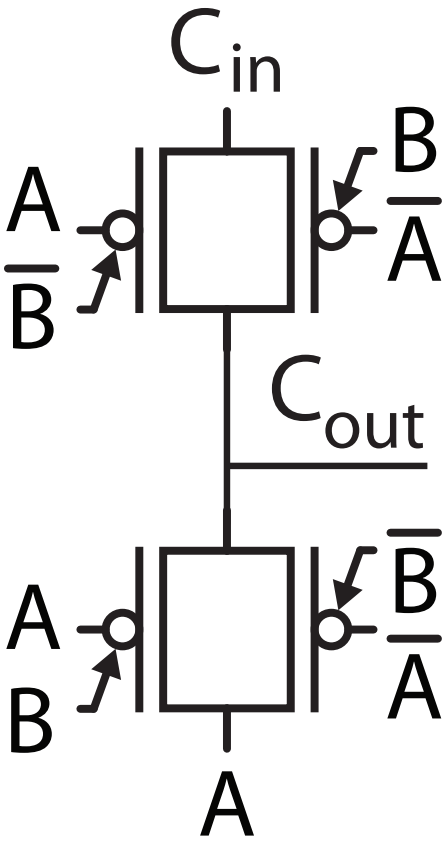
A. Zukovski *et al.*, *DAC'11*

Compact *Full-Adder* implementation

$$Sum = A \oplus B \oplus C_{IN} \qquad C_{OUT} = MAJ(A, B, C_{IN})$$



SUM



CARRY

8 Transistors

Area saving

(smaller gates)

Delay saving

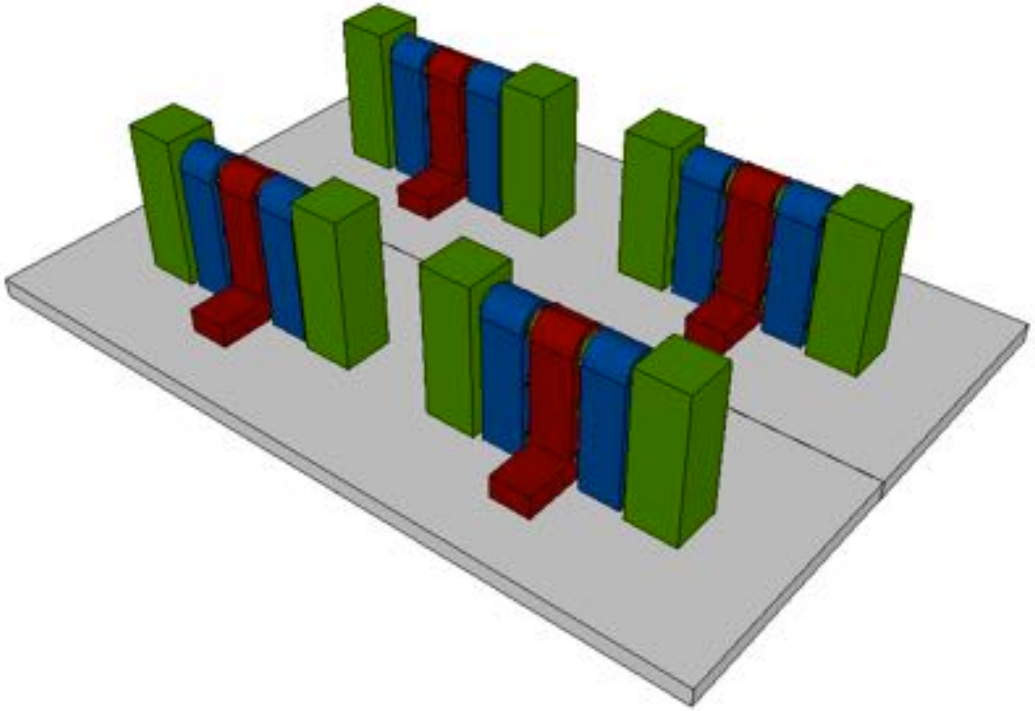
(smaller stacks)

Compact computation primitives

XOR - MAJ

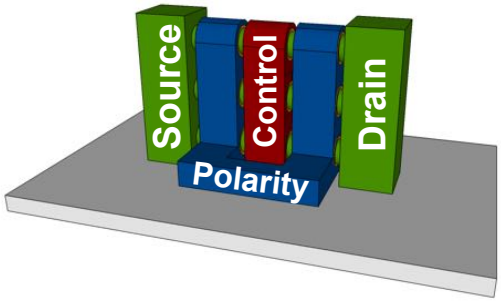
O. Turkyilmaz *et al.*, *ISCAS'13*

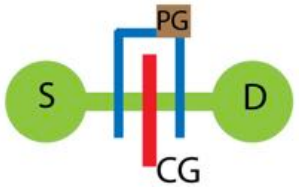
Mitigating the wiring complexity



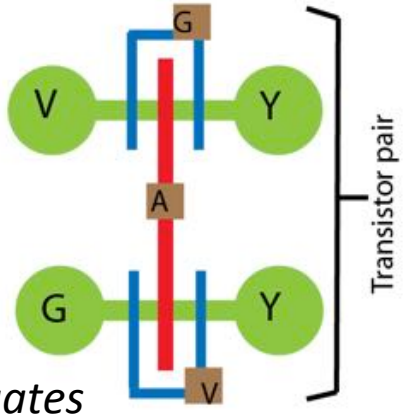
- Fewer transistors for XOR operation
- Every transistor has two gate terminals to route

Layout regularity with *Tiles*

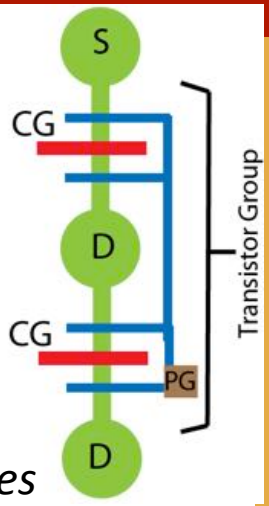




Dumbbell-stick

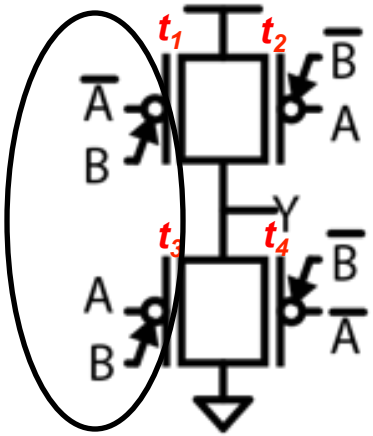


Control gates connected together

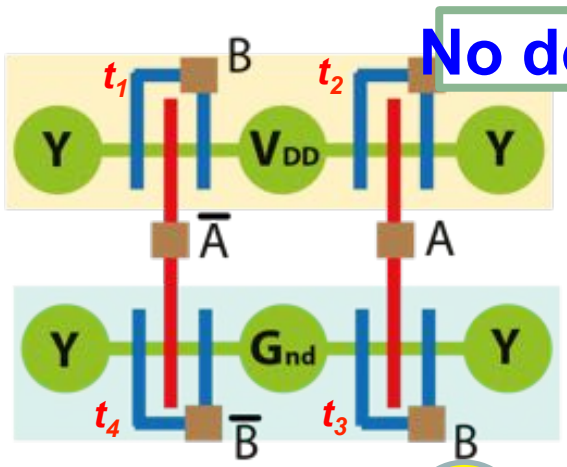


Polarity gates connected together

2-input XOR gate



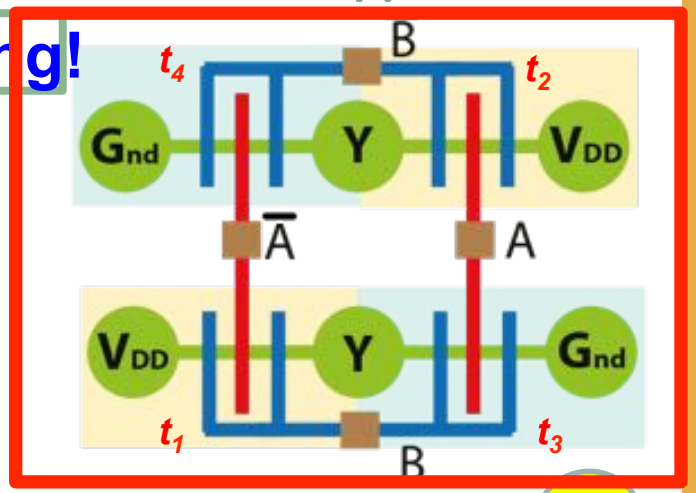
CMOS style layout



Complex routing

No doping!

Novel approach

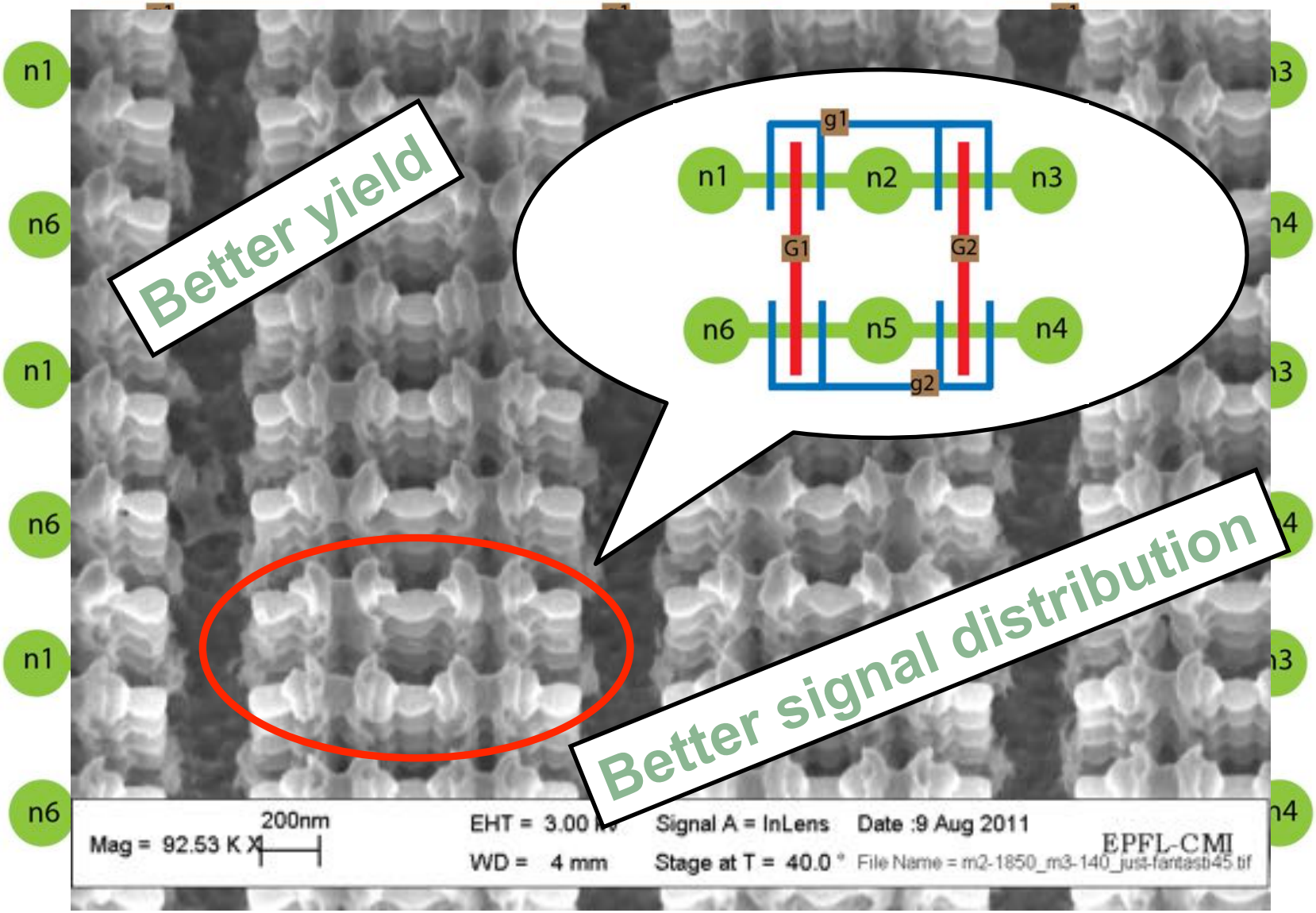


TILE

Simplified routing

S. Bobba *et al*, *DAC'12*

Sea-of-Tiles (SoT)



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Logic Synthesis (Optimization) Challenges

- Logic Synthesis is a technology supporter
  - LS techniques derive from CMOS abilities -NAND/NOR/ MUX
  - Many real-life applications contains different type of functions intertwined (AND/OR, XOR) together
  - LS heuristics target only one type of function for pragmatic reasons
- Logic Synthesis as a design enabler

Path1: ***Model comparator primitives*** ***(rather than switches)***

BBDDs

L. Amarù et al., DATE'13, DATE'14

Path2: ***Exploit more generic data structures***

MIG

L. Amarù et al., DAC'13, DAC'14

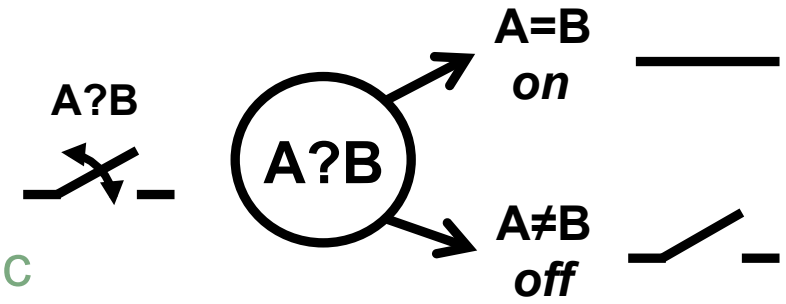
Can we derive novel architectures from these techniques?

Path1: Model the Comparator Primitive

Comparator primitive

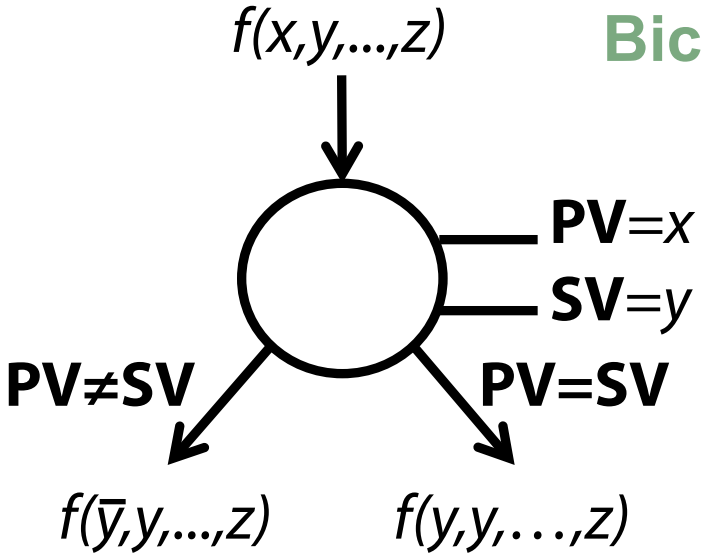
Arithmetic-intensive representation form

Ability to still model efficiently general logic



- Comparator behavior captured in the biconditional expansion:

$$f(x,y,..,z) = (x \oplus y) f(y',y,..,z) + (x \overline{\oplus} y) f(y,y,..,z)$$



Biconditional Binary Decision Diagrams

- Each BBDD node:
  - Has 2 branching variables
  - Implements the biconditional expansion
  - Can reduce to Shannon's expansion

L. Amarù *et al.*, *DATE'13, DATE'14*

Elementary Properties of BBDDs

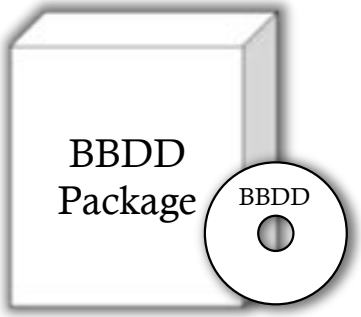
- BBDDs are canonical!
  - Reduction and Ordering rules extended from standard BDDs
  - Variable reordering and sifting operations still efficient

- BBDDs can support efficient logic manipulation
  - Traditional DD algorithms can be extended
  - BBDD software package available at: **http://lsi.epfl.ch**

- BBDDs are compact for arithmetic functions
  - *n*-bit adder: 40% nodes reduction

    BBDDs: $3n+1$ BDDs: $5n+2$
  - *n*-bit majority: 4× for large enough *n*

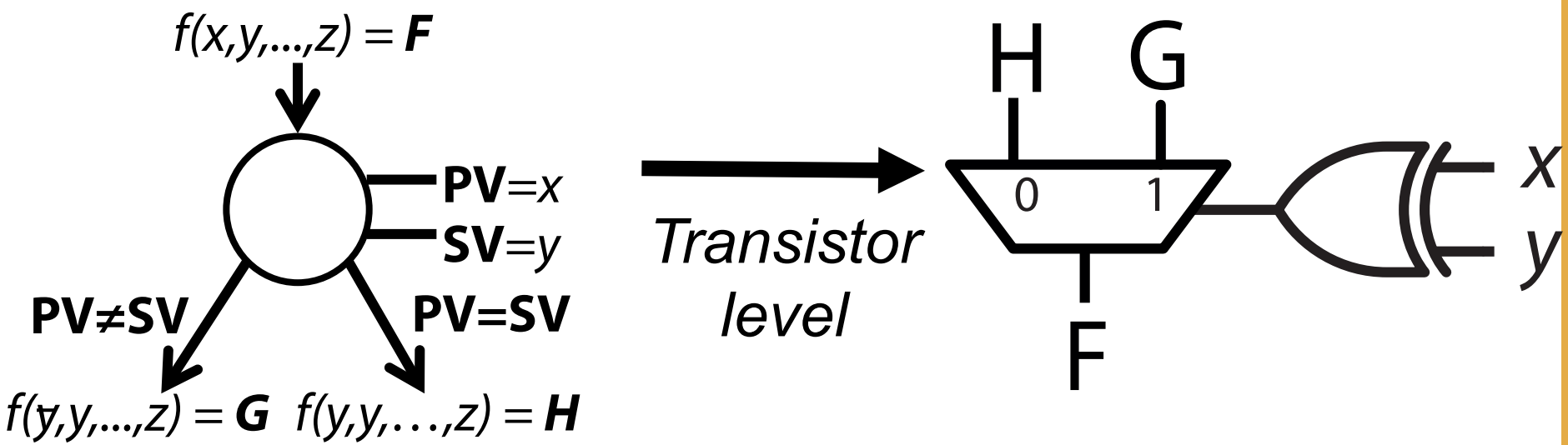
    BBDDs: $\frac{1}{8}n^2+\frac{1}{2}n+\frac{11}{8}$ BDDs: $\left\lceil\frac{n}{2}\right\rceil\left(n-\left\lceil\frac{n}{2}\right\rceil+1\right)+1$



L. Amarù *et al.*, *DATE'13, DATE'14*

BBDD superiority over standard BDDs in ASICs

- One-to-one correspondence between the BBDD nodes and XOR-MUX structure:



- DD performances (MCNC, opencores and hard arithmetic circuits):
  - BBDDs are frequently more compact than BDDs (**1.1× to 5×**)
  - BBDDs build faster than standard DDs (**1.4× to 4.4×**)
- EDA impact (Telecom circuit testcase)
  - BBDD restructuration reduces by **20% the critical path delay** as compared to a vanilla synthesis performed by Design Compiler

L. Amarù *et al.*, *DATE'13, DATE'14*

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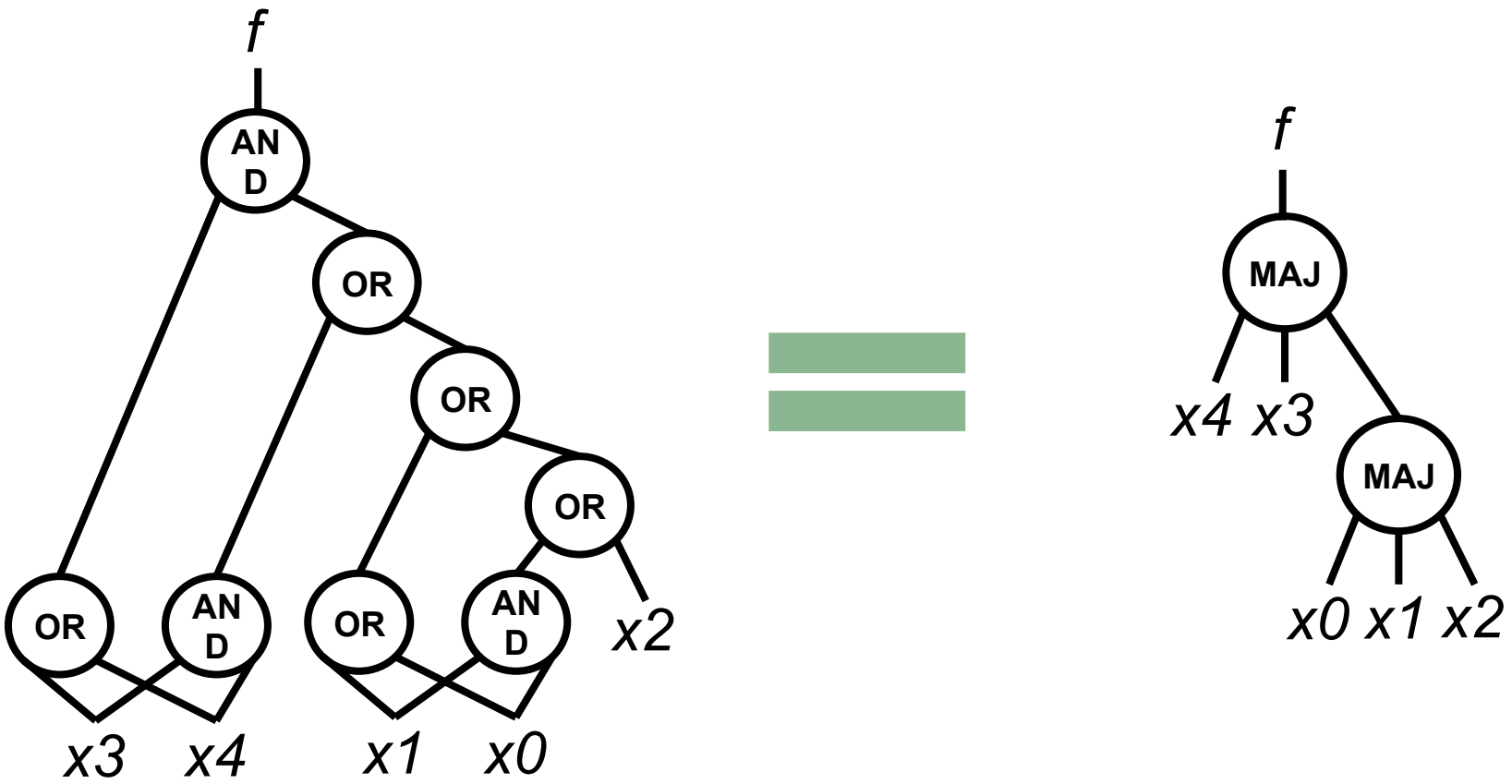
Path 2: Exploit more generic data structures

- Majority logic is a powerful generalization of AND/ORs.

Ex1: *MAJ(a,b,c)=ab+ac+bc* **Ex2:** *MAJ(a,b,1)=a+b* **Ex3:** *MAJ(a,b,0)=ab*

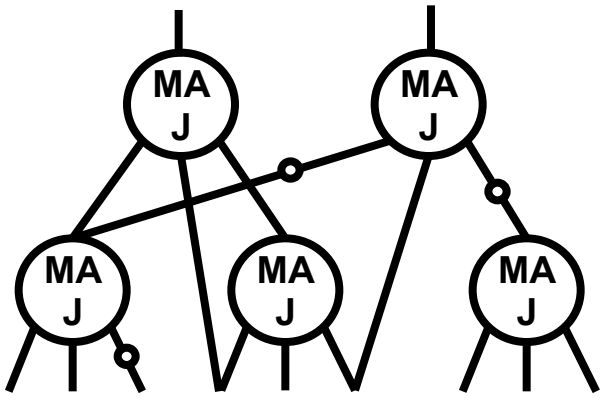
- Unlocks optimization opportunities not apparent before.



L. Amarù *et al.*, *DAC'14*

How to exploit MAJ logic?: Majority-Inverter Graph

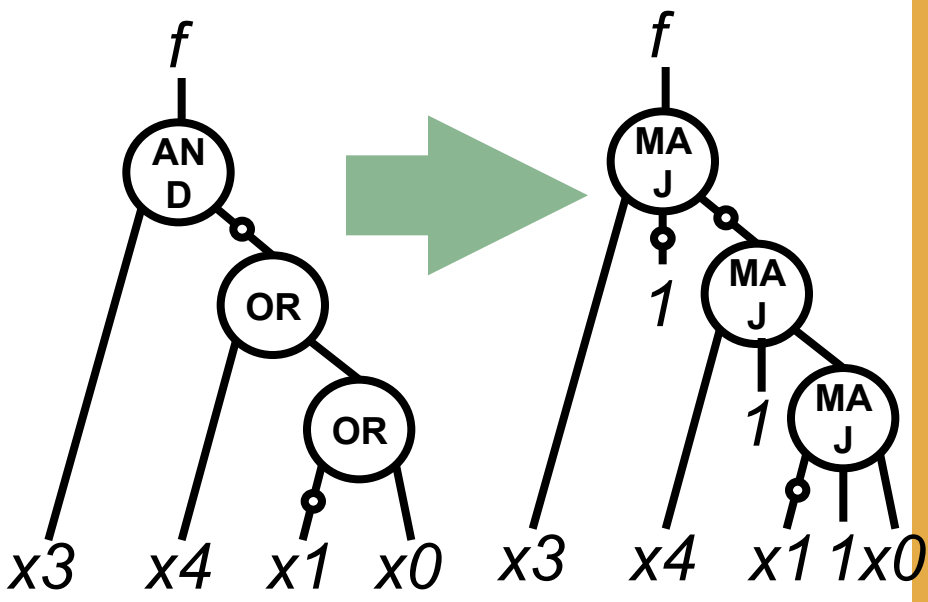
Definition: An MIG is a logic network consisting of 3-input majority nodes and regular/complemented edges.



From AOIG to MIG by direct transposition

Theorem: MIGs include AOIGs
MIGs include AIGs

MIGs are at least as compact as AOIGs
Exploiting the MAJ functionality unlock better representations



L. Amarù *et al.*, *DAC'14*

MIG Manipulation through an efficient Boolean Algebra

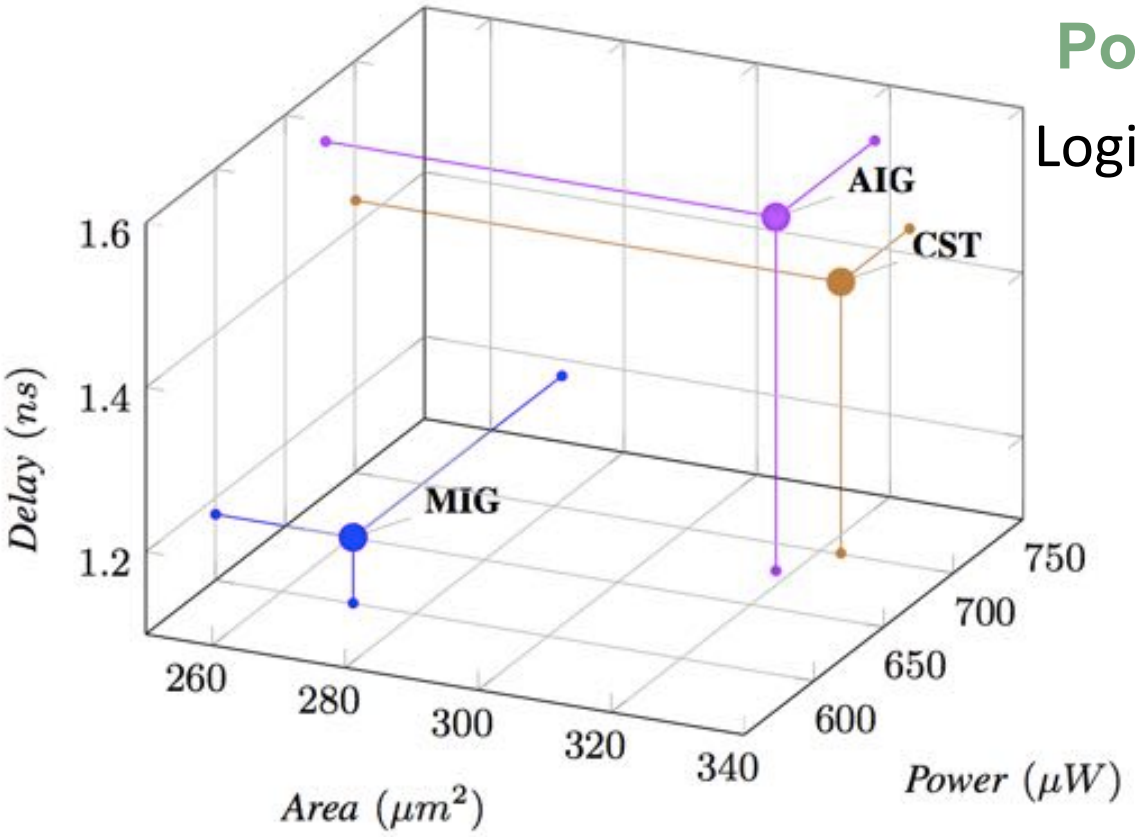
- MIG Axiomatic System Ω:
  - Commutativity: $M(x, y, z) = M(y, x, z) = M(z, y, x)$
  - Majority: $if(x = y),\ M(x, y, z) = x = y \quad if(x = y'),\ M(x, y, z) = z$
  - Associativity: $M(x, u, M(y, u, z)) = M(z, u, M(y, u, x))$
  - Distributivity: $M(x, y, M(u, v, z)) = M(M(x, y, u), M(x, y, v), z)$
  - Inverter Propagation: $M'(x, y, z) = M(x', y', z')$
- **Theorem:** (B,M,',0,1) subject to axiom in Ω is a Boolean algebra.
- **Theorem:** It is possible to transform any MIG α into any other logically equivalent MIG β, by a sequence of transformations in Ω.

In practice, it is always possible to reach a desired MIG, i.e., an **optimized** MIG, starting from an initial MIG.

Area = MIG size – Delay = MIG depth – Power = MIG SWactivity

L. Amarù *et al.*, *DAC'14*

Superiority of MIG w.r.t. Standard Techniques



Cells = {MIN, XOR, XNOR, NAND, NOR, INV}

Post Tech. Mapping (ASIC)

Logic Synthesis results in 22-nm **CMOS** – MCNC suite

-(22%, 14%, 11%) delay, area, power

w.r.t. AOIG-based synthesis

Post P&R

-(15%, 5%, 2%) delay, area, power

w.r.t. commercial flow

Novel LS techniques promising to push design efficiency!
Let's go to FPGAs and see how to exploit them (focus on BBDDs)!

L. Amarù *et al.*, *DAC'14*

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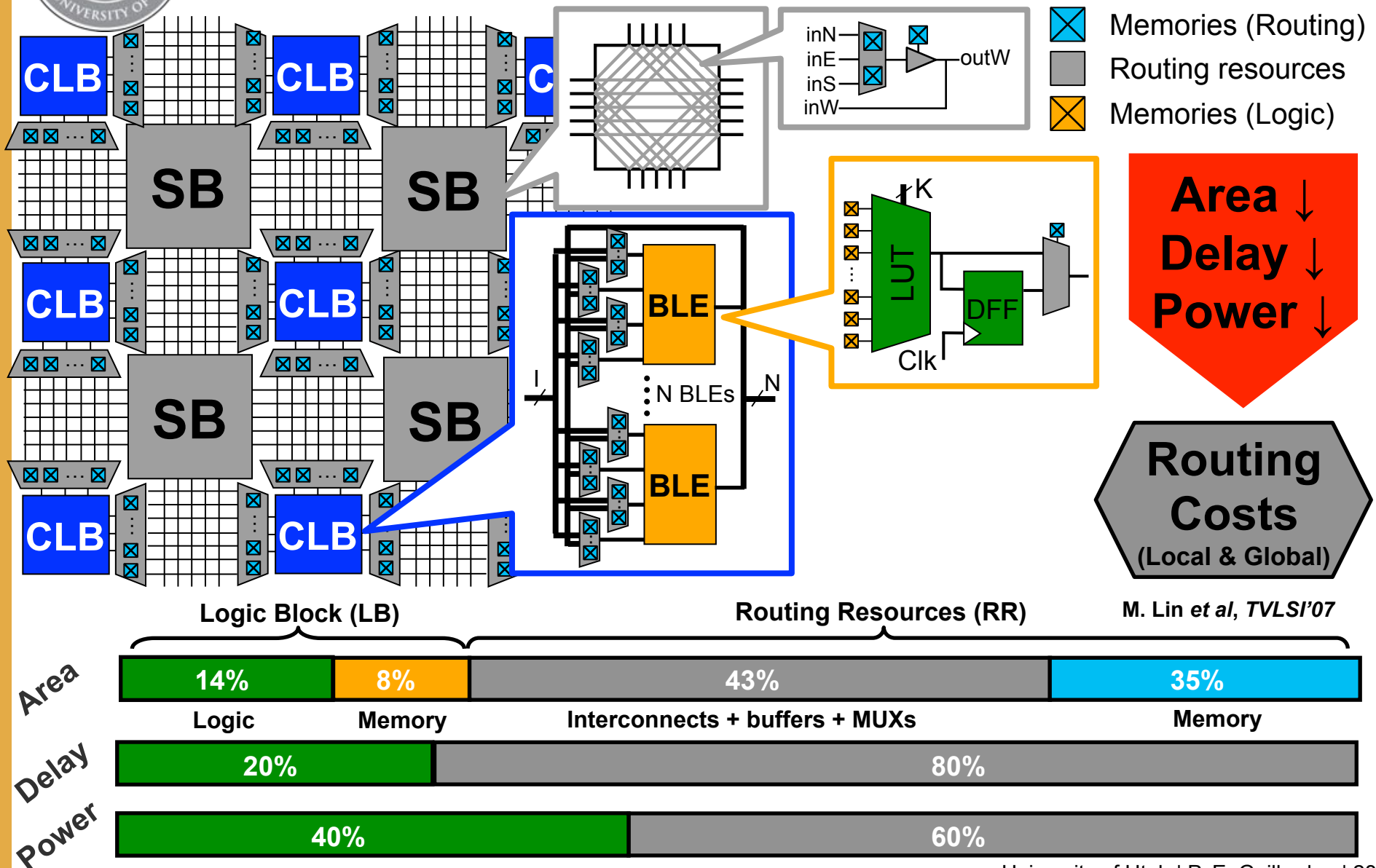
FPGAs: Where to play?

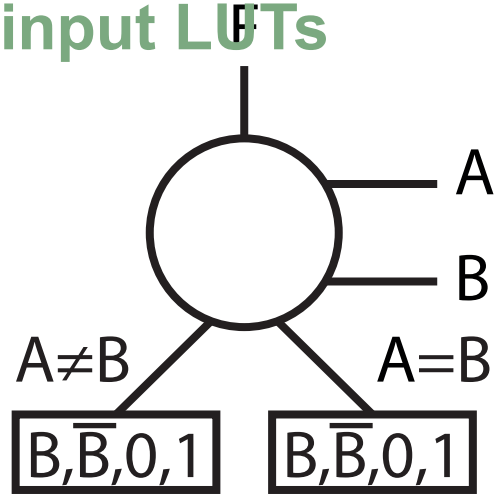


M. Lin *et al*, *TVLSI'07*

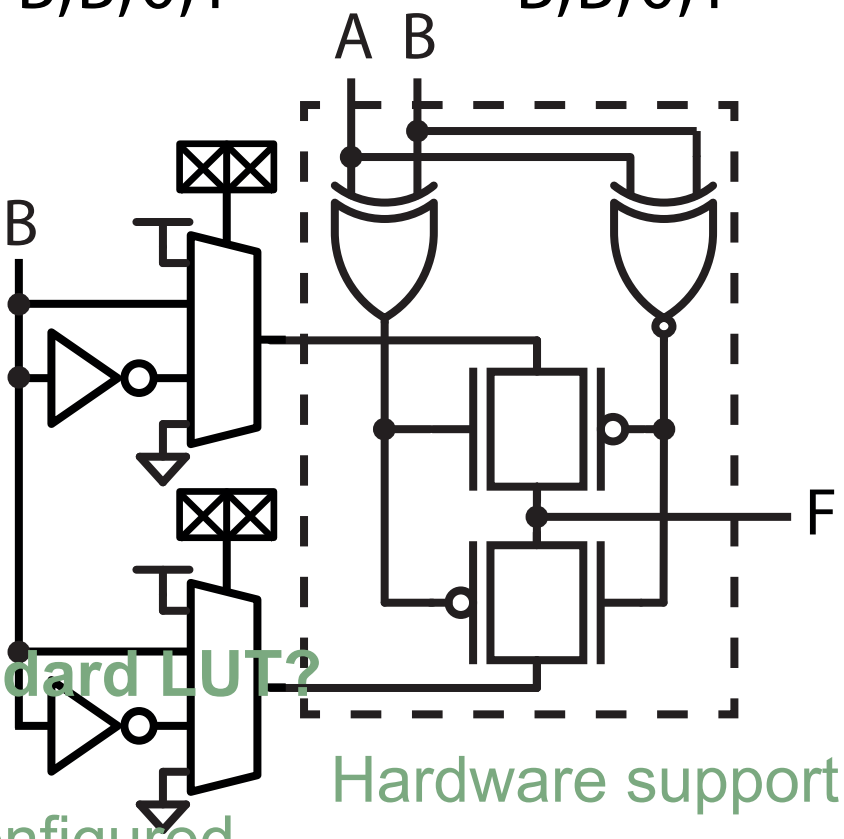
Exploiting the biconditional expansion in LUTs

Let's consider 2-input LUTs

$$f(A,B) = A \oplus B \,.\, \underbrace{f(\bar{B},B)}_{B,\bar{B},0,1} + \overline{A \oplus B} \,.\, \underbrace{f(B,B)}_{B,\bar{B},0,1}$$



BBDD representation



Hardware support

What is the advantage w.r.t. a standard LUT?

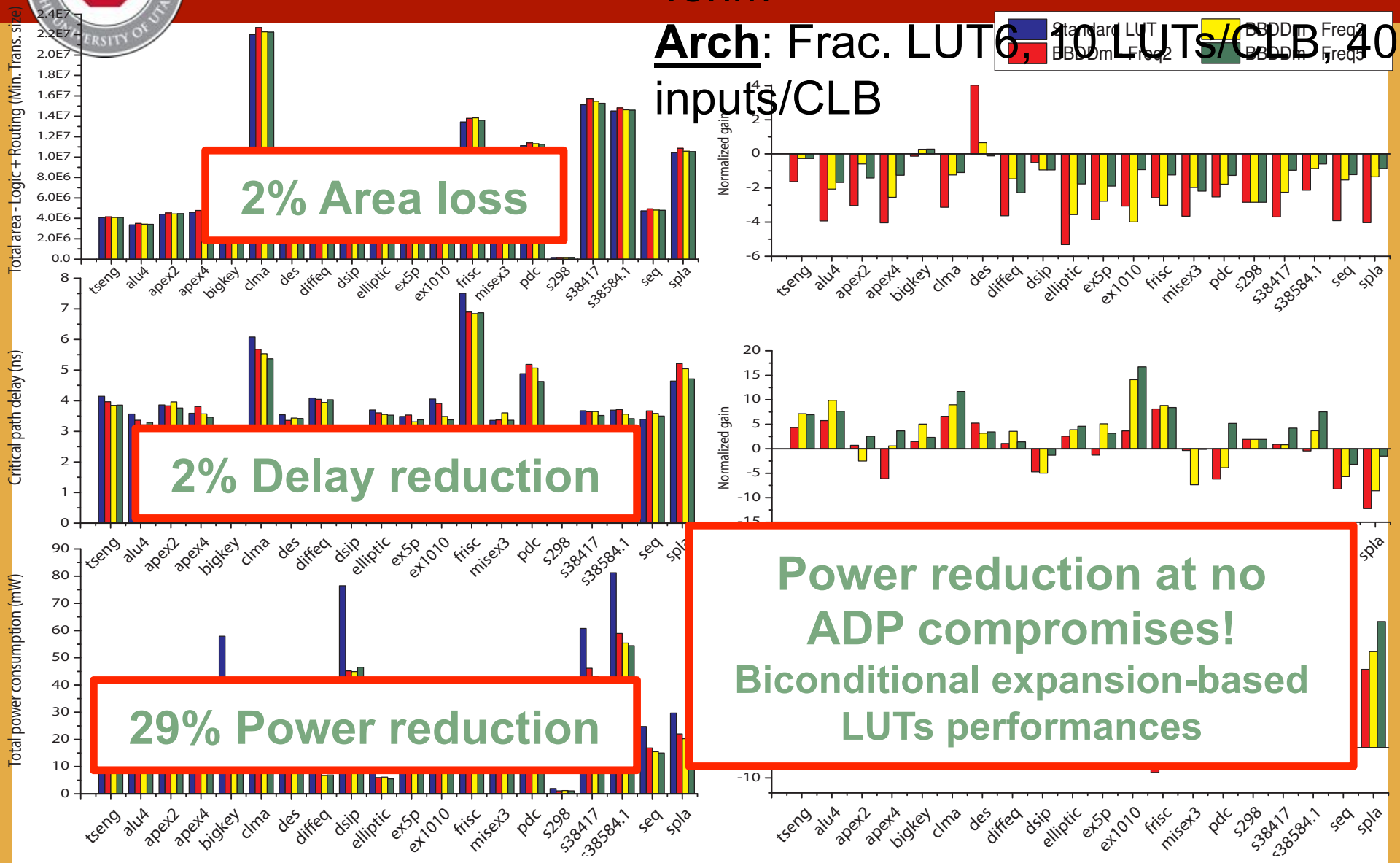
Strong power advantage

- 1st level of MUXes are statically configured
- 2nd level of MUXes activity is reduced thanks to the XORs
- MUX tree is not driven by SRAMs → Buffering requirements redu

MCNC big20 Suite

Tools: VTR7.0 flow – Perf. post layo
45nm

Arch: Frac. LUT6, 10 LUTs/CLB, 40
inputs/CLB



2% Area loss

2% Delay reduction

29% Power reduction

Power reduction at no ADP compromises!
Biconditional expansion-based LUTs performances

P.-E. Gaillardon *et al.*, *FPGA'14, FPGA'15*

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- Functionality-enhanced Devices
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- Emerging *Electronic Design Automation* techniques
  - Biconditional Binary Decision Diagrams (BBDDs)
  - Majority Inverter Graphs (MIGs)
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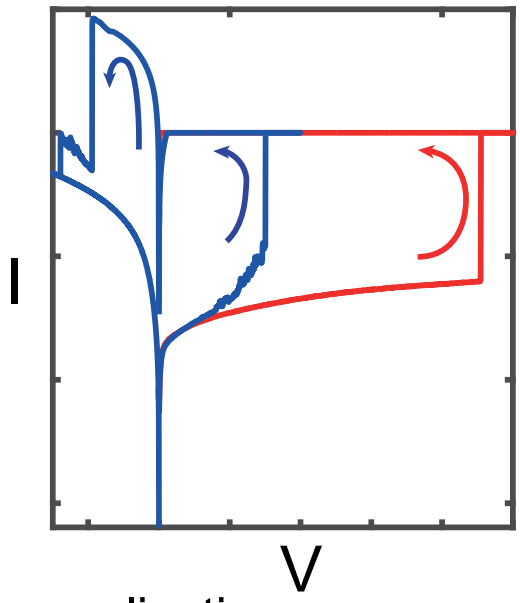
  - **RRAM: A low-power system enabler**
  - RRAM-based FPGA design
- Conclusion

RRAM: A Low-Power System Enabler

- MIM structures
  - Different switching mechanisms
  - Different physical origins
- Back-End-of-Line integration process
- Interesting device properties
  - Non-volatile storage (1-bit or multi-bit)
  - The properties can be engineered according to the application (Thresholds, resistance levels, aging, data retention, …)
  - Radiation tolerant



Low-Power Logic-in-memory Applications

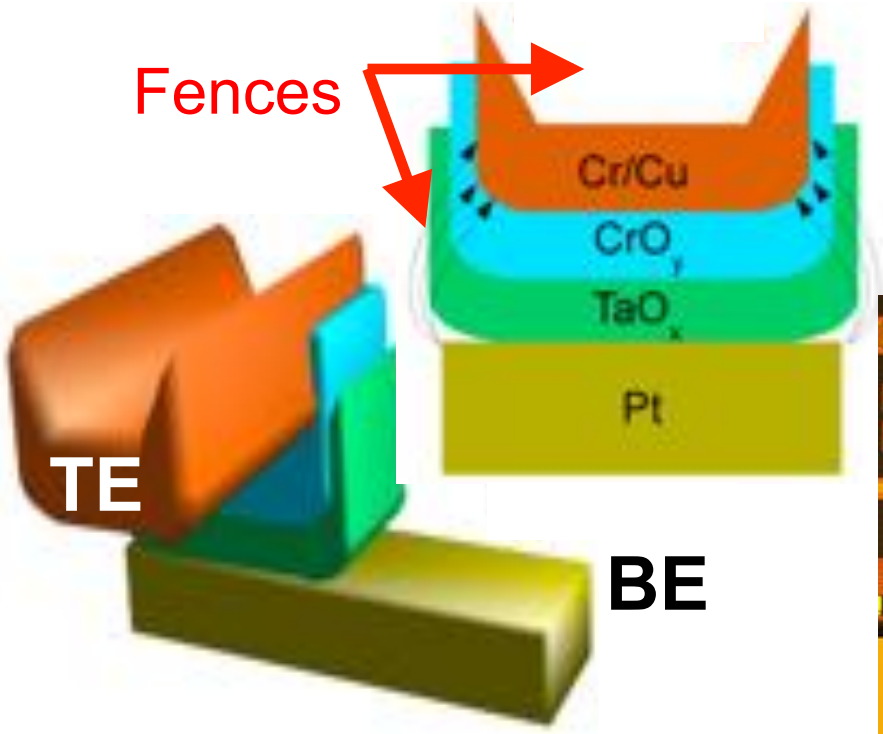
Can we find an unconventional killer application that goes beyond the simple notion of storage?

Merge them with the data path of reconfigurable logic to achieve 5× ⬇power and 1.5× ⬇ ADP

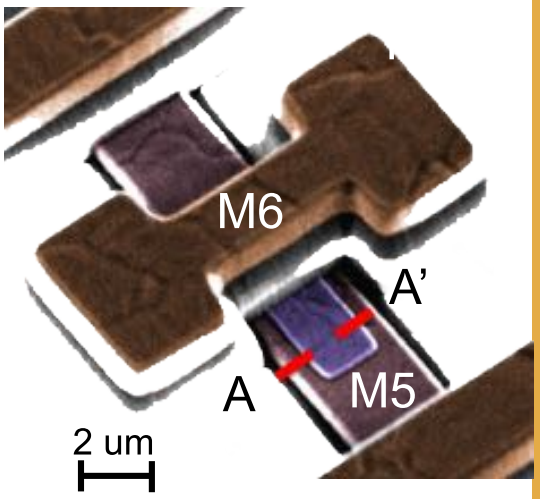
RRAM Technological Developments

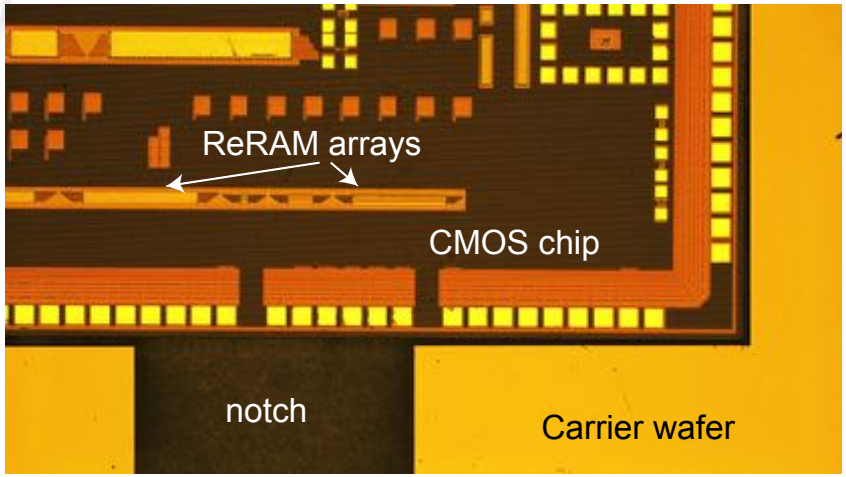
Controlling the technology and its CMOS co-integration opens a path towards innovative low-power circuits and systems

- Material Innovations: *Pt/TaOx/CrOy/Cr/Cu, Pt/Ti/HfO_2/Pt*
- Structural Innovations: Fences (better scalability)
- CMOS-RRAM co-integration



D. Sacchetto *et al.*, *CASM'13*





J. Sandrini *et al.*, *MNE'14, JME'15, JETCAS'15*

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FPGA Non-Volatile Routing Multiplexer

FPGAs rely on Routing Multiplexers

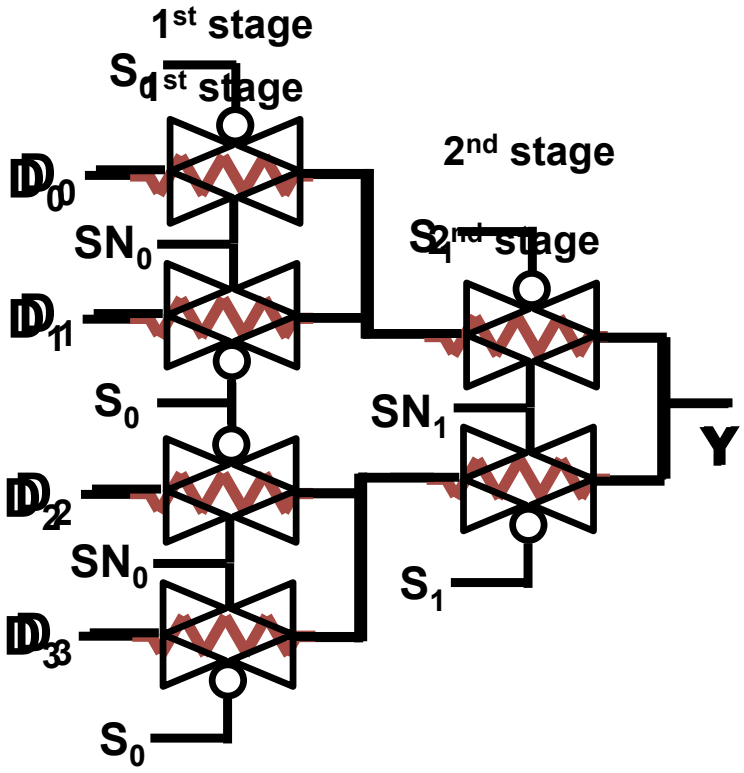
Multi-stage Multiplexers are based on transmission-gates

RRAM elements = Non-Volatile Switches

Replacement of all the Transmission-Gates

Non-Volatile Routing MUX

Performance improvement



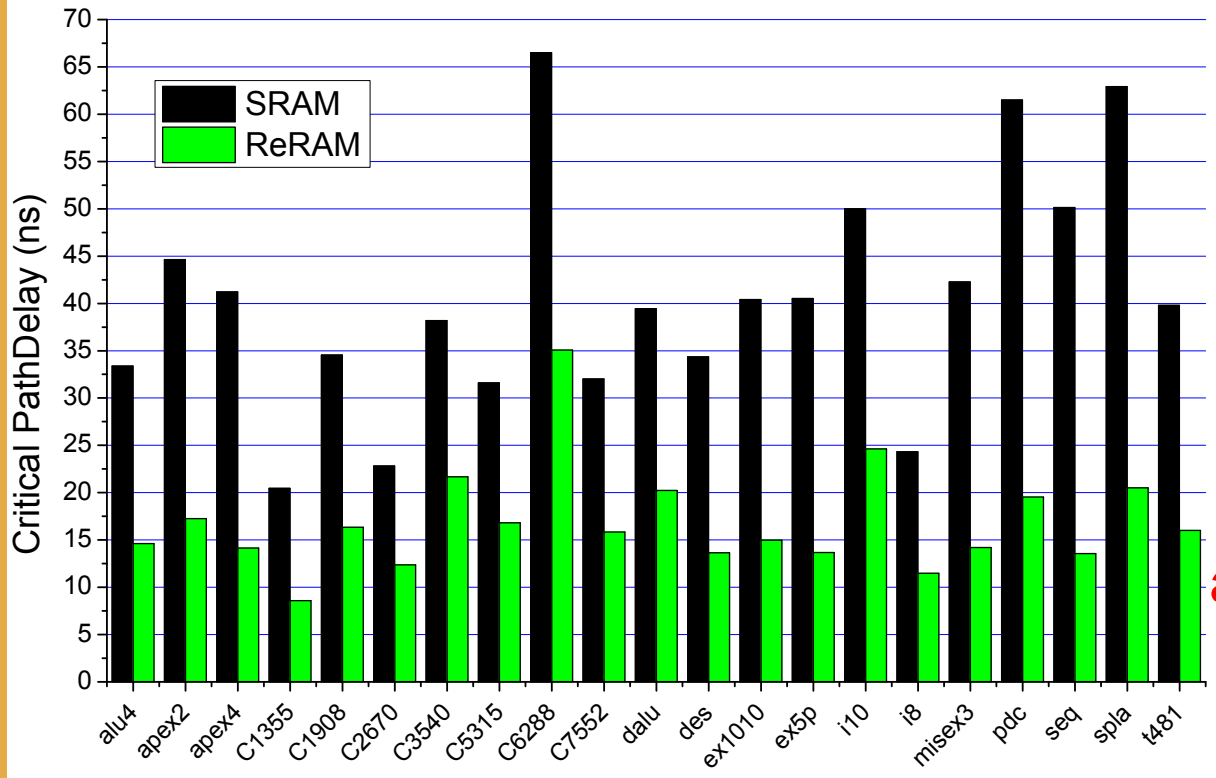
P.-E. Gaillardon *et al*, *VLSI-SoC'12*

Towards Faster FPGAs?

Low-on Resistance Routing Structures

Faster FPGAs
Nominal Vdd

- Area reduction up to 8%: Slight reduction – programming circuits
- Delay reduction up to 73%: Low On-resistance in data paths



Toolflow
VTR Toolflow
40-nm tech. node
MCNC Benchmarks

Room for architectural innovations

P.-E. Gaillardon *et al*, *VLSI-SoC'12*

Towards Low-Power FPGAs?

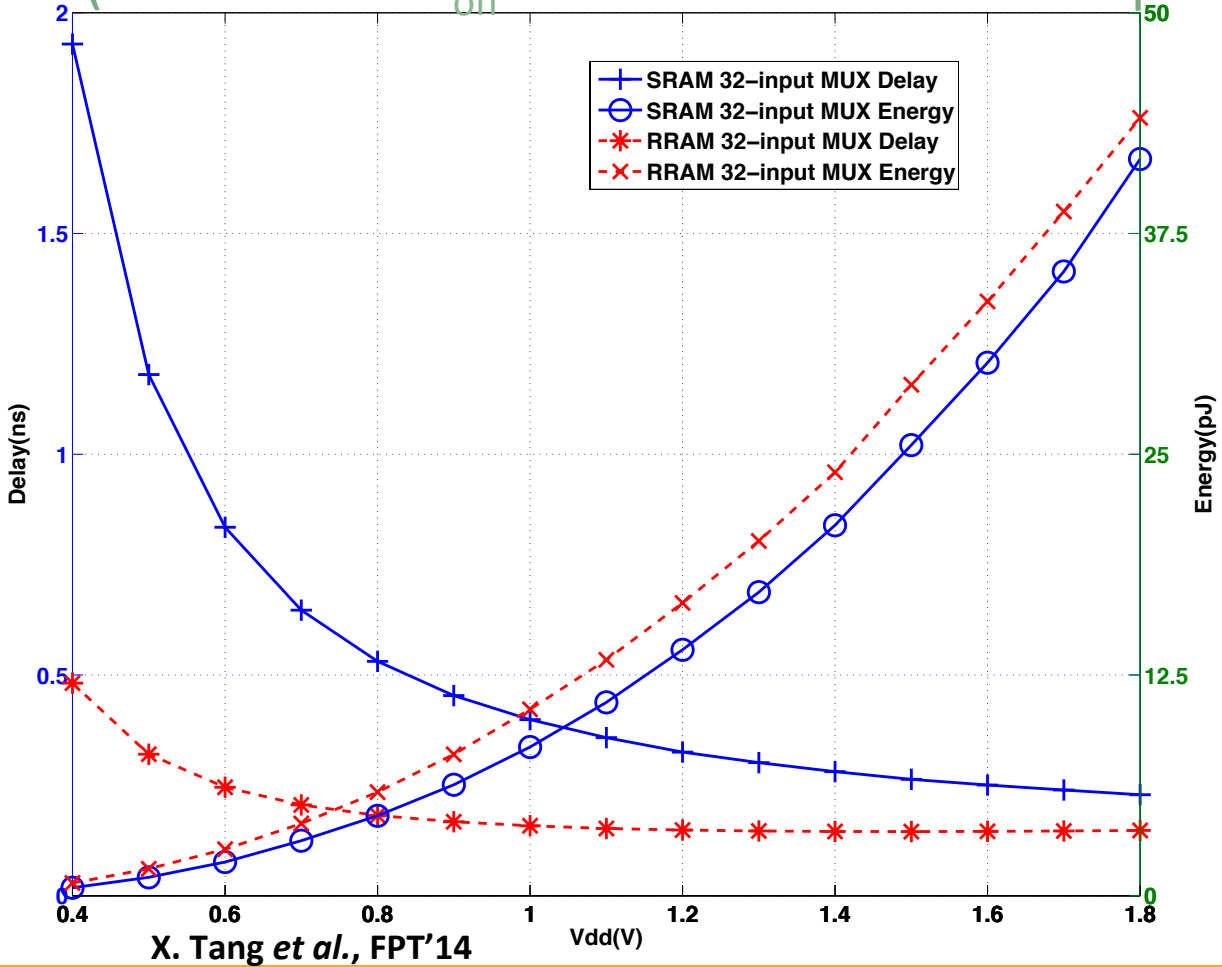
High-Performance Low-Power Routing Structures

Ultra-low Power FPGAs

Near-V_T power supply

In CMOS, V_{dd} reduction leads to low energy consumption but large delay

(reduction of I_{on} current and increase of parasitic capacitances)



X. Tang *et al.*, FPT'14

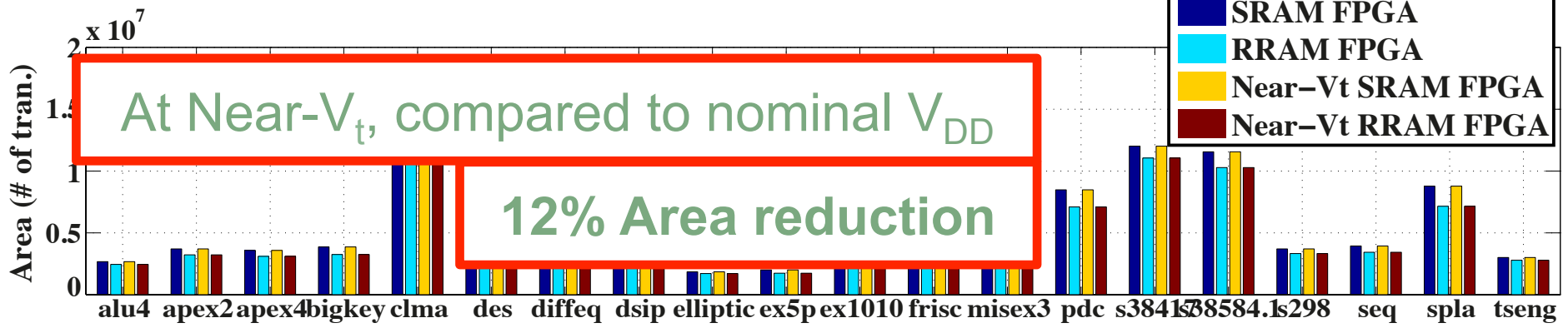
In ReRAM MUX, pass-gates are replaced by RRAMs

No R_{on} degradation

Limited delay degradation but similar energy gains

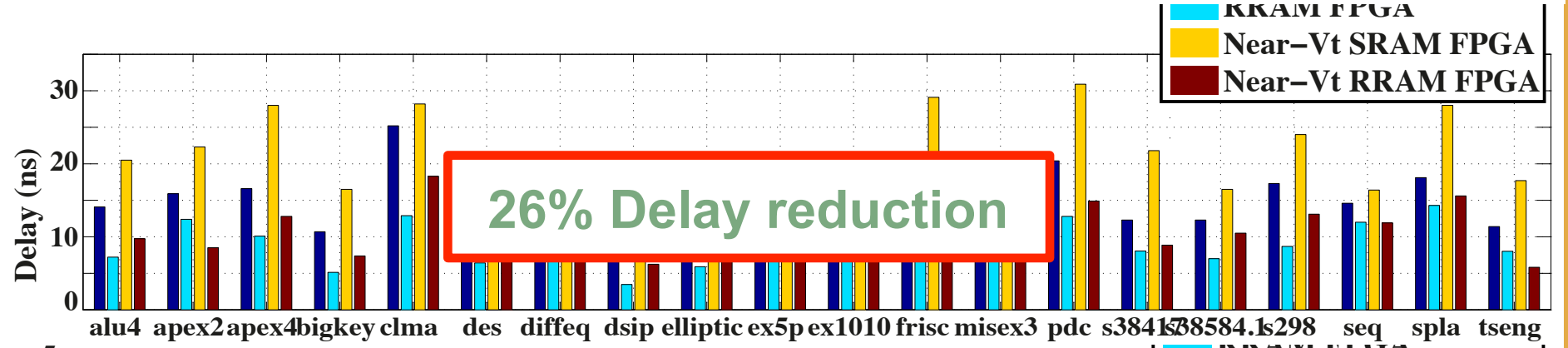
RRAM-based MUX can operate at low voltage without delay degradation

RRAM-based FPGA Architectural Exploration

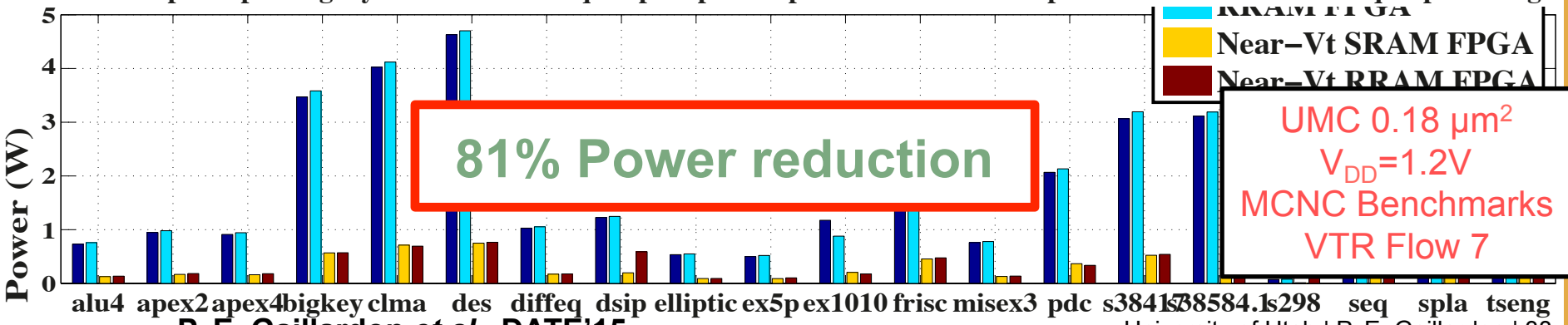


At Near-V_t, compared to nominal V_{DD}

12% Area reduction



26% Delay reduction



81% Power reduction

UMC 0.18 µm²
V_{DD}=1.2V
MCNC Benchmarks
VTR Flow 7

P.-E. Gaillardon *et al.*, DATE'15

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Take-away Messages

- Better devices do not mean smaller devices
  - ❖ Exploit the functionality rather than the density
  - ❖ Trigger many innovations at the circuit level (arithmetic, routing, …)
- Novel EDA techniques are promising sources of inspiration
  - ❖ Biconditional expansion shows great quality
  - ❖ Majority logic even more promising!
- The architecture/application should lead the game

Acknowledgments




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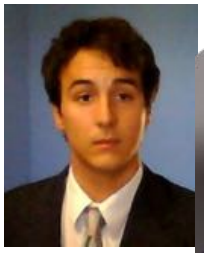
Mr. Gain Kim

Architecture Design

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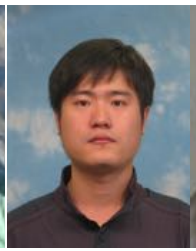
Mr. Jury Sandrini

Thank you for your attention

Questions?

Integrated Nanosystems Research Group
Department of Electrical and Computer Engineering
MEB building – University of Utah – Salt Lake City – UT – USA