Job Notification Form, IIT Delhi

Company Overview

Name: Tejas Networks Ltd

Website: www.tejasnetworks.com

Company Type:

Core (Technical)

Description:

Tejas Networks, an India-based optical and data networking products company, designs and develops market leading products in the Optical Networking and Broadband Access (4G/LTE, GPON) segments. Having a strong focus on R&D and IPR creation, Tejas has filed 330+ patents in USA, Europe and India. It is ranked #1 in India's Optical Aggregation Market and stands among top ten players globally. With a customer footprint in over 75+ countries, it has shipped 500,000+ systems across the globe. It serves telecommunications service providers, internet service providers, utilities, defense and government entities with its costcompetitive and high-performance products globally.

Job Details

Designation: Engineer, R&D

Type: Core (Technical)

Place

of Bangalore Gurgaon

Posting:

Job Details:

JOB DESCRIPTION - HARDWARE

About Tejas Networks:

Tejas Networks, an India-based optical and data networking products company, designs and develops market leading products in the Optical Networking and Broadband Access (4G/LTE, GPON) segments. Having a strong focus on R&D and IPR creation, Tejas has filed 349 patents in USA, Europe and India. It is ranked #1 in India's Optical Aggregation Market and stands among top ten players globally. With a customer footprint in over 75+ countries, it has shipped 500,000+ systems across the globe. It serves telecommunications service providers, internet service providers, utilities, defense and government entities with its costcompetitive and high-performance products globally.

Position: Engineer, R&D Location: Bangalore/Gurgaon

JD:

- B.E, BTech/M. E, MTech (E&C)
- · You need to have a thorough understanding of hardware concepts and be very comfortable with electronic circuits and how they operate.
- You need to be familiar with digital/analogue design concepts.
- Exposure to FPGA design is an advantage.
- You are a self-starter and have ability to think deeply. **Board Design**
- You will be a key member of the team developing high speed boards for telecom applications upto 100 Ghtz.
- You will work on the latest generation embedded processors, switches, optical components, FPGAs etc.

FPGA Design

You will be a key member of the design/development team of FPGA systems

mainly working on VHDL/Verilog for telecom applications.

JOB DESCRIPTION - SOFTWARE

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Position: Engineer, R&D Location: Bangalore/Gurgaon

- JD:
- B.E, BTech/M. E, MTech (E&C, Comp Science)
- You have a passion for coding & are great at problem-solving.
- You are proficient in either C/C++ or other scripting languages like Perl.
- You have a strong understanding of computing concepts including data structures, operating systems & Algorithms.
- Ideally you have been exposed to networking protocols like TCP/IP and have some exposure to embedded systems (Linux).
- You are a self-starter and have ability to think deeply.
 Roles:
- You will be a key member of the team developing next-generation telecom networking products.
- These products support GPON / TDM / OTN / Packet / Hybrid cross-connects ranging from gigabits to multi-terabits and high speed interfaces.
- You will work across the entire product life-cycle and your code will go into live products virtually from day 1.

Joining By: 1 August 2022

Salary Details

CTC: 100,000 INR Per Annum

Gross: 89,100 INR Per Annum

CTC 10 L for B.Tech: Fixed: 8.91 + Welfare Benefits: 0.26 + Retirals: 0.83

Breakup:

11L for M.Tech: Fixed: 9.33 + Variable Pay: 0.54 + Welfare Benefits: 0.26 +

Retirals: 0.87

Perks /

No

Bonus:

Selection Process

Resume Shortlist:

Yes

Written Test:

Online Test: Yes

Group

No

Discussion:

Medical Test: No

Personal

Yes

Interview:

No. of 2

Rounds:

No. of 4

Offers:

Minimum CGPA:

7.5 & above CGPA in all academics

Eligibility

Recruiting PHDs:

No

Eligible

B.Tech in Computer Science & Engineering, B.Tech and M.Tech in Computer Science & Engineering, M.Tech in Computer Science & Engineering

Departments: