Fibonacci Sequence till Term 15

Iteration 1

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 3

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 4

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 5

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 6

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 7

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 8

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 9

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 10

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 11

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 12

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 13

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 14

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								

Iteration 15

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Status Register	I	T	H	S	V	N	Z	C
Alterations								
Reason for alterations								