EC-210

MICROPROCESSORS LAB

LAB-2

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Objective: To demonstrate the use of arithmetic instructions

Exercise:

2.1] Write an assembly program to take two 32 bit unsigned numbers in to the registers using MOV or MVN instructions and perform the following

(a) Add using ADD, ADDS, ADC

(b) Subtract using SUB, SUBS, SBC

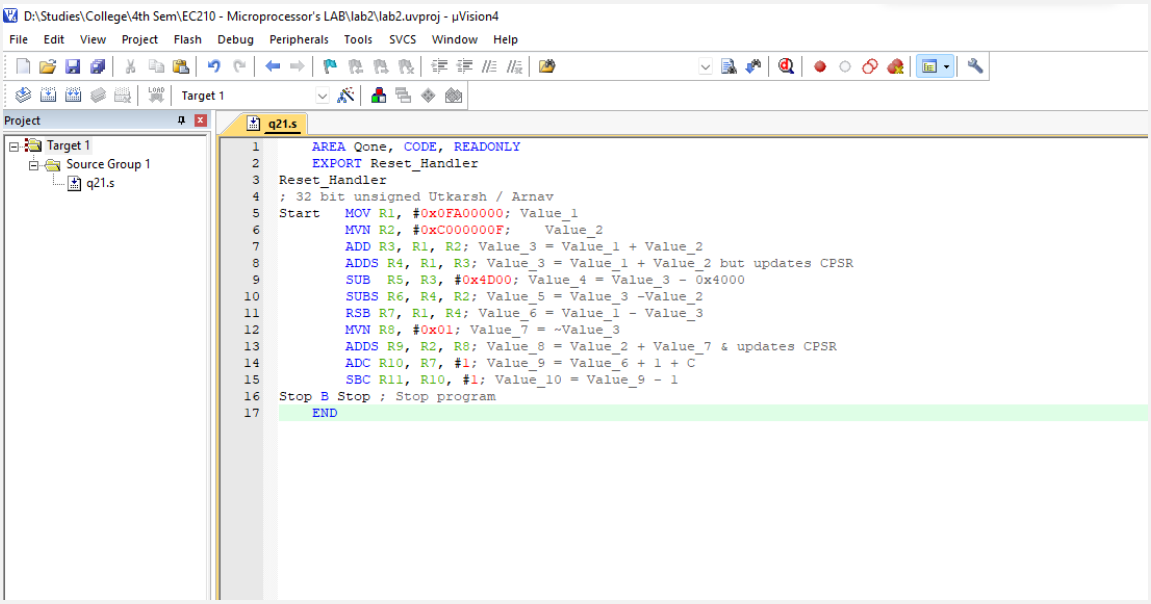
(c) Reverse subtract using RSB, RSC

-> using all of the above instructions in a single assembly file.

Source Code:

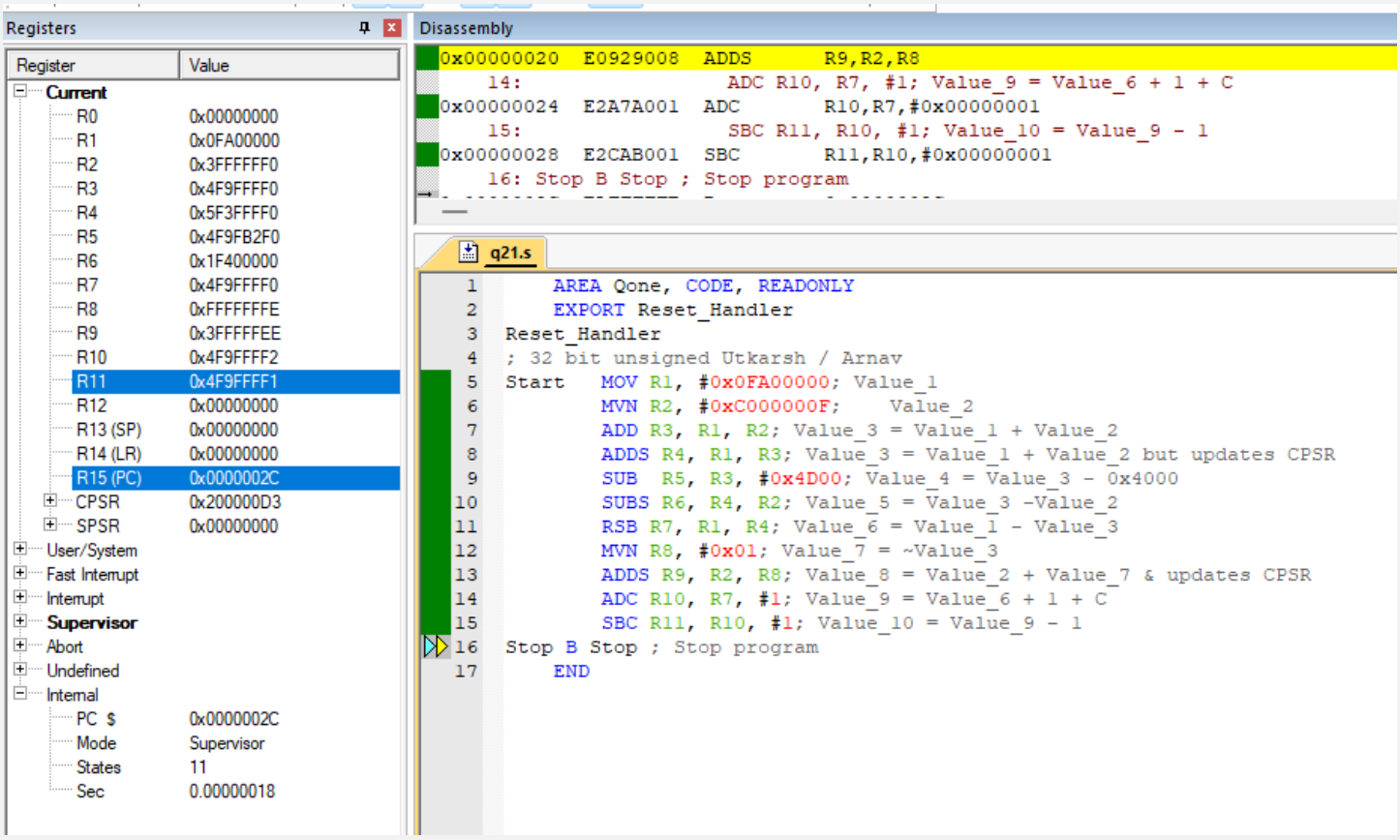
```
    AREA Qone, CODE, READONLY
    EXPORT Reset_Handler
Reset_Handler
; 32 bit unsigned Utkarsh / Arnav
Start   MOV R1, #0x0FA00000; Value_1
        MVN R2, #0xC000000F;    Value_2
        ADD R3, R1, R2; Value_3 = Value_1 + Value_2
        ADDS R4, R1, R3; Value_3 = Value_1 + Value_2 but updates CPSR
        SUB  R5, R3, #0x4D00; Value_4 = Value_3 - 0x4000
        SUBS R6, R4, R2; Value_5 = Value_3 -Value_2
        RSB R7, R1, R4; Value_6 = Value_1 - Value_3
        MVN R8, #0x01; Value_7 = ~Value_3
        ADDS R9, R2, R8; Value_8 = Value_2 + Value_7 & updates CPSR
        ADC R10, R7, #1; Value_9 = Value_6 + 1 + C
        SBC R11, R10, #1; Value_10 = Value_9 - 1
Stop B Stop ; Stop program
    END
```

Setup:



Debugging:

End Result:

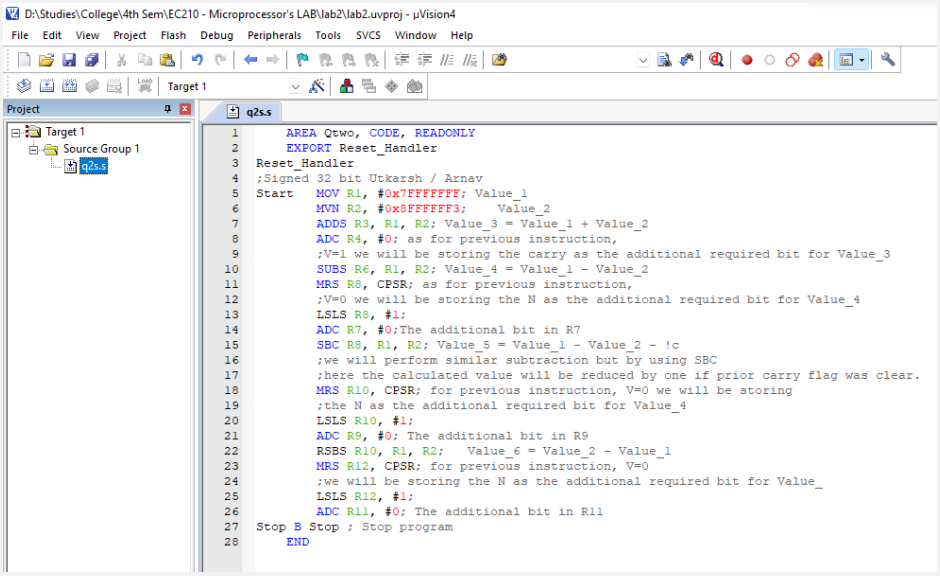


2.2 (a) Repeat ex 2.1 a,b,c for 32 bit signed numbers.

-> Source Code:

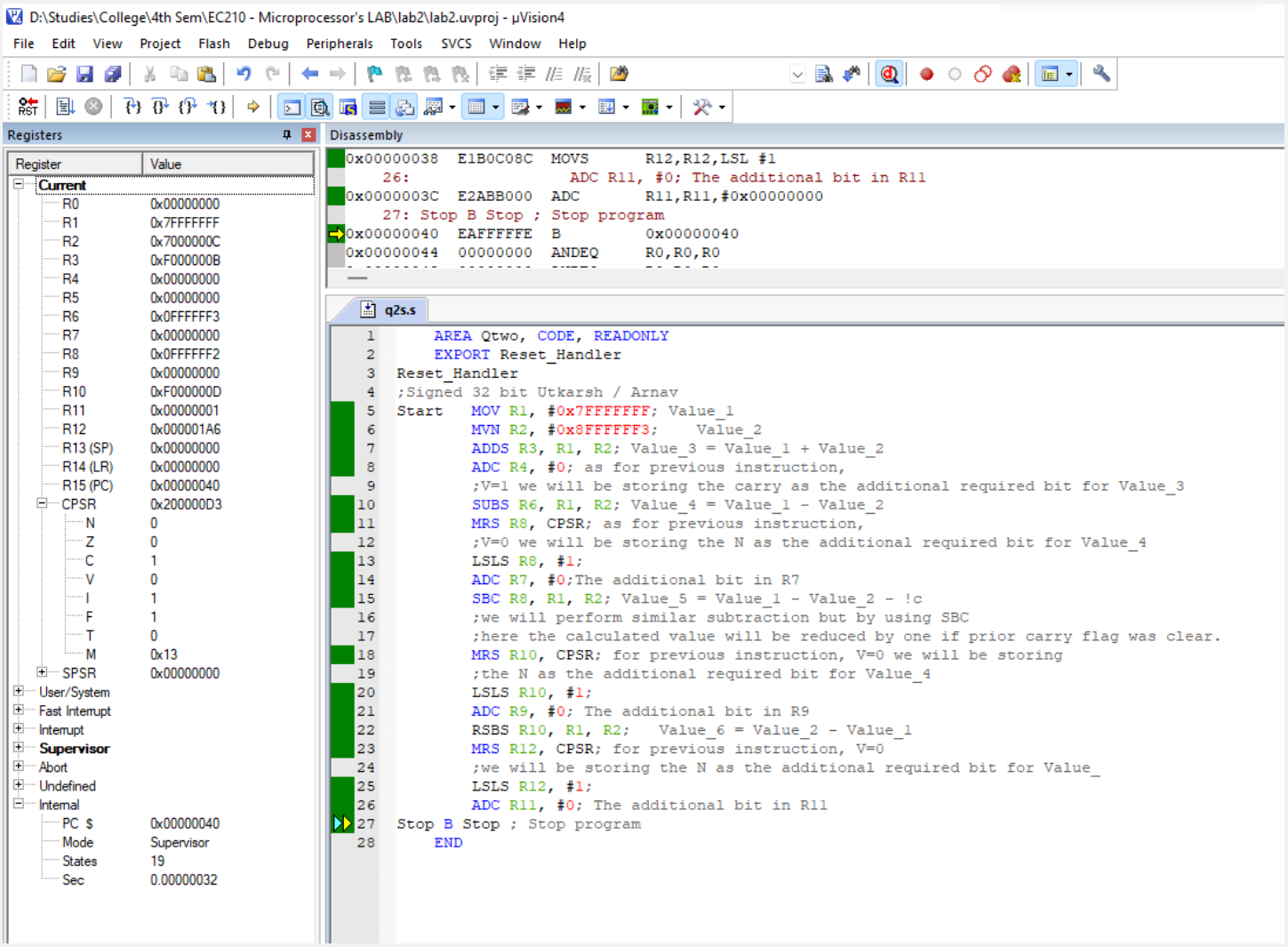
```
    AREA Qtwo, CODE, READONLY
    EXPORT Reset_Handler
Reset_Handler
;Signed 32 bit Utkarsh / Arnav
Start   MOV R1, #0x7FFFFFFF; Value_1
        MVN R2, #0x8FFFFFF3;    Value_2
        ADDS R3, R1, R2; Value_3 = Value_1 + Value_2
        ADC R4, #0; as for previous instruction,
        ;V=1 we will be storing the carry as the additional required bit for Value_3
        SUBS R6, R1, R2; Value_4 = Value_1 - Value_2
        MRS R8, CPSR; as for previous instruction,
        ;V=0 we will be storing the N as the additional required bit for Value_4
        LSLS R8, #1;
        ADC R7, #0;The additional bit in R7
        SBC R8, R1, R2; Value_5 = Value_1 - Value_2 - !c
        ;we will perform similar subtraction but by using SBC
        ;here the calculated value will be reduced by one if prior carry flag was clear.
        MRS R10, CPSR; for previous instruction, V=0 we will be storing
        ;the N as the additional required bit for Value_4
        LSLS R10, #1;
        ADC R9, #0; The additional bit in R9
        RSBS R10, R1, R2;   Value_6 = Value_2 - Value_1
        MRS R12, CPSR; for previous instruction, V=0
        ;we will be storing the N as the additional required bit for Value_
        LSLS R12, #1;
        ADC R11, #0; The additional bit in R11
Stop B Stop ; Stop program
    END
```

Setup:



Debugging:

End Result:

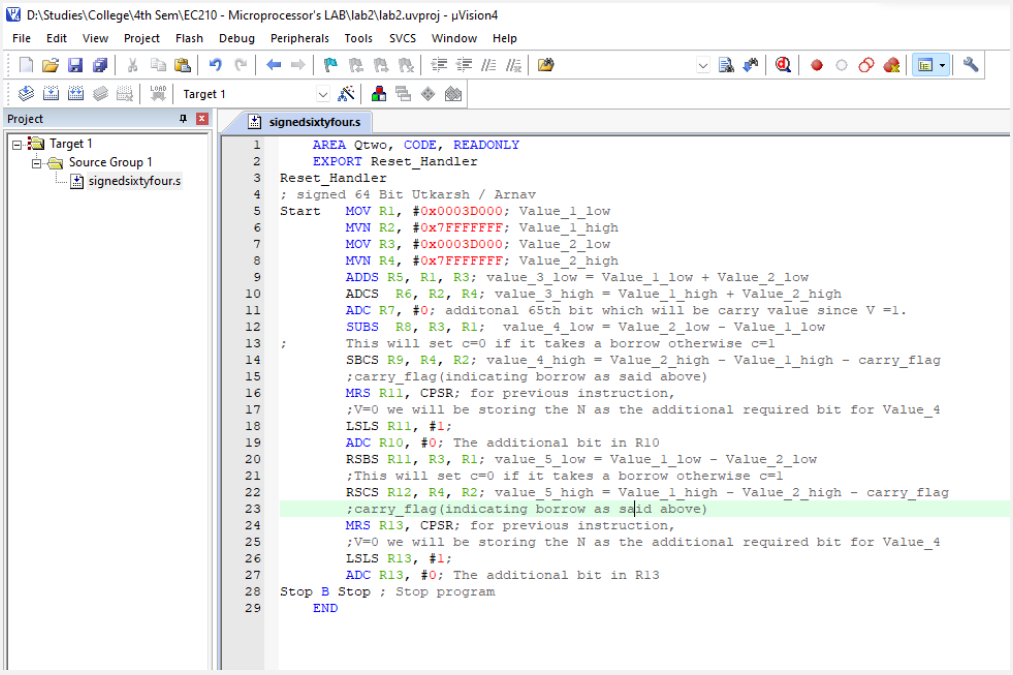


(b) Repeat ex 2.1 a,b,c for 64 bit signed numbers.

-> Source Code:

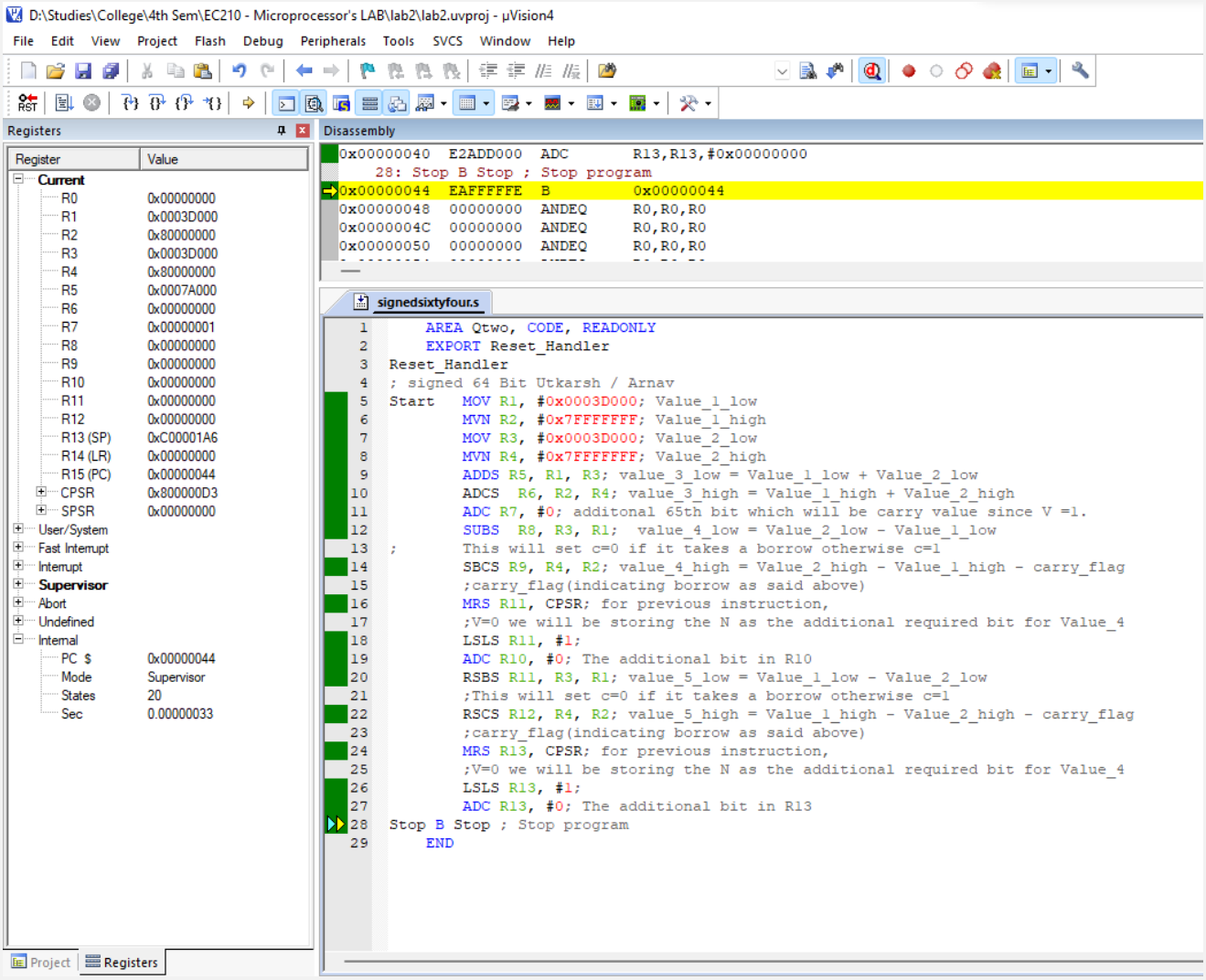
```
    AREA Qtwo, CODE, READONLY
    EXPORT Reset_Handler
Reset_Handler
; signed 64 Bit Utkarsh / Arnav
Start   MOV R1, #0x0003D000; Value_1_low
        MVN R2, #0x7FFFFFFF; Value_1_high
        MOV R3, #0x0003D000; Value_2_low
        MVN R4, #0x7FFFFFFF; Value_2_high
        ADDS R5, R1, R3; value_3_low = Value_1_low + Value_2_low
        ADCS  R6, R2, R4; value_3_high = Value_1_high + Value_2_high
        ADC R7, #0; additonal 65th bit which will be carry value since V =1.
        SUBS  R8, R3, R1;  value_4_low = Value_2_low - Value_1_low
;       This will set c=0 if it takes a borrow otherwise c=1
        SBCS R9, R4, R2; value_4_high = Value_2_high - Value_1_high - carry_flag
        ;carry_flag(indicating borrow as said above)
        MRS R11, CPSR; for previous instruction,
        ;V=0 we will be storing the N as the additional required bit for Value_4
        LSLS R11, #1;
        ADC R10, #0; The additional bit in R10
        RSBS R11, R3, R1; value_5_low = Value_1_low - Value_2_low
        ;This will set c=0 if it takes a borrow otherwise c=1
        RSCS R12, R4, R2; value_5_high = Value_1_high - Value_2_high - carry_flag
        ;carry_flag(indicating borrow as said above)
        MRS R13, CPSR; for previous instruction,
        ;V=0 we will be storing the N as the additional required bit for Value_4
        LSLS R13, #1;
        ADC R13, #0; The additional bit in R13
Stop B Stop ; Stop program
    END
```

Setup:



Debugging:

End Result:

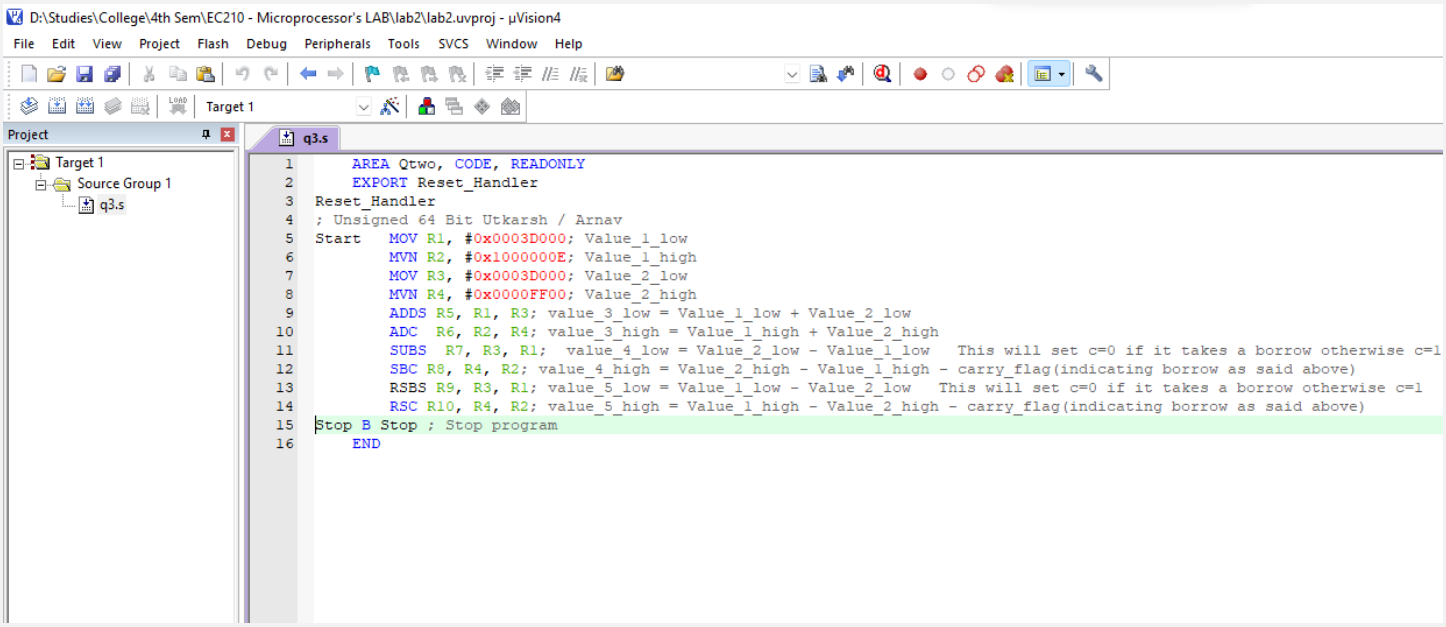


(c) Repeat ex 2.1 a,b,c for 64 bit unsigned numbers.

-> Source Code:

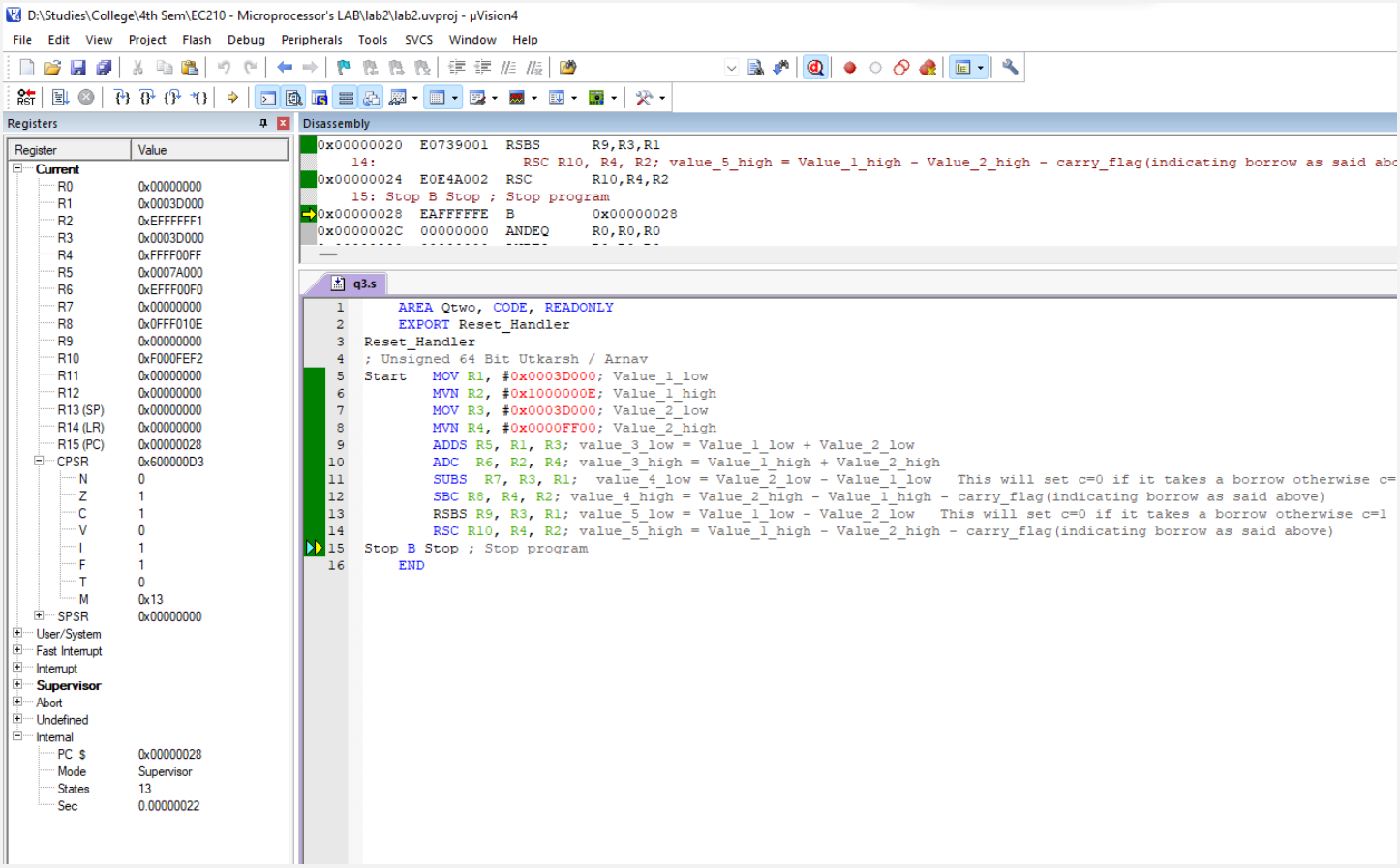
```
    AREA Qtwo, CODE, READONLY
    EXPORT Reset_Handler
Reset_Handler
; Unsigned 64 Bit Utkarsh / Arnav
Start   MOV R1, #0x0003D000; Value_1_low
        MVN R2, #0x1000000E; Value_1_high
        MOV R3, #0x0003D000; Value_2_low
        MVN R4, #0x0000FF00; Value_2_high
        ADDS R5, R1, R3; value_3_low = Value_1_low + Value_2_low
        ADC  R6, R2, R4; value_3_high = Value_1_high + Value_2_high
        SUBS  R7, R3, R1;  value_4_low = Value_2_low - Value_1_low
        ;  This will set c=0 if it takes a borrow otherwise c=1
        SBC R8, R4, R2; value_4_high = Value_2_high - Value_1_high - carry_flag
        ;carry_flag(indicating borrow as said above)
        RSBS R9, R3, R1; value_5_low = Value_1_low - Value_2_low
        ; This will set c=0 if it takes a borrow otherwise c=1
        RSC R10, R4, R2; value_5_high = Value_1_high - Value_2_high - carry_flag
        ; This will set c=0 if it takes a borrow otherwise c=1
Stop B Stop ; Stop program
    END
```

Setup:



Debugging:

End Result:


D:\Studies\College\4th Sem\EC210 - Microprocessor's LAB\lab2\lab2.uvproj - µVision4
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Registers
Register Value
Current
R0 0x00000000
R1 0x0003D000
R2 0xEFFFFFF1
R3 0x0003D000
R4 0xFFFF00FF
R5 0x0007A000
R6 0xEFFF00F0
R7 0x00000000
R8 0x0FFF010E
R9 0x00000000
R10 0xF000FEF2
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x00000028
CPSR 0x600000D3
N 0
Z 1
C 1
V 0
I 1
F 1
T 0
M 0x13
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000028
Mode Supervisor
States 13
Sec 0.00000022
Disassembly
0x00000020 E0739001 RSBS R9,R3,R1
14: RSC R10, R4, R2; value_5_high = Value_1_high - Value_2_high - carry_flag(indicating borrow as said abo
0x00000024 E0E4A002 RSC R10,R4,R2
15: Stop B Stop ; Stop program
0x00000028 EAFFFFFE B 0x00000028
0x0000002C 00000000 ANDEQ R0,R0,R0
q3.s
1 AREA Qtwo, CODE, READONLY
2 EXPORT Reset_Handler
3 Reset_Handler
4 ; Unsigned 64 Bit Utkarsh / Arnav
5 Start MOV R1, #0x0003D000; Value_1_low
6 MVN R2, #0x1000000E; Value_1_high
7 MOV R3, #0x0003D000; Value_2_low
8 MVN R4, #0x0000FF00; Value_2_high
9 ADDS R5, R1, R3; value_3_low = Value_1_low + Value_2_low
10 ADC R6, R2, R4; value_3_high = Value_1_high + Value_2_high
11 SUBS R7, R3, R1; value_4_low = Value_2_low - Value_1_low This will set c=0 if it takes a borrow otherwise c=
12 SBC R8, R4, R2; value_4_high = Value_2_high - Value_1_high - carry_flag(indicating borrow as said above)
13 RSBS R9, R3, R1; value_5_low = Value_1_low - Value_2_low This will set c=0 if it takes a borrow otherwise c=1
14 RSC R10, R4, R2; value_5_high = Value_1_high - Value_2_high - carry_flag(indicating borrow as said above)
15 Stop B Stop ; Stop program
16 END